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Design and Implementation of 1:2 Power Divider for Radar Applications

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ABSTRACT: This paper describes the design and simulation of 1:2 power divider using lumped element model at 53 MHz frequency for radar applications using ADS (Advanced Design System) software. This device provides maximum isolation among three ports. This device is highly advantageous for limited bandwidth applications.

KEYWORDS: RADAR, Wilkinson Power Dividers, ADS.

I.INTRODUCTION

RADAR (Radio Detection and Ranging) works on the principle that when a pulse of electromagnetic wave is directed towards a remotely located object, the pulse is returned through either reflection or scattering, providing information about the object. The power divider is a part of back-end receiver of radar. Various RF applications require power to be distributed among various paths. The easiest way could be possible by utilizing a power splitter/divider. Power dividers are reciprocal devices, i.e. they can also be used to combine the power from output ports into the input port. The power dividers are widely used in microwave circuit designs. A power divider is a three-port microwave device that is used for power division or power combining. In an ideal power divider the power given in port 1 is equally split between the two output ports for power division and vice versa for power combining is shown in figure1.



Figure 1: 1:2 Power Divider with Quarter Wavelength Section

At higher frequencies (above 500 MHz) these devices are usually realized as a micro strip or Strip line Wilkinson design. Figure 1 shows a simple 2-Way or 1:2 Wilkinson power divider. Being a lossless reciprocal three port network, it acquires every one of its properties which express that this kind of network can't have all the ports simultaneously matched.

To solve this, isolating resistor is placed between the two output ports, since no current flows through the resistor, this resistor does not contribute to any resistive loss. This makes an ideal Wilkinson a 100% efficient device. This resistor also provides excellent isolation even when the device is used as a combiner. Another property of the Wilkinson divider is that it is separated into quarter wavelength (1/4) sections.



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In this paper, it proposes designing of a 1:2 Power divider using Advanced design system with theoretical calculations. At low frequencies the size of the quarter-wavelength segments gets exceedingly large. The conventional approach is to reduce the size of the circuit is by replacing the transmission lines with its lumped components. An equivalent circuit diagram is shown below in figure 2.



Figure 2: Lumped Model Power Divider

II. THEROTICAL EVALUATION OF LUMPED COMPONENTS FOR ANALYSIS

The scattering parameters (S-parameters) for the proposed Wilkinson Power Divider are evaluated using even- and odd-mode analysis to find the incident and reflected voltages at the ports.

Firstly, apply a voltage source with impedance Z_o at port 2 with port 1 and 3 terminated with Z_o (Z_o being the system impedance). The circuit is split into two along the horizontal axis, with a positive port at the upper half and a negative at the lower half, as shown in Figure 3. This circuit has odd symmetry which implies that the symmetry line turns into a virtual short. Now treat the upper and lower parts of the circuit as separate.

A. ODD MODE ANALYSIS:



Figure 3: Setup for Odd Mode Wilkinson Power Divider Analysis

As shown in figure 3, the V_1° (o indicates odd) is zero since this port is short-circuited. Since the line is a quarter wavelength, the short is changed to an open at port 2 and 3. So from simple voltage division rule, found $V_2^{\circ} = Vs/4$ and $V_3^{\circ} = -Vs/4$.

Now, use the even mode circuit in Figure 4 to find the even mode voltages. Due to even mode symmetry, the symmetry line represents a virtual open. The $2*Z_0$ resistor at port 1 transforms (using the quarter wavelength formula) to Z at ports 2 and 3. Using simple voltage division again, found $V_2^o = V_s/4$ and $V_3^o = V_s/4$. In the event that apply the telegraphers mathematical statement with the limit conditions, found that $V_1 = -jV_s/(2\sqrt{2})$.



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B. EVEN MODE ANALYSIS:



Figure 4: Setup for even mode Wilkinson power divider analysis.

By adding the odd and even voltages (superposition), find the total voltages at the ports, which is the sum of the incident and reflected voltages. Doing this gives V1=-jVs/($2\sqrt{2}$), V =V /4 and V =0. Since ports 1 and 3 is terminated in Z, the reflected voltages at these two ports must be zero, so V₁⁺=0, V₁⁻=-jVs/($2\sqrt{2}$), V₃⁺=0 and V₃⁻=0. Now, since the source impedance at port 2 is matched to the line impedance, which is electrically small, gives V₂⁺=Vs/2 and V₂⁻=0. Necessary voltages are calculated to find S12, S22 and S32:

 $S12 = \frac{v_1^{-1}}{v_2^{+}} = \left(\frac{-jv_s}{2\sqrt{2}}\right)\frac{2}{v_s} = \frac{-j}{\sqrt{2}}$ $S22 = \frac{v_2^{-1}}{v_2^{+}} = (0)\frac{2}{v_s} = 0$ $S32 = \frac{v_3^{-1}}{v_2^{+}} = (0)\frac{2}{v_s} = 0$

From symmetry property, the parameters S13 = S12, S33 = S22 and S23 = S32. While reciprocity gives, S21 = S12 and S31 = S13.

To find S11, move the source to port 1 and use even symmetry as shown in figure 5.



Figure 5: Setup for even mode Wilkinson power divider analysis to find s11.

Using the upper half of the circuit, transform the load at port 2 to the input and apply voltage division to find V₁=Vs/2. Using the same logic for V₂ above, obtained V₁⁺=Vs/2 and V₁⁻=0. Now S11 is easily found as: $S11=\frac{V_1^-}{V_1^+}=(0)\frac{2}{V_c}=0$

Therefore, the S-parameter matrix for an ideal Wilkinson Power Divider is given below:



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$$\mathbf{S} = \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & 0 & 0 \\ \frac{-j}{\sqrt{2}} & 0 & 0 \end{bmatrix}$$

Figure 6: S-Parameter matrix for an ideal Wilkinson power divider.

C. DESIGN OF LUMPED MODEL WILKINSON POWER DIVIDER

Calculate the values of the capacitances (C1, C2 & C3), inductances (L1 & L2) and resistance (R1) required for the Lumped model using the given formulae.

$$\begin{split} &Z_o = 500 \text{hm} \ f_c = 53 \text{MHz} \\ &\text{The characteristic impedance of the λ/4 length transmission line is} \\ &\text{Ro} = \sqrt[4]{N*Z_o}, \\ &\text{Where N=2 because we are using two output ports} \\ &\text{Therefore Ro} = \sqrt{2} * 50 = 70.7 \text{ohms} \\ &\text{L} = (\sqrt{N} * Z_o / \omega_o), \text{ where } \omega_o = 2\pi \text{fc} \\ &= (\sqrt{2} * 50/2\pi * 53 * 106) \\ &= 212 \ \text{nH} \\ &\text{C} = (1/\sqrt{N*\omega_o} * Z_o) \\ &= (1/\sqrt{2} * 2\pi * 53 * 106 * 50) \\ &= 42 \text{pF} \end{split}$$

III.SCHEMATIC SIMULATION PROCEDURE FOR 1:2 POWER DIVIDER

The theoretically evaluated lumped component circuit diagram of Wilkinson power divider using ADS is shown in figure7.



Figure 7: Design of 1:2 power divider using ads.

The Wilkinson power divider has one input port and two output ports. The three ports are isolated with each other. The performance of the network for S-parameters is studied using 50 Ohms termination at all the ports.

A.SIMULATION RESULTS:

The frequency responses of the developed Wilkinson power divider are studied in the range of 50 to 60 MHz and with step size of 1MHz is shown in the figure 8.



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Figure 8: Frequency Responses Of S (1, 1), S (2, 1), S (2, 2), S (3, 2)

The return loss S (1, 1) is of 46.552dB at port 1 and S (2, 2) of 62.630dB at port 2 A high return loss is desirable and results in a lower insertion loss

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The insertion loss S (2, 1) shows the attenuation from input to output is 3dB therefore the signal at port 1 is split equally between port 2 and port 3 without loss.

Insertion losses= 10 log N

S (3, 2) shows the isolation between the ports.

B.PHASE SHIFT:

The phase shift of the system is also studied from 50 to 60 MHz range. We can see all the S-parameter except S21 show resonance at the design frequency. The output of the system shows 900 phase shift for parameter S21 in figure 9.



Figure 9: Variation of phase response of S (1, 1), S (2, 1), S (2, 2), S (3, 2) with respect to frequency response.

Therefore the developed network system possesses the favorable characteristics of flat frequency response at 53 MHz and a perfect phase shift about 90° . Therefore no instrumentation system possesses all the required specifications to act as a device at the load end of the system.



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IV. CONCLUSION

The 1:2 Power Divider for radar applications have been successfully designed and simulated using the Advanced Design System. The power divider has a good insertion loss of 3dB, return loss of <30dB and phase response of 90dB. This system with necessary minor or major notification will suits to the requirements of various power divider networks employed in driving circuits.

REFERENCES

[1] First winter school on Indian MST Radar jan-28-feb 4, 1991, SV University Tirupati

[2] Second winter school on Indian MST Radar lecture notes feb-1995, editor by A.R JAIN, D. Narayana Rao.

[3] Pozar, D. M., Microwave Engineering, John Wiley & Sons, Inc., 2005, third Ed., pp. 318-324.

[4] www.microwaves101.com.

[5] Application notes on power dividers.

[6] Agilent EEs of EDA Advanced Design System Circuit Design Cookbook2.0

BIOGRAPHY



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