



Design of Tunable Versatile Filter Using Operational Trans-conductance Amplifier

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ABSTRACT: In this paper, design of a CMOS tunable versatile filter using current conveyor (CC) is presented. The filter is realized at the same time as on the chip is tunable for low pass, band pass, high pass, and elliptical notch filter. The circuit utilizes two current conveyors, one Operational Trans-conductance Amplifier (OTA), four resistors and two grounded capacitors, ideal for integration. It has only one output terminal and the number of input terminals may be used. Further, there is no further requirement of component matching in the circuit.

KEYWORDS: CMOS, Current Conveyor, OTA, Tunable Versatile Filter

I. INTRODUCTION

The controlled quadrature optical filters are extremely useful for the circuits of various communication applications such as compact portable spectroscopy and hyper-spectral imaging for real-time, medical diagnostics, surveillance and defence. Now a day's Tunable optical filters having a very wide range of applications from spectroscopy to optical communication networks, to remote sensing as well as biomedical imaging and diagnostics [1]. The bi-layer Polarization Grating (BPG) is a novel diffractive optical element, which allows the implementation of a tunable photo sensitive filter completely un-responsive to input polarization and exhibiting the high peak value of transmittance and a potential in favor of very low cost and compact implementation. Consider the theory and fabrication of the BPG itself, highlighting its compelling properties and unique advantages for the tunable filter application. Introducing two configurations of a tunable optical filter is based on BPGs and analyzes it in terms of key filter parameters including bandwidth, free-spectral-range, peak transmittance and maximum tuning range [2]. The applications of tunable optical filters are many and varied ranging from astronomy to medicine, education, remote-sensing, optical communications and even the cosmetics industry [3].

II. CURRENT CONVEYOR

The current conveyor is a basic building block that can be implemented in analog circuit design. This was introduced by Sedra and Smith in 1968 [16]. In recent years, current-mode circuits have emerged as an important class of circuits with Current conveyors can be used in variety of applications ranging from universal and multifunction filters, oscillators etc. Current conveyors can provide larger band-width and are suitable for low voltage applications. Operational amplifier does not perform well where a current output signal is needed and consequently there is an application field for current conveyor circuits [4]. There is no feedback in current conveyor, so it is able to give high frequency behaviour as compared to Op-Amp. In a conventional Op-Amp there is a gain bandwidth product limitation so it is not suitable for high frequency. Block representation of current conveyor is given operations in fig. 1; a current is a three port network. Current conveyor represents emerging class of high performance analog circuit design based on current mode approach. It has simple architecture, wider bandwidth and capability to operate at low voltage developments in the field of current conveyor can be classified:-

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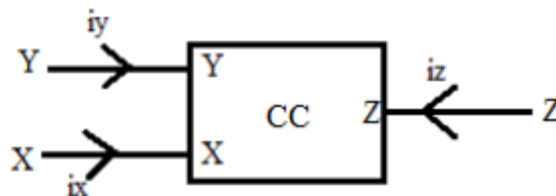


Fig. 1 Block diagram of Current Conveyor

- First Generation Current conveyor, CCI.
- Second Generation Current conveyor, CCII.
- Third conveyor, CCIII. Generation Current

A. First and Second Generation Current Conveyor

The concept of the current-conveyor was first accessible in 1968. The current-conveyor is proposed as a general building block as with the operational amplifier [7]. Because of the operational amplifier concept has been current since the late, it is difficult to get any other similar concept widely accepted. However, operational amplifiers do not perform well in applications where a current output signal is needed and consequently there is an application field for current. The second generation current conveyor (CCII) is one of the most versatile current-mode building block for many applications, a high impedance input port is preferable in order to avoid loading effect. So, second generation current conveyor was developed to fulfil this requirement. It has one high and another is low impedance input port rather than the two low impedance input ports of CCI [5] [6]. Since its introduction in 1970, it has been used in a wide range of applications and several circuits have been realized using this block. The CCII can be considered as the basic analog circuit design block because all the active devices can be made of a suitable connection of one or two CCII. It is a three terminal device. This current conveyor differs from the first generation current conveyor in a sense that the port Y is a high impedance port i.e. there is no current flowing into port Y. The port Y of the second generation current conveyor is used as a voltage input and port Z is used as a current output port [7]. Whereas, the port X can be used as a voltage output or as a current input port. Therefore, this current conveyor can be used to process both voltage and current signals. There are two types of second generation current conveyors:

- Positive current conveyor (CCII+) in which the currents i_x and i_z have the same direction as in a current mirror.
- Negative current conveyor (CCII-) in which currents i_x and i_z have the different direction as in current buffer

The class AB topology of second generation, to ensure correct operation the bias current I_{bias1} and I_{bias2} have to be equal. Unlike in the first generation push-pull conveyor, in this conveyor the quiescent current is set directly by I_B by two current sources. Here the current flow through X is nonlinearly divided in to signal path through either an NMOS or a PMOS current mirror which are summed up at port Z. characteristics is nearly 1 [8] [9]. Like CCI, the impedances at X and Y terminals of the CCIII are low. CCIII is very useful in many applications as it provides the current in the floating terminal. The main features of CCIII are low gain errors, high linearity and wide frequency response. In addition, the cascading of CCIII with other circuits is easier owing to high output impedance at Z-terminal, without need of additional active element. It may also be used as the input cell of probes.

III. DESIGN ISSUE WITH FILTER

The voltage-mode of filters employing current conveyors has been receiving attention these days. More-over, it is good for a circuit to employ only grounded passive elements especially grounded capacitors and not require passive component-matching conditions therefore it is convenient for fully integrated circuit technology. Second generation current controlled conveyors (CCII) have recently become popular for realizing tunable functions as their port-X tunable resistance can be controlled through the bias current of conveyor. Thus several electronic functions using these devices have been reported in the introduction [10].

A. Description of the Circuit

Tank voltage amplitude has an important effect on the phase noise, as emphasized by the presence of q_{max} in the denominator of the expression for the single-sideband phase noise

$$\frac{V_{o1}}{V_{in}} = \frac{sC_2G_{X1}}{s^2C_1C_2 + sC_2G_{X1} + G_{X1}G_{X2}}$$

$$\frac{V_{o2}}{V_{in}} = \frac{-G_{X1}G_{X2}}{s^2C_1C_2 + sC_2G_{X1} + G_{X1}G_{X2}}$$

$$\frac{V_{o3}}{V_{in}} = \frac{s^2C_1C_2}{s^2C_1C_2 + sC_2G_{X1} + G_{X1}G_{X2}}$$

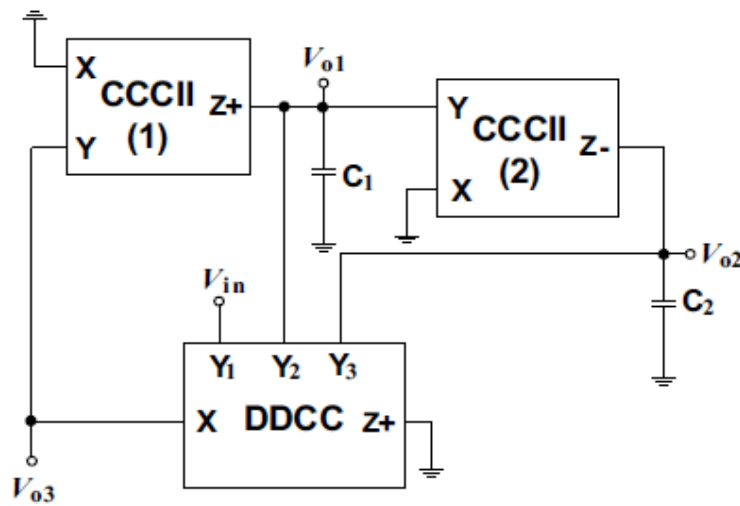


Fig 2. Current flow when the stage is switched to one side

It is the power spectral density of the current where it is the rms value of the impulse noise, sensitivity function associated with that noise source, q_{max} is the maximum signal charge swing, and $\Delta\omega$ is the offset frequency from the carrier [11]. A simple expression for the tank amplitude can be obtained assuming that the current in the differential stage switches quickly from one side to another. Fig. 2 shows the current flowing in the complementary cross-coupled differential LC oscillator when it is completely switched to one side. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modelled as a current source switching between I_{tail} and $-I_{tail}$ in parallel with a resistance, inductance and capacitance (RLC) tank, as shown in Fig. 2 it is the equivalent parallel resistance of the tank [12] [13].

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B. Rectangular current waveform

At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as

$$\omega_o = \sqrt{\frac{G_{X1}G_{X2}}{C_1C_2}} \quad \text{and} \quad Q = \sqrt{\frac{C_1G_{X2}}{C_2G_{X1}}}$$

This mode of operation is referred to as the current-limited regime of operation since, in this regime, the tank amplitude is solely determined by the tail-current source and the tank equivalent resistance. Fig. 2 shows the simulated node voltages as well as the drain currents of the NMOS transistors, M1 and M2, in this regime of operation. The value of L and C are such that the circuit oscillates at 1 GHz [14] [15].

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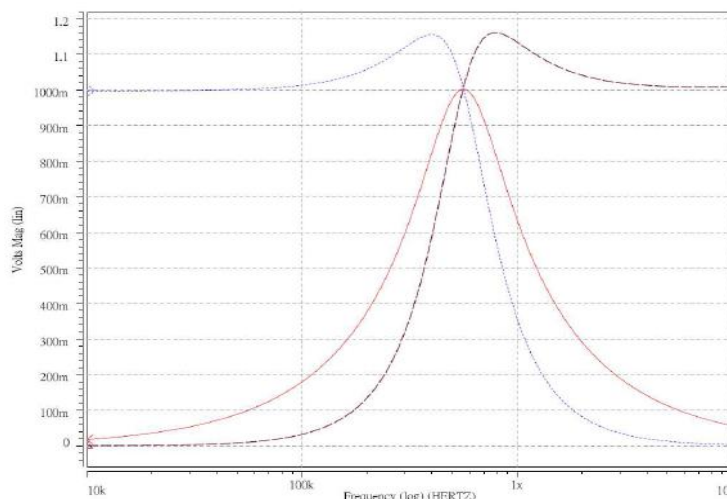


Fig. 3. The high pass, band pass and low pass amplitude-frequency response

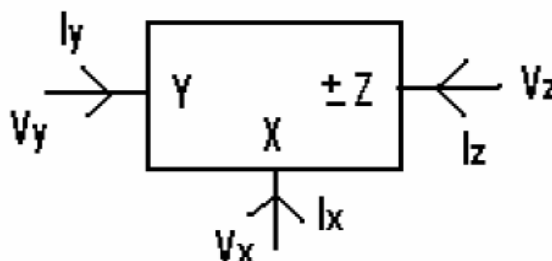


Fig. 4 Block diagram of the filter section

The amplitude approaches the supply voltage because of both NMOS and PMOS pairs that will be enter the triode region at the peaks of the voltage. Also the tail NMOS transistor may spend most (or even all) of its time in the linear region.

IV. DESIGN OF FILTER USING CURRENT CONVEYOR

Active filters with current/voltage controllable frequency have a wide range of applications in the signal processing and instrumentation area. The realization on chip MOSFET as voltage controlled resistor. Their contributions and several other research papers may be considered to be motivation for the VLSI industry to make on chip tunable filters. These realizations have small range of variation in the frequency. The OTA-C structure is highly suitable for realizing electronically tunable continuous time filters. A number of voltage mode/current mode OTA-C bi-quard has been reported in the literature. Multiple-input multiple-output (MIMO), multiple-input single-output (MISO) and single-input multiple-output (SIMO) type circuits have also appeared in the literature. A third order current mode oscillator, based on current conveyor and VDTA. The features of the proposed circuits are that the oscillation conditions can be adjusted independently from the oscillation frequency by electronic method. The circuit construction consists of 1DDCC, 1 VDTA, 1 grounded resistor and 2 grounded capacitors. The PSPICE simulation results are shown; the electrical behaviours of the ideal DDCC are represented by the following hybrid matrixes which are in correspondence with the theoretical analysis.

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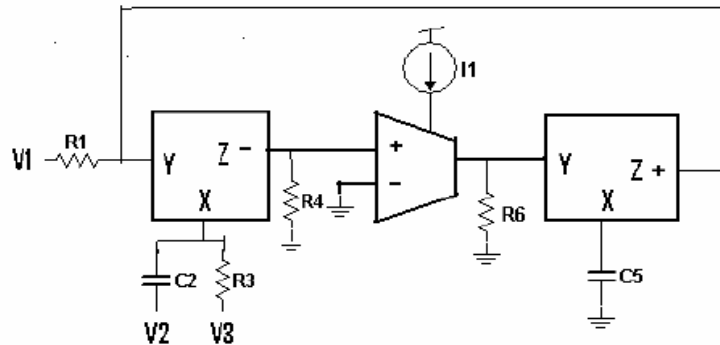


Fig. 5 Proposed circuit using current conveyor

1) Design using CCHs:

The circuit symbol of CC-II is shown in Fig. 4, where VP and VN are the input terminals, Z and X is the output ones. Hence, Z is the current output terminal; current through Z terminal follows the difference of the voltages at VP and VN terminals by trans-conductance of gm1. The voltage vZ on Z terminal is transferred into current using trans-conductance gm2, which flows into output terminal X.

$$V_{out} = \frac{1}{D(s)} \left(s^2 C_2 C_5 R_1 R_3 R_4 R_6 g_m V_2 + R_3 V_1 + \right)$$

$$D(s) = s C_5 g_m R_1 R_4 R_6 V_3$$

Where

$$D(s) = s^2 C_2 C_5 g_m R_1 R_3 R_4 R_6 + s C_5 g_m R_1 R_4 R_6 + R_3$$

The gm1 and gm2 are tuned by IB1 and IB2, respectively. In general, CDTA can contain an arbitrary number of x terminals, providing currents IX of both directions. All terminals of VDTA exhibit high impedance values. The characteristics of the ideal VDTA are represented by the following hybrid matrix: If the VDTA is realized using CMOS technology, gm1 and gm2 can be respectively written as

$$g_{m1} = \sqrt{k I_{B1}},$$

and

$$g_{m2} = \sqrt{k I_{B2}}.$$

Here k is the physical trans-conductance parameter of the CMOS transistor. IB1 and IB2 are the bias current used to control the gm1 and gm2, respectively.

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TABLE I. VARIOUS FILTER RESPONSES

Filter\Input	V ₁	V ₂	V ₃
Low-pass	1	0	0
High-pass	0	1	0
Band-pass	0	0	1
Notch	1	1	0

$$\omega_0 = \sqrt{\frac{1}{R_1 R_4 R_6 C_2 C_5 g_m}}$$

$$\frac{\omega_0}{Q} = \frac{1}{R_3 C_2}$$

$$Q = R_3 \sqrt{\frac{C_2}{g_m R_1 R_4 R_6 C_5}}$$

2) General structure of CCII's:

The oscillator is designed by cascading an inverting second order low-pass filter and the lossless integrators as systematically. Fig. 4, we will receive the characteristic equation as

$$s^3 + bs^2 + as + ck = 0$$

The condition of oscillation (OC) and frequency of oscillation (FO) can be written as

$$OC : ab = ck$$

and

$$\omega_{osc} = \sqrt{a}$$

From Eq. (5), if $a = c$, the oscillation condition and oscillation frequency can be adjusted independently, which are the oscillation condition able to be controlled by b and k , while the oscillation frequency can be tuned by a .

3) Structure of proposed Filter

The completed 3rd current-mode quadrature oscillator is shown in Fig. 4. The condition of oscillation and frequency of oscillation can be written as

$$\frac{1}{C_1 R} = \frac{g_{m2}}{C_3},$$

and

$$\omega_{osc} = \sqrt{\frac{g_{m1}}{C_1 C_2 R}}$$

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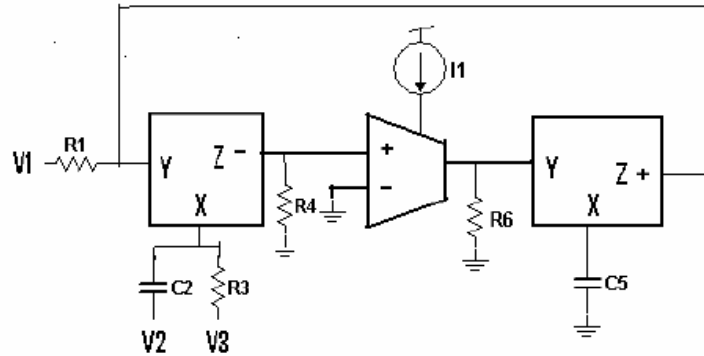


Fig. 6 Proposed current-mode oscillator

If $m_1 B_1 g = kI$, $m_2 B_2 g = kI$ and $C_1 = C_2 = C_3 = C$, the condition of oscillation and frequency of oscillation can be rewritten as

$$\frac{1}{R} = \sqrt{kI_{B2}} ,$$

and

$$\omega_{osc} = \frac{1}{C} \sqrt{\frac{(kI_{B1})^2}{R}} .$$

It is obviously found that, the condition of oscillation and frequency of oscillation can be adjusted independently; which are the oscillations of oscillation can be controlled by setting I_{B2} , while the frequency of oscillation can be tuned by setting I_{B1} . From the circuit in Fig. 4, the current transfer function from I_{o1} to I_{o2} is

$$\frac{I_{o2}(s)}{I_{o1}(s)} = \frac{g_{m1}}{sC_2} .$$

For sinusoidal steady state, becomes

$$\frac{I_{o2}(j\omega)}{I_{o1}(j\omega)} = \frac{g_{m1}}{\omega C_2} e^{-j90^\circ} .$$

The phase difference ϕ between I_{o1} and I_{o2} is $\phi = -90^\circ$ ensuring that the currents I_{o2} and I_{o1} are in quadrature.

V. OUTPUT OF PROPOSED FILTER

The working of the proposed oscillator has been verified in PSpice simulation software. Internal constructions of DDCC and VDTA used in simulation are respectively shown in Fig. 6 and 7. The PMOS and NMOS transistors have been simulated by respectively using the parameters of a 0.25 μ m TSMC-CMOS technology. The transistor aspect ratios of PMOS and NMOS transistor are indicated in Table I. The circuit was biased with $\pm 1.25V$ supply voltages, $V_{BB} = -0.55V$, $C_1 = C_2 = C_3 = 50pF$, $I_{B1} = I_{B2} = 60\mu A$ and $R = 3.5k\Omega$. This yields simulated oscillation frequency of 1MHz. Fig. 8 shows simulated quadrature output waveforms. Fig. 8 shows the simulated output spectrum, where the total harmonic distortion (THD) is about 2.95%. The quadrature relationship between the generated waveforms has been verified using Lissajous figure and shown in Fig. 8. The power consumption is approximately 1.76mW.

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TABLE I
DIMENSIONS OF THE TRANSISTORS

Transistor	W (μm)	L (μm)
M ₁ -M ₄	3	0.25
M ₅ -M ₈	1	0.25
M ₉ -M ₁₀	10	0.25
M ₁₁ -M ₁₂ , M ₁₃ -M ₁₆	5	0.25
M ₁₇ -M ₂₀	8	0.25

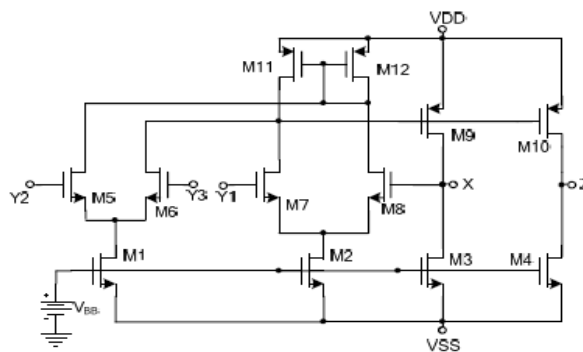


Fig. 7 Internal construction of the CMOS DDCC

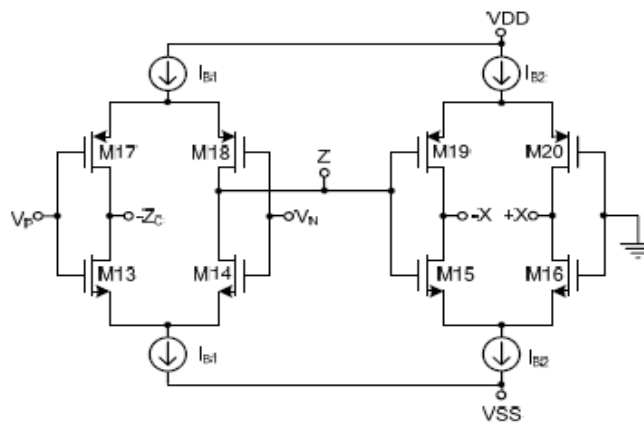


Fig. 8 Internal construction of the CMOS VDTA

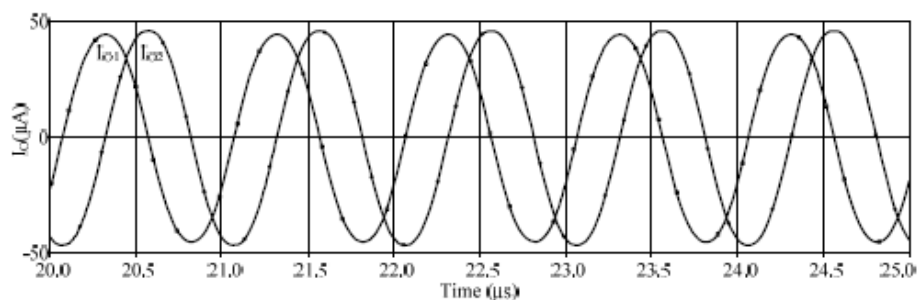


Fig. 9 The simulation result of quadrature outputs

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VI. RESULT

The complete circuit is simulated using commercially available AD844 and LM13700. The AD844 is used for the realization of CCII+ and CCII-. Table 1 displays the simulation result for the proposed filter. The circuit is designed for $\omega_0 = 8.7$ KHz and $Q=0.12$ by considering $R_1 = R_4 = R_6 = 10K\Omega$, $C_2 = C_5 = 10nF$, $R_3 = 14K\Omega$ and $g_m=13.2mS$. The theoretical results have been verified to match with simulation result. Figure 3 shows that the quality factor of the notch filter is very high. It is due to the transfer function of the notch filter is having complex conjugate zeros with zero real values. Figure 8 shows the cutoff/center frequency of the filter with respect to the changes in bias current of the OTA. The response is showing the when the bias current is higher than the output current of the OTA than the frequency variation is linear and circuit will be stable. The report which is obtained with the help of simulation contains different sections, of all the sections only the parameters obtained in the final report are shown.

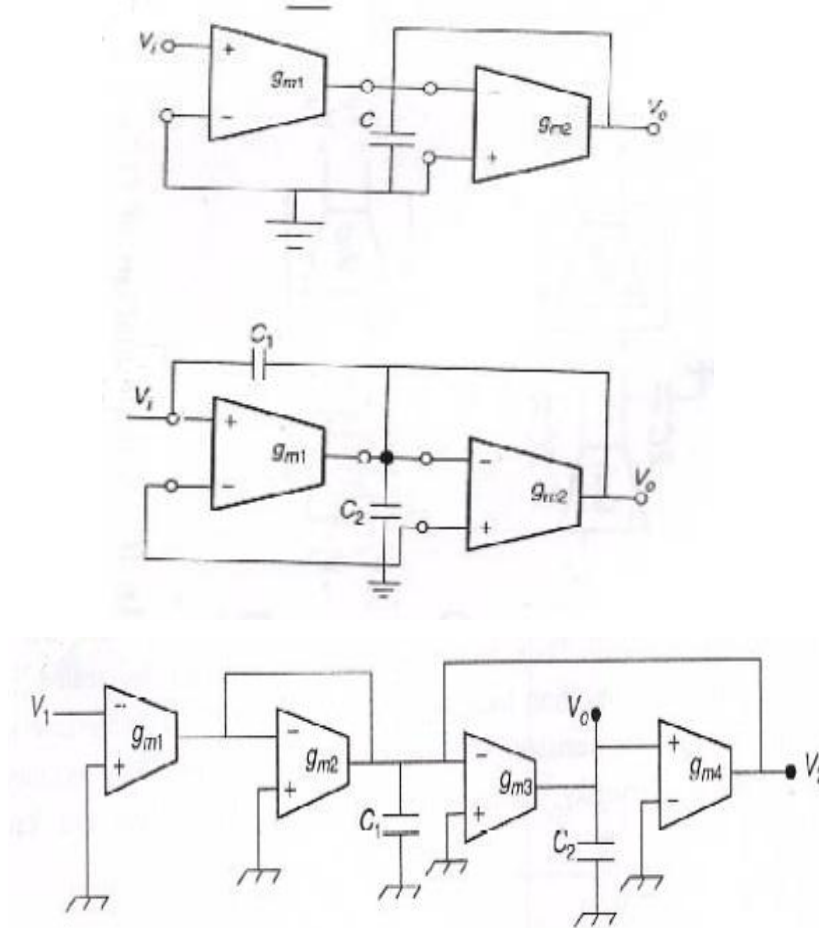


Fig. 10 Experimental designed of OTA

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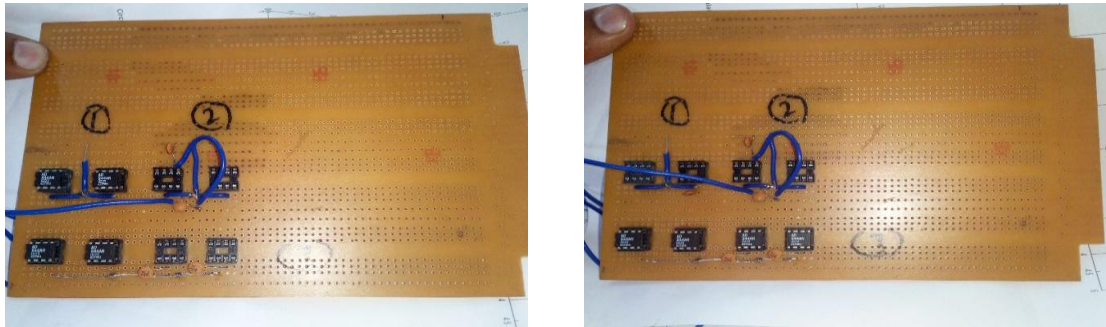


Fig. 11 Experimental designed of OTA on PCB

Table 1 Results for the output obtained

Frequency MHz	V _{Output} (dB)	Gain(dB)=V ₀ /V ₁ =20 log V ₀ /V ₁
80	0.001	-60
82	0.003162	-50
84	0.01	-40
86	0.031623	-30
88	0.1	-20
90	0.316228	-10
92	1	0

Output Graphical representation of OTA

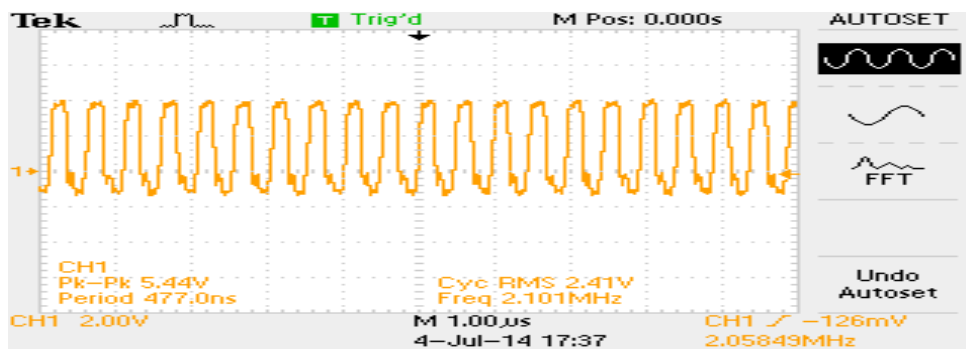


Fig. 12 Output graphical representation of OTA

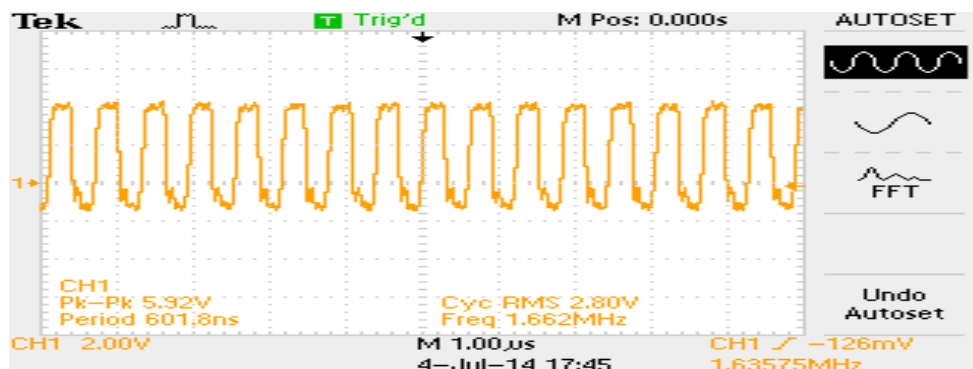


Fig. 13 Output graphical representation of OTA



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VII. CONCLUSION

The circuit proposed in this thesis generates low-pass, high pass, band-pass and notch filter using two current conveyors, four resistors and two capacitors. The circuit provides more number of filter realizations at the single output terminal. In addition of this proposed circuit does not have any matching constraint/cancellation condition. The circuit employs grounded capacitor, suitable for IC fabrication. The circuit enjoys the orthogonality between the cut-off frequency and the bandwidth. The OTA is linearly tunable when the bias current is higher than the output current. It has low sensitivities figure of both active and passive components.

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BIOGRAPHY



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