



Elimination of Leakage Current using HBZVR-D Topology

Merin Raphel¹, G.Rajkumar²

PG Student [Power Electronics & Drives], Dept. of EEE, NCERC, Pampady, Kerala, India

Assistant Professor, Dept. of EEE, NCERC, Pampady, Kerala, India

ABSTRACT: Small, light, low cost and high efficiency grid connected photovoltaic (PV) systems can be achieved when the transformer is omitted from the inverter. However, dangerous leakage current will flow between PV array and the grid due to the stray capacitance. In the past, various transformerless PV inverter topologies have been introduced, with leakage current minimized by means of galvanic isolation and common-mode voltage (CMV) clamping. Among them, it is found that H-bridge zero-voltage state rectifier (HBZVR) topology minimizes leakage current and CMV to the maximum extent since it is having both AC and DC bypasses. But better than HBZVR, leakage current can be minimized by adding an additional diode to the existing DC bypass, which is termed as HBZVR-D topology. Here, a simple modified topology is proposed, to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination. The performances of different topologies, in terms of CMV and leakage current are compared. The analyses are done theoretically and via simulation studies.

KEYWORDS: Common-mode voltage, leakage current, photovoltaic system, transformerless.

I.INTRODUCTION

Due to the rapid increase in human population and limited reserve of natural resources such as coal and fuel, solar power is considered to be a better option to meet these challenges since it is naturally available, pollution free and inexhaustible. Besides, with the help of government incentives and decrease in PV module prices, grid-connected PV systems play an important role in distributed power generation. The decrease in cost of PV system, the advancement of power electronics and semiconductor technology and incentives from government strongly encourage the growth of grid connected PV systems.

Grid connected PV system can be classified into two categories: with and without transformer. Most of the PV systems are designed with transformer for safety purpose with galvanic isolation. Galvanic isolation ensures no injection of DC current into the grid and reduces the leakage current between PV module and grid. In DC side, high frequency transformer is used whereas bulky low frequency transformer is used in output side of the inverter. However, the transformer is big, heavy and expensive. Also, it reduces the overall frequency of the conversion stage. To overcome these problems, transformerless PV system is introduced. It is smaller, lighter, cheaper and higher in efficiency.

However, safety issue is the main concern for the transformerless PV systems due to high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow from the PV to the grid. At the same time, the fluctuating potential, also known as common-mode voltage (CMV), charges and discharges the stray capacitance which generates high leakage current. Besides safety issue, this leakage current increases grid current ripples, system losses, and electromagnetic interference.

Hence, many research works have been proposed recently to eliminate the leakage current via galvanic isolation and CMV clamping techniques. Galvanic isolation topologies such as H5, H6, and HERIC introduce dc-decoupling and ac-decoupling to disconnect the PV and the grid. It is found that ac-decoupling provides lower losses due to reduced switch count in the conduction path. Nevertheless, the galvanic isolation alone cannot completely eliminate the leakage current due to the influence of switches' junction capacitances and parasitic parameters. Therefore, CMV clamping has been used in oH5, H6, and H-bridge zero-voltage state rectifier (HBZVR), as shown in Fig. 1(d)–(f), to completely

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

eliminate the leakage current. However, the clamping branch of HBZVR does not perform optimally. It is shown in the later section that the leakage current is as high as those of galvanic isolation topologies.

In this paper, several recently proposed transformerless PV inverters with different galvanic isolation methods and CMV clamping techniques, as shown in Fig. 1, are analyzed and compared.

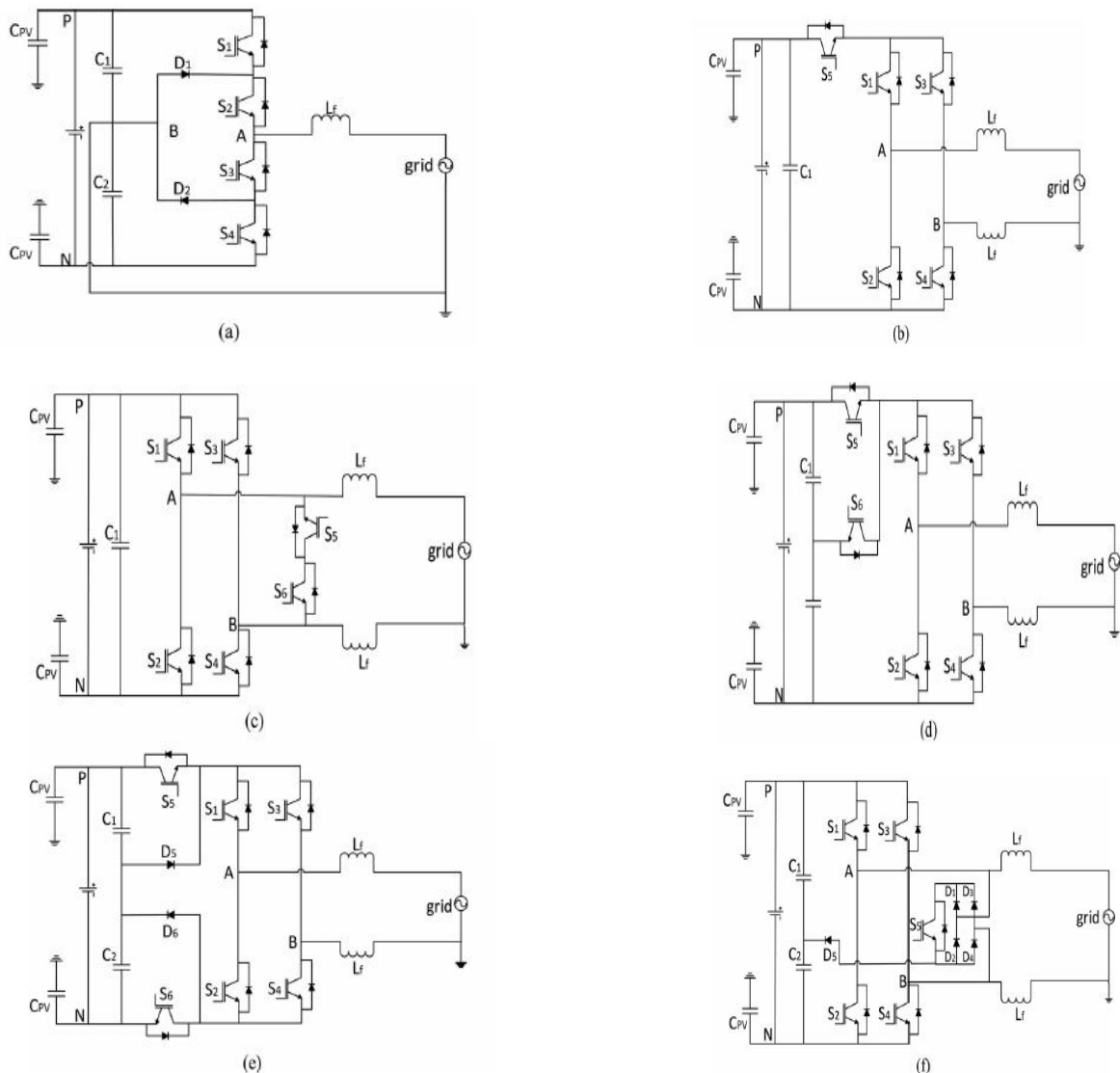


Fig. 1. Recently proposed transformerless topologies. (a) Diode-clamped topology. (b) H5 topology. (c) HERIC topology. (d) oH5 topology. (e) H6 topology. (f) HBZVR topology.

A simple modified HBZVR-D is also proposed, to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination. Performance of HBZVR-D is compared to other existing topologies in terms of CMV and leakage current.

II. COMMON-MODE BEHAVIOR AND LEAKAGE CURRENT REDUCTION METHODS

When the transformer is removed from the inverter, a resonant circuit is formed as shown in Fig. 2(a). This resonant circuit includes stray capacitance (C_{PV}), filter inductors (L_1 and L_2), and leakage current (I_L). Here, the power converter

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

is represented by a block with four terminals to allow a general representation of various converter topologies. On the dc side, P and N are connected to the positive and negative rail of the dc-link, respectively; while on the ac side, terminals A and B are connected to the single-phase grid via filter inductors. From the view point of the grid, the power converter block shown in Fig. 2(a) can be considered as voltage sources, generating voltage V_{AN} and V_{BN} . Hence, regardless of the conversion structure, this power converter block can be simplified into the equivalent circuit which consists of V_{AN} and V_{BN} as shown in Fig. 2(b). The leakage current is thus a function of V_{AN} , V_{BN} , grid voltage, filter inductance, and stray capacitance.

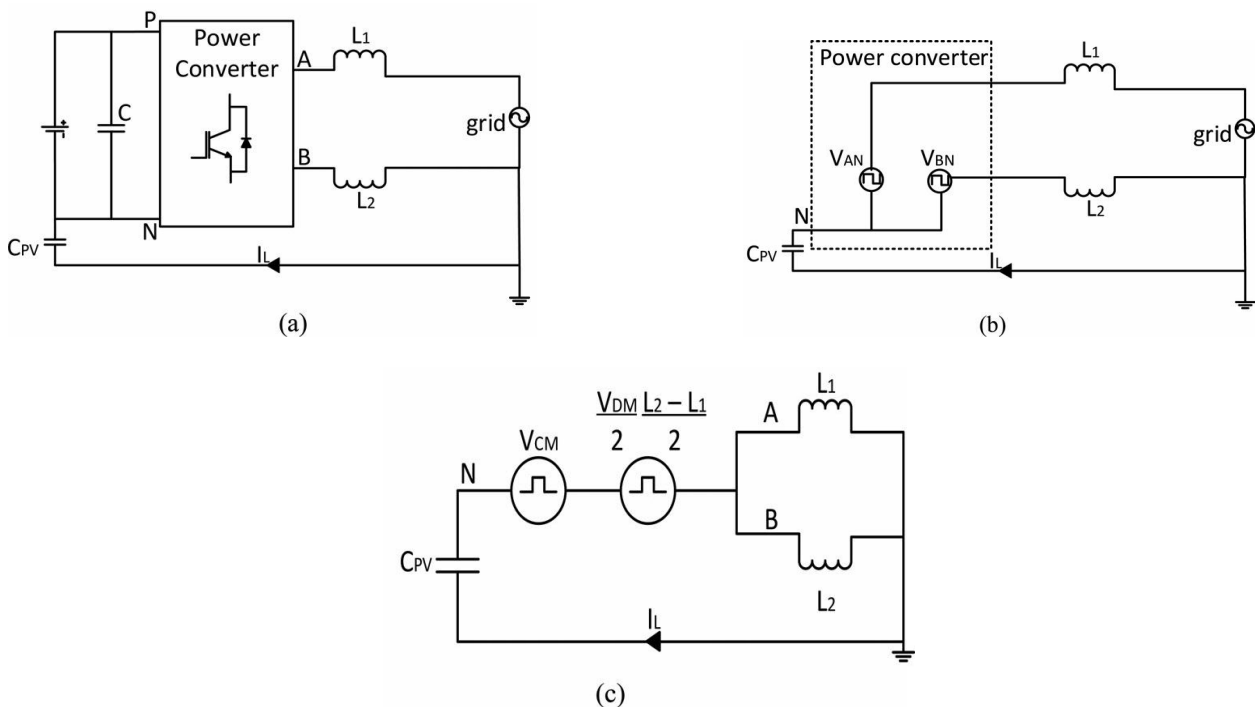


Fig. 2. Common-mode model for single-phase grid-connected inverter. (a) Full model. (b) Simplified model. (c) Simplified common-mode model.

The CMV V_{CM} and differential-mode voltage V_{DM} be defined as

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

$$V_{DM} = V_{AN} - V_{BN} \quad (2)$$

Rearranging (1) and (2), the output voltages can be expressed in terms of V_{CM} and V_{DM} as

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \quad (3)$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \quad (4)$$

Using (3)–(4) and considering only the common-mode components of the circuit, a simplified common-mode model can be obtained as in Figure. 2(c). The equivalent CMV (V_{ECM}) is defined as

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2} \frac{L_2 - L_1}{L_1 + L_2} \quad (5)$$

Since identical filter inductors ($L_1 = L_2$) are used, the V_{ECM} is equal to V_{CM}

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (6)$$

From the model, it can be concluded that the leakage current is very much dependent of the CMV. Thus, converter structure and the modulation technique must be designed to generate constant CMV in order to eliminate the leakage current. It is worth highlighting that the model in Fig.2(c) has been commonly used for describing the common-mode behaviour of the conventional full-bridge (H4) topology. However, due to the generality of the model, it is obvious that the model is valid for other topologies discussed here, apart from H4. As a matter of fact, the same model has been used to analyse the common-mode behaviour of various transformer less converter topologies. However, since different topology has different V_{AN} and V_{BN} , the expressions for V_{CM} and V_{DM} will differ from one another, which yield different common-mode behaviour.

A. Galvanic Isolation

In transformerless PV inverters, the galvanic connection between the PV and the grid allows leakage current to flow. Hence, in topologies such as H5 and HERIC, galvanic isolation is provided to reduce the leakage current. The galvanic isolation can basically be categorized into dc-decoupling and ac-decoupling methods. For dc-decoupling method, dc-bypass switches are added on the dc side of the inverter to disconnect the PV arrays from the grid during the freewheeling period. However, the dc-bypass branch, which consists of switches or diodes, is included in the conduction path as shown in Fig. 3. For H6, output current flows through two switches and the two dc-bypass branches during the conduction period. Hence, the conduction losses increase due to the increased number of semiconductors in the conduction path. On the other hand, bypass branch can also be provided on the ac side of the inverter (i.e., ac-decoupling method) such as seen in HERIC. This ac-bypass branch functions as a freewheeling path which is completely isolated from the conduction path, as shown in Fig. 3. As a result, the output current flows through only two switches during the conduction period. Therefore, topologies employing ac-decoupling techniques are found to be higher in efficiency as compared to dc-decoupling topologies. One setback of galvanic isolation is that there is no way of controlling the CMV by PWM during the freewheeling period. Fig.4 shows operation modes of galvanic isolation which employs dc-decoupling method. As shown in Fig. 4(a), during the conduction period, S_1 and S_4 conduct to generate the desired output voltage. At the same time, V_A is directly connected to V_{DC} and V_B is connected to the negative terminal(N) of the dc-link. Hence, the CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \quad (7)$$

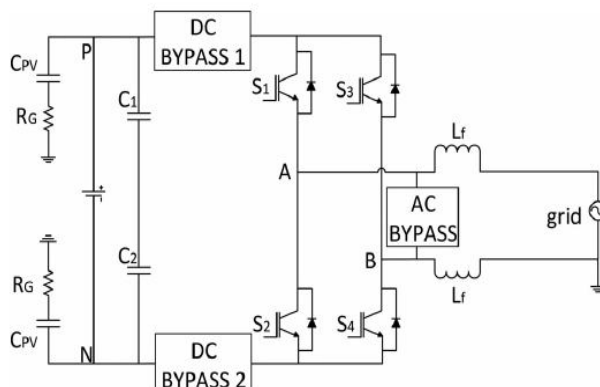


Fig.3. Universal transformerless topologies.

During the freewheeling period, the dc-bypass switches disconnect the dc-link from the grid. Therefore, point A and point B are isolated from the dc-link, and V_A and V_B are floating with respect to the dc-link as shown in Fig. 4(b).

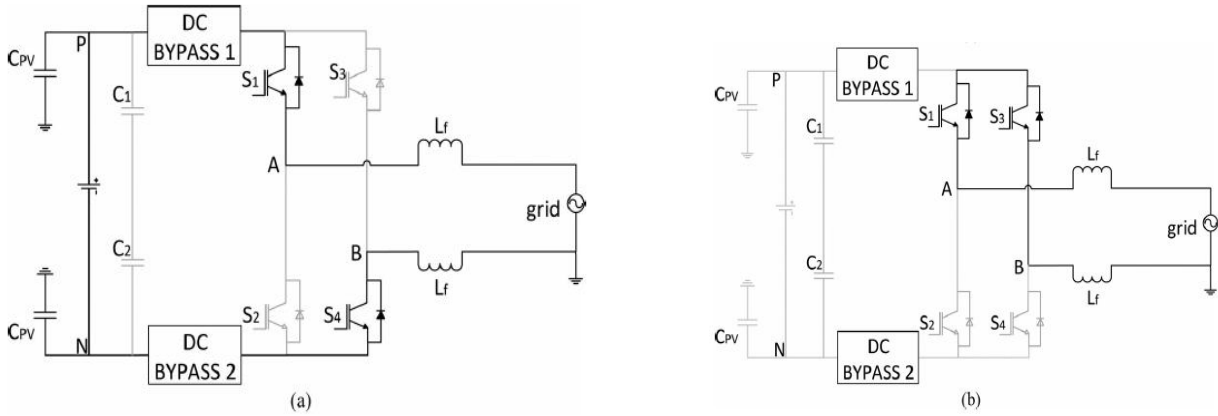


Fig. 4. Operation modes of dc-decoupling topology. (a) Conduction mode. (b) freewheeling mode.

III. HBZVR-D TOPOLOGY

A. Structure of HBZVR-D

Based on the analysis above, a simple modified HBZVR-D is presented to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. HBZVR-D is modified by adding a fast-recovery diode, D_6 , to the existing HBZVR as shown in Fig.5(a). The voltage divider is made up of C_1 and C_2 . S_1 – S_4 are the switches for full-bridge inverter. The antiparallel diodes, D_1 – D_4 , as well as S_5 provide a freewheeling path for the current to flow during the freewheeling period. Diodes D_5 and D_6 form the clamping branches of the freewheeling path.

Fig.5(b) illustrates the switching patterns of the HBZVR-D. Switches S_1 – S_4 commute at switching frequency to generate unipolar output voltage. S_5 commutates complementarily to S_1 – S_4 to create freewheeling path.

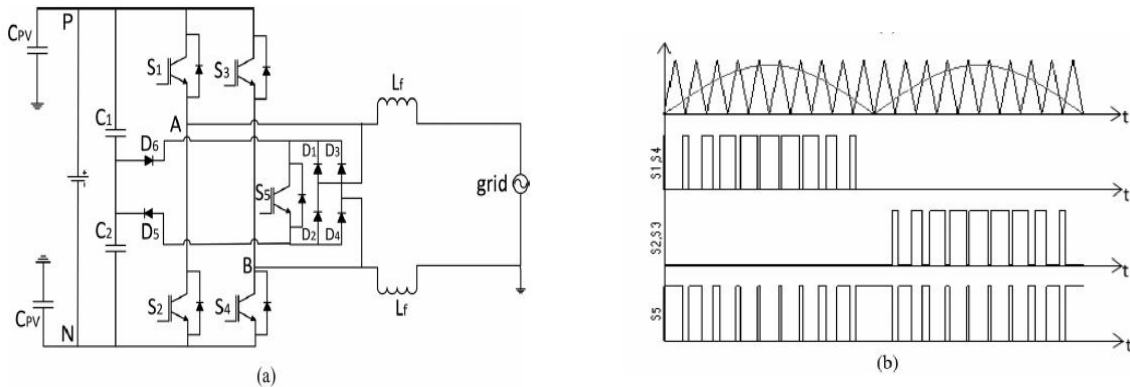


Fig. 5. Proposed HBZVR-D topology. (a) Converter structure. (b) Switching waveforms.

B. Operation Modes and Analysis

Mode I:

During this mode, S_1 and S_4 are ON while S_2 , S_3 and S_5 are OFF. Current increases and flows through S_1 and S_4 . $V_{AB} = +V_{DC}$. The CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \quad (8)$$

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

Mode II:

Here, S_1 – S_4 are OFF. S_5 is ON to create a freewheeling path. Current decreases and freewheels through diodes D_3 , D_2 , and the grid. The voltage V_{AN} decreases and V_{BN} increases until their values reach the common point, $V_{DC/2}$, such that $V_{AB} = 0$. The CMV is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2} \left(\frac{V_{DC}}{2} + \frac{V_{DC}}{2} \right) = \frac{V_{DC}}{2} \quad (9)$$

Mode III:

In this mode, S_2 and S_3 are ON, while S_1 , S_4 and S_5 are OFF. Current increases and flows through S_2 and S_3 . $V_{AB} = -V_{DC}$. The CMV become

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2} (0 + V_{DC}) = \frac{V_{DC}}{2} \quad (10)$$

Mode IV:

In this mode, S_1 – S_4 are OFF. S_5 is ON to create freewheeling path. Current decreases and freewheels through diodes D_1 , D_4 and the grid. The voltage V_{AN} decreases and V_{BN} increases until their values reach the common point $V_{DC/2}$, and $V_{AB} = 0$. The CMV is as derived in (10).

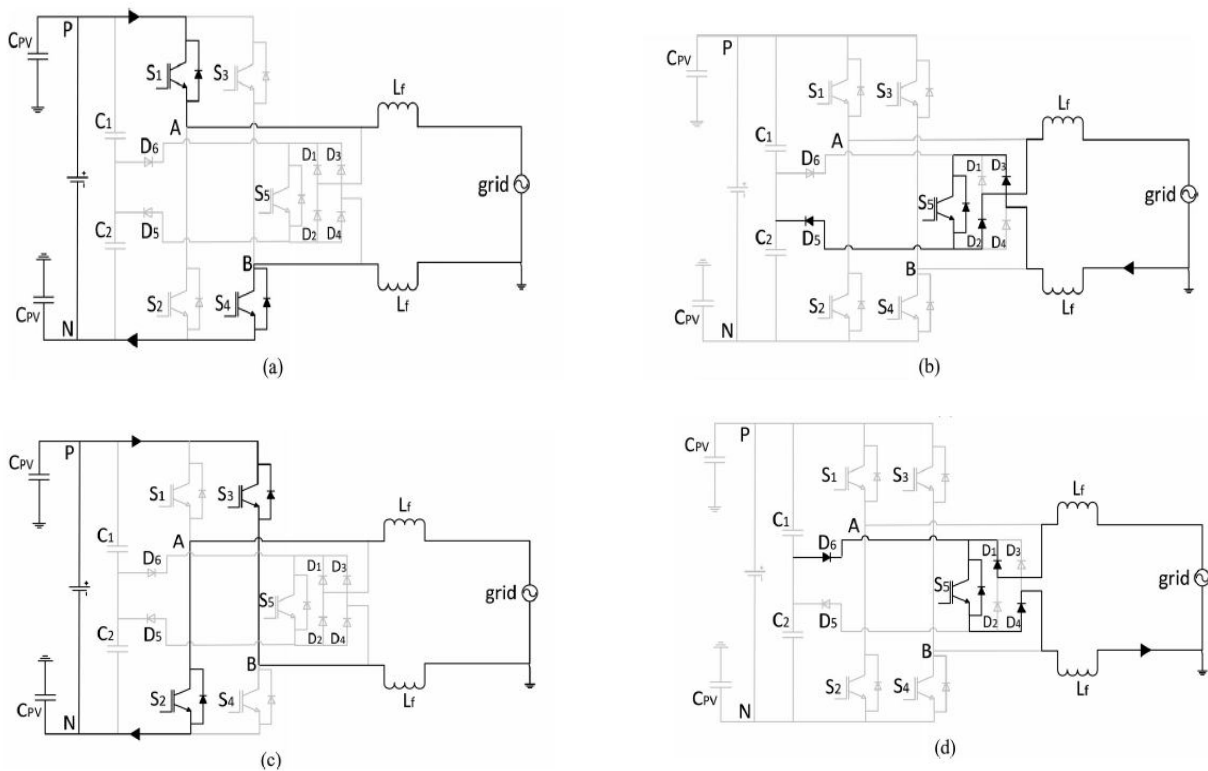


Fig. 6. Operation modes of HBZVR-D topology. (a) Mode I: conduction mode and (b) Mode II: freewheeling mode during positive half cycle. (c) Mode III: conduction mode and (d) Mode IV: freewheeling mode during negative half cycle.

Obviously, modulation techniques are designed to generate constant CMV in all four operation modes. All the research works are designed based on the principles above. Practically, V_{AN} and V_{BN} do not reach common point during the

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

freewheeling period (mode 2 and mode 4). During the freewheeling period, both V_{AN} and V_{BN} are not clamped to $V_{DC/2}$ and is oscillating with amplitude depending on the parasitic parameters and junctions' capacitance of those topologies. The improved clamping branch of HBZVR-D ensures the complete clamping of CMV to $V_{DC/2}$ during the freewheeling period. It is well noted that the output current flows through only two switches in every conduction period (mode 1 and mode 3) as shown in Fig.6 (a) and (c). This explains why HBZVR-D has relatively higher efficiency than those of dc-decoupling topologies.

IV.SIMULATION RESULTS

A.Output Performance and Common Mode Behaviour

The PV array is simulated with dc voltage source of 400V. The stray capacitance (C_{PV}) is modeled with two capacitors of 100 nF, each connected to the PV terminal and the ground. The ground resistance (R_G) is 11 Ω . The filter is made up of two inductors (L); each has a value of 3 mH. The grid line to neutral voltage is 230 V (rms) with frequency (f) of 50 Hz. This topology generates unipolar output voltage, which reduces the grid current ripples and filter inductor losses as addressed in bipolar modulation techniques. Hence, smaller filter inductors are required as compared to topologies with bipolar output.

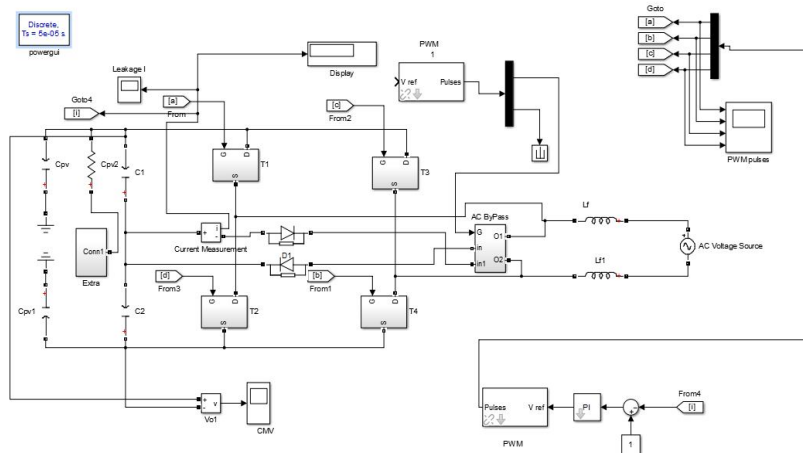


Fig. 7. Simulaion diagram of HBZVR-D topology.

Proposed HBZVR-D has improved the performance of the clamping branch as shown in Fig. 9. It gives the superior performance of clamping branch family.

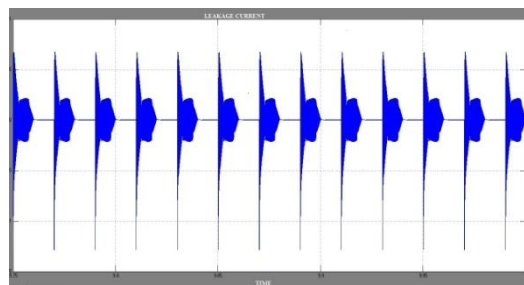


Fig.8. Leakage current of HBZVR-D topology



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 6, June 2015

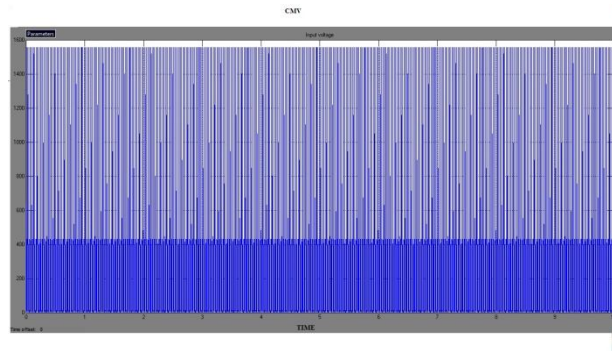


Fig. 9. CMV of HBZVR-D topology

V. CONCLUSION

Two strategies have been commonly used for reducing leakage current, galvanic isolation and CMV clamping. Based on the characteristic of the two strategies, performance of the different topologies can be evaluated. With the understanding on the merits and demerits of the different approaches, a modified HBZVR topology is obtained by addition of a fast-recovery diode. The new topology (known as HBZVR-D) combines the advantages of the low loss ac-decoupling method and the complete leakage current elimination. On comparing HBZVR and proposed topology, it is found that leakage current and CMV is slightly reduced.

TABLE.I
Performance Comparison of HBZVR & HBZVR-D

Topology	Leakage Current(A)	CMV(V)
HBZVR	1.33	semifloating
HBZVR-D	1.28	Constant

REFERENCES

- [1] G. Petrone et al., "Reliability issues in photovoltaic power processing systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2569–2580, Jul. 2008.
- [2] R. Gonzalez et al., "Transformerless single-phase multilevel photovoltaic inverter," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2694–2702, Jul. 2008.
- [3] T. Kerekes et al., "Evaluation of three-phase transformerless photovoltaic inverter topologies," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2202–2211, Sep. 2009.
- [4] S. V. Araujo, P. Zacharias, R. Mallwithz, "Highly efficient singlephase transformerless inverters for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 9, pp. 3118–3128, Sep. 2010.
- [5] O. Lopez et al., "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2010.
- [6] F. T. K. Suan, N. A. Rahim, H. W. Ping, "Modeling, analysis and control of various types of transformerless grid connected PV inverters," in *Proc. IEEE Clean Energy Technol.*, Jun. 2011, pp. 51–56.
- [7] J.M. Shen, H. L. Jou, J. C. Wu, "Novel transformerless grid connected power converter with negative grounding for photovoltaic generation system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1181–1829, Apr. 2012.