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Design of DC–AC Cascaded H-Bridge Multilevel Inverter for Hybrid Electric Vehicles Using SIMULINK/MATLAB

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ABSTRACT: The paper presents a Multilevel Boost Inverter for Hybrid vehicles employing Cascaded H Bridge topology for Hybrid electric vehicle applications. Current inverter systems make use of DC-DC boost converters to increase the battery voltage before converting it into AC signal for the inverter. The current traction drive inverters have low power density, are expensive, and have low efficiency as they need a bulky inductor. A multilevel boost inverter design implemented without the use of inductors is proposed in this paper. Conventionally, each H-bridge needs a dc power supply. The paper proposes a design using a standard three-leg inverter and an H-bridge in series with each inverter leg which uses a capacitor as the dc power source. Results show that the harmonic distortion reduces with multilevel inverters.

KEYWORDS: Multilevel Inverters Cascaded H Bridge Inverters. Hybrid Electric Vehicle (HEV**).**

I.INTRODUCTION

Recently, due to rise in oil prices and environmental pollution issues, hybrid electric vehicles (HEVs) and electric vehicles (EVs) are gaining increased attention due to lower emissions and better efficiencies obtained due to the advancement of power electronics [1-3]. An HEV usually combines a smaller internal combustion engine of a conventional vehicle with a battery pack and an electric motor to drive the vehicle.. An EV typically uses rechargeable batteries and an electric motor. The batteries need to be charged regularly.
Fig 1 shows the power train of HEVs, representing the role of DC-AC converter which provides necessary voltage for the traction drive system.

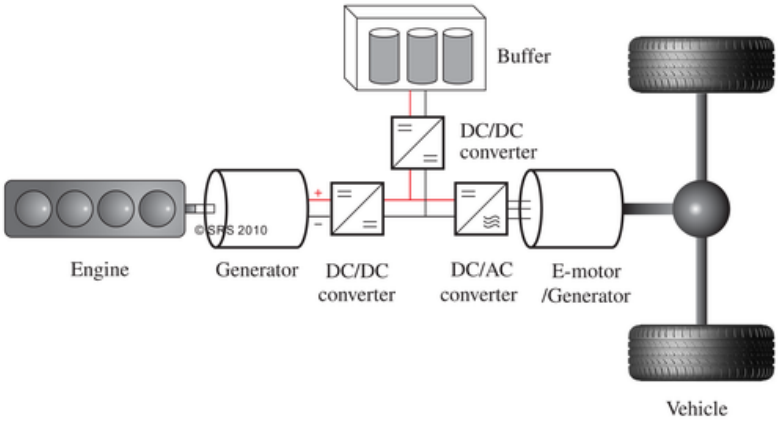

Fig 1. Power train of a Hybrid Electric Vehicle.

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As shown in fig 1 the traction is driven either through electric motor or a combustion engine. The electric motor derives its supply from the DC-AC converter. This converter converts the high voltage DC voltage into AC voltgage to drive the Motor. This motor works in generator mode during regenerative braking. The Buffer(Battery or supercapacitors or fuel cells etc) is increased with the help of a boost DC-DC converter. This can be eliminated with application of cascaded H bridge concept.

II MULTILEVEL INVERTERS

Recently, industry has begun to demand higher power equipment, reaching a range of megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Hence it becomes difficult to connect a single power semiconductor switch directly to medium voltage grids (kV). For these reasons, a new family of multilevel inverters provide a better solution for working with higher voltage levels [7].Multilevel inverters typically include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Due to commutation of the switches, the addition of the capacitor voltages is possible, which produces high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 2 shows a schematic diagram of one phase leg of inverters with different numbers of levels, where the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values i.e., levels with respect to the negative terminal of the capacitor [see Fig. 2(a)], while the three-level inverter generates three voltages, and so on.
If *m* is number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load is

$$k = 2m+1 \qquad (1)$$

As the conventional two or three levels inverter cannot completely eliminate the unwanted harmonics in the output signal. Hence, using the multilevel inverter can serve as a better alternative to conventional PWM inverters. Here in this topology, each bridge needs a separate dc link capacitor and the voltage across the capacitor may be different. Thus, each power circuit needs just one dc source voltage. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H-bridge cell may have positive, negative or zero voltage. The resulting output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd always. The term multilevel comes from the three-level inverter introduced by Nabae *et al.* By increasing the number of levels in the inverter, the output voltages with more steps can be produced generating a staircase waveform, having reduced harmonic distortion. But, increasing number of levels increases the control complexity and introduces voltage imbalance problems.

Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped), capacitor-Clamped (flying capacitors) and cascaded multicell with separate dc sources.

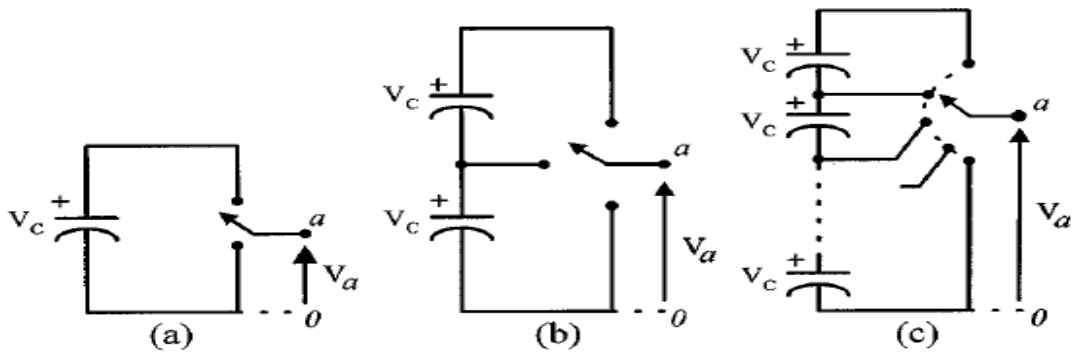

Fig 2. Single phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

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III. WORKING PRINCIPLE OF INDUCTORLESS CASCADED H-BRIDGE MULTILEVEL BOOST INVERTER

The typical inductorless DC-AC cascaded H-bridge multilevel boost inverter is shown in Fig. 2. The inverter uses a standard 3-leg inverter (for each phase) and an H-bridge considering a capacitor as its DC source in series with each phase leg.

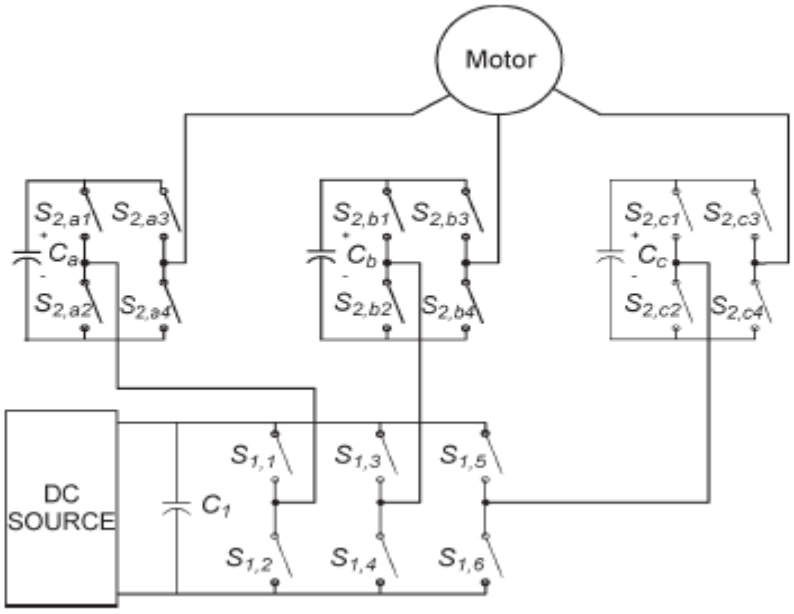

Fig 3. Topology of the proposed dc–ac cascaded H-bridge multilevel boost inverter.

To understand the working of the circuit, a simple single phase circuit is shown in Fig. 4. The output voltage V1 of this leg of the bottom inverter (with respect to the ground) is either +Vdc/2 (when S5 is closed) or −Vdc/2 (when S6 is closed). This is further connected in series with a full H-bridge which in turn is supplied by a capacitor voltage. If the capacitor is kept charged to Vdc/2, then the output voltage of the H-bridge can have the values +Vdc/2(when S1, S4 are closed), 0 (S1, S2 closed or S3, S4 closed), or −Vdc/2 (S2, S3 closed). An example output waveform that this topology can achieve is shown in Fig. 5(a). When the output voltage v = v1 + v2 is required to be zero, one can either set V1 = +Vdc/2 and V2 = −Vdc/2 or V1 = −Vdc/2 and V2 = +Vdc/2.

Further capacitor's voltage regulation control detail is illustrated in Fig. 5. During $\theta_1 \leq \theta \leq \pi$, the output voltage in Fig. 5(a) is zero and the current i > 0. If S1, S4 are closed (so that V2 = +Vdc/2) along with S6 closed (so that V1 = −Vdc/2), then the capacitor is discharging (ic = −i < 0 see Fig. 5(b)) and V = V1 + V2 = 0. On the other hand, if S2, S3 are closed (so that V2 = −Vdc/2) and S5 is also closed (so that V1 = +Vdc/2), then the Capacitor is charging (ic = i > 0 see Fig. 5(c)) and V = V1+V2 = 0. The case i < 0 is accomplished by simply reversing the switch positions of the i > 0 case for charging and discharging of the capacitor. Consequently, the method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output, either the switches S1, S4, and S6 are closed or the switches S2, S3, S5 are closed depending on whether it is necessary to charge or discharge the capacitor. Therefore, it is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage.

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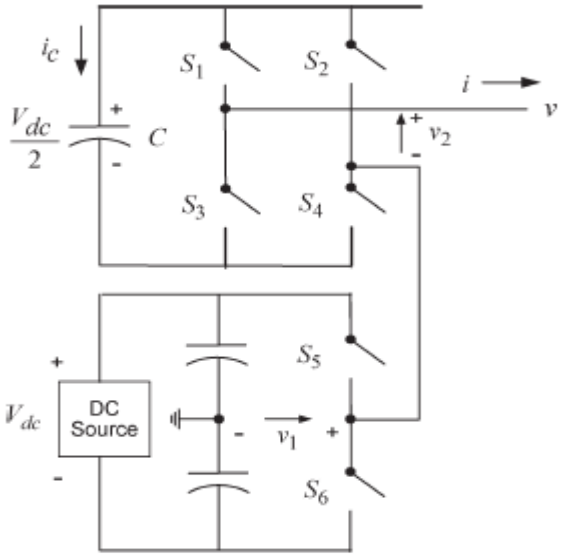

Fig 4. Single phase of the proposed dc–ac cascaded H-bridge multilevel boost inverter

The goal of using fundamental frequency switching modulation control is to output a five-level voltage waveform, with a sinusoidal load current waveform, as shown in Fig. 5(a). If the capacitor's voltage is higher than $V_{dc}/2$, switches S_5 and S_6 are controlled to output voltage waveform V1, and the switches S1, S2, S3, and S4 are controlled to output voltage waveform V2, shown in Fig. 5(b). The highlighted part of the waveform in Fig. 5(b) is the capacitor discharging period, during which the inverter's output voltage is 0 V.

If the capacitor's voltage is lower than Vdc/2, the switches S5 and S6 are controlled to output voltage waveform v1, and switches S1, S2, S3, and S4 are controlled to output voltage waveform v2, shown in Fig. 5(c). The highlighted part of the waveform in Fig. 5(c) is the capacitor charging period, when the inverter's output voltage is 0 V. Therefore, the capacitors' voltage can be regulated by alternating the capacitor's charging and discharging control, when the inverter output is 0 V.

This method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current. In other words, the highest output ac voltage of the inverter depends on the displacement power factor of the load.

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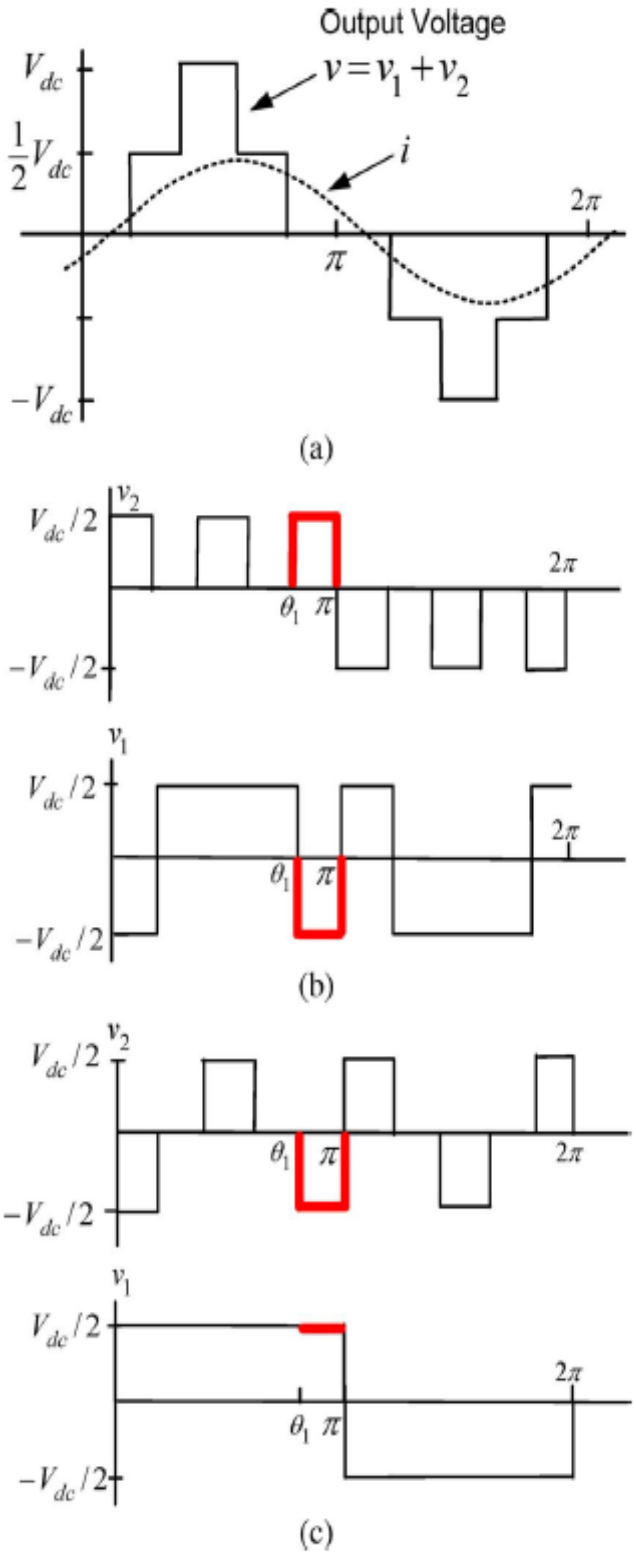

Fig 5. Capacitor voltage regulation with capacitor charging and discharging. (a) Overall output voltage and load current. (b) Capacitor discharging. (c) Capacitor charging.

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III. SWITCHING CONTROL OF CASCADED H-BRIDGE MULTILEVEL BOOST INVERTER WITHOUT INDUCTORS

We have different kinds of modulation control methods such as traditional sinusoidal pulsewidth modulation (SPWM), space vector PWM, harmonic optimization or selective harmonic elimination, and active harmonic elimination, and all of these can be used for inverter modulation control. For the proposed dc–ac boost inverter control, a practical modulation control method is the fundamental frequency switching control for high output voltage and SPWM control for low output voltage, which only uses the bottom inverter. In this simulation level shift technique is used for pulse generation.

IV. OUTPUT VOLTAGE BOOST

As previously mentioned, the cascaded H-bridge multilevel inverter can output a boosted AC voltage to increase the output power, and the output AC voltage depends on the displacement power factor of the load. Here, the relationship of boosted AC voltage and the displacement power factor is discussed.
It is assumed that the load current displacement angle is ϕ as shown in Fig. 5. To balance the capacitor voltage, the pure capacitor charging amount needs to be greater than the pure discharging amount. That is, to regulate the capacitor's voltage with fundamental frequency switching scheme, the following equation must be satisfied,

$$\int Icharging\, d\theta + \int Idischarging\, d\theta > 0$$

V. MATLAB SIMULATION AND RESULTS

A five level DC to AC cascaded H bridge Mutilevel Inverter has been implemented through simulink model and the relevant output waveforms for three phase are as shown

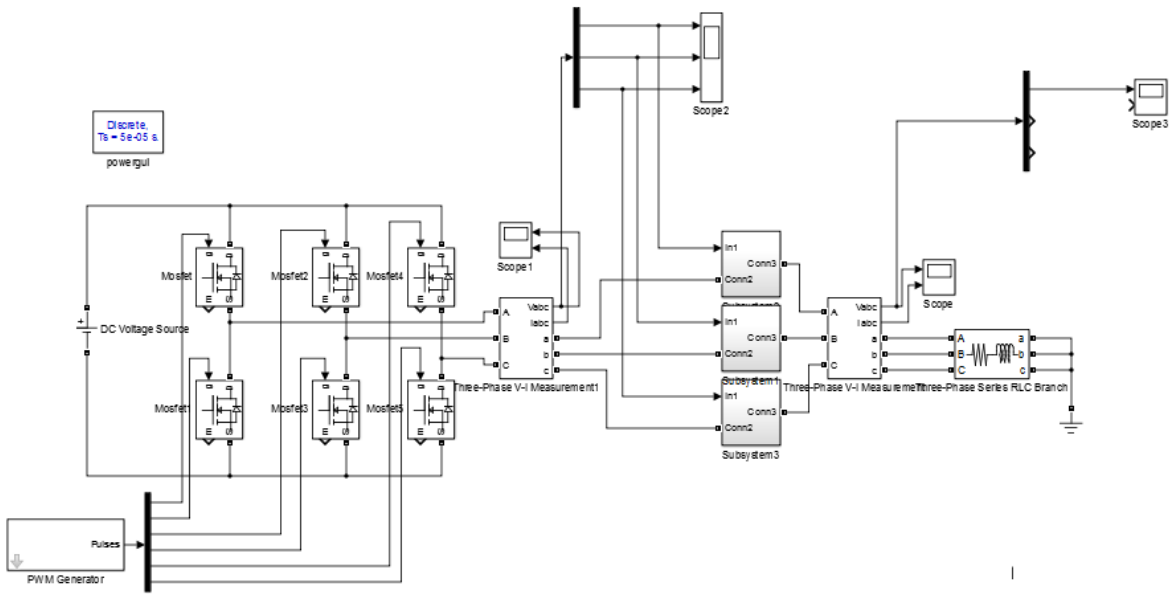

Fig 6. Simulink model of three phase cascaded H bridge multilevel Inverter.

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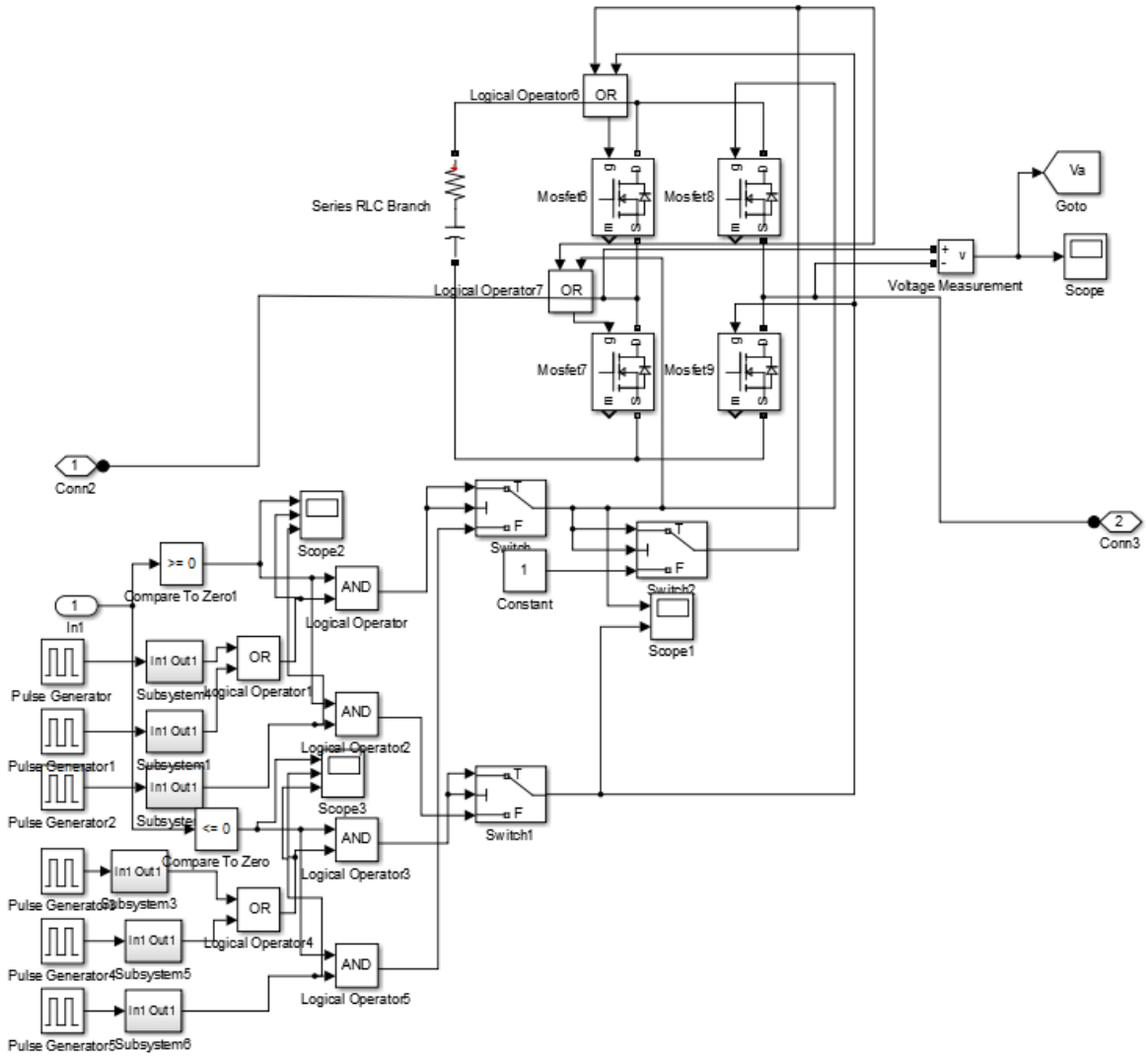

Fig 7. Subsytem showing H bridge for one of the phases

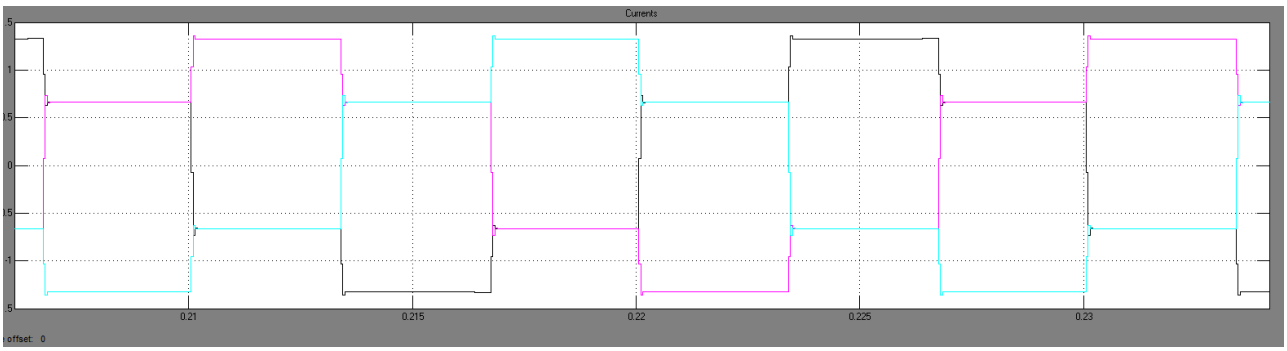

Fig 9. Output current

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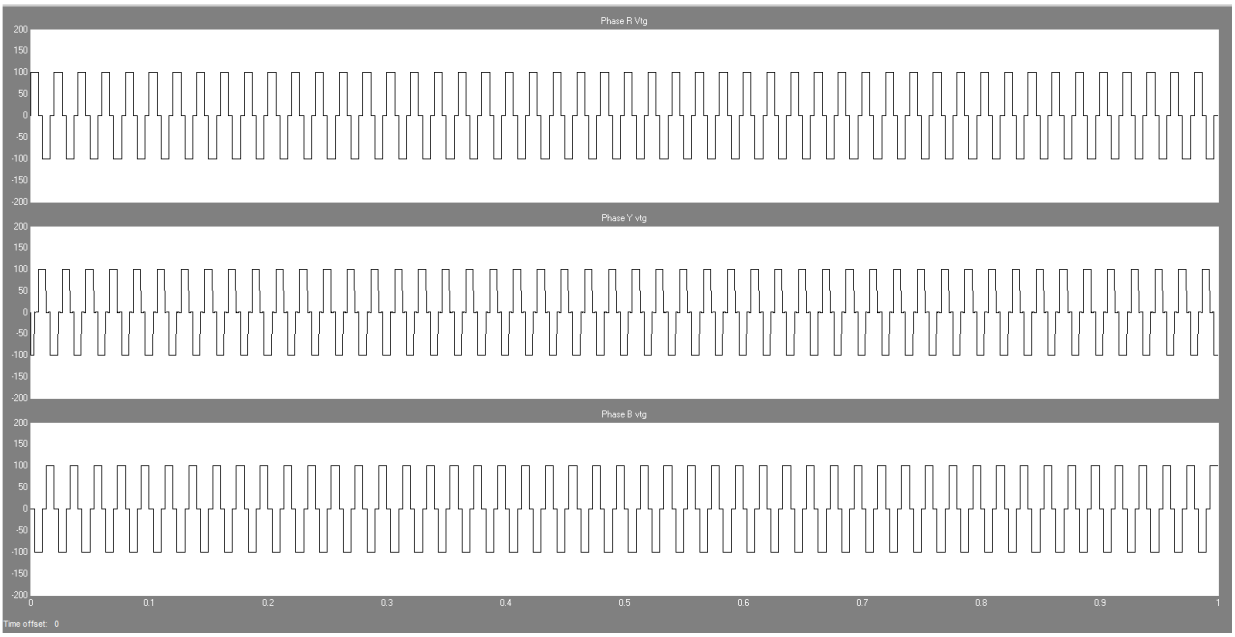

Fig 8. Output Voltage

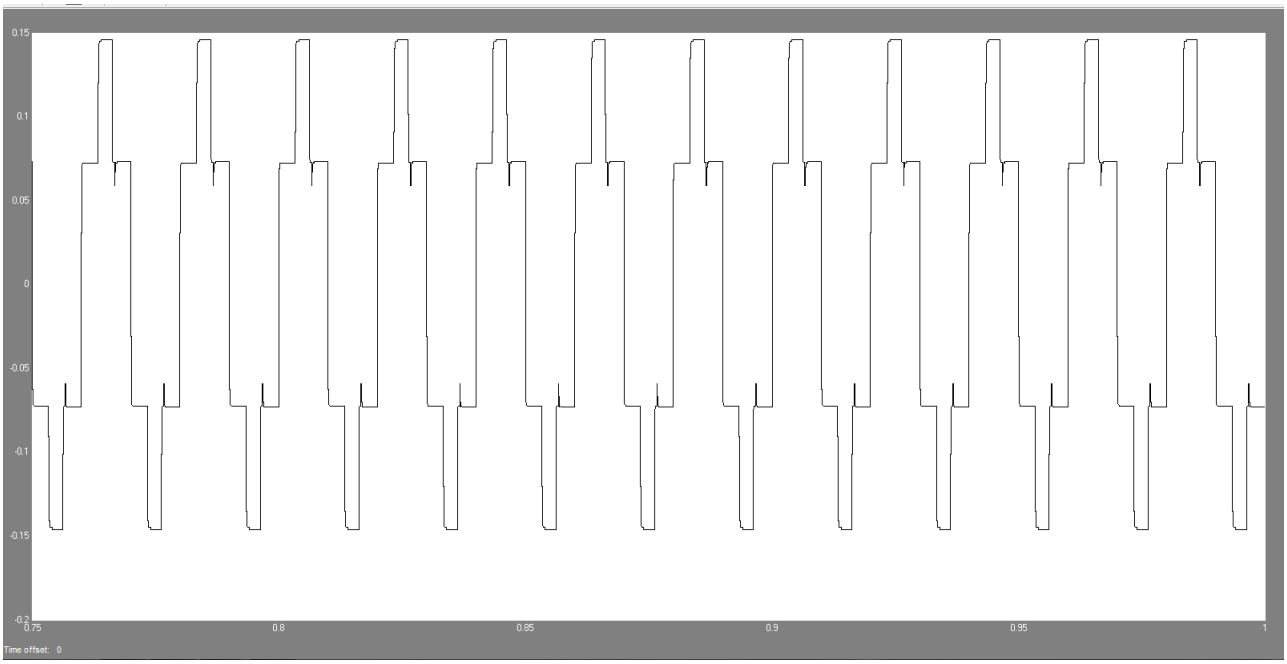

Fig 10. Output of H bridge for one of the phases.

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VI. THD ANALYSIS

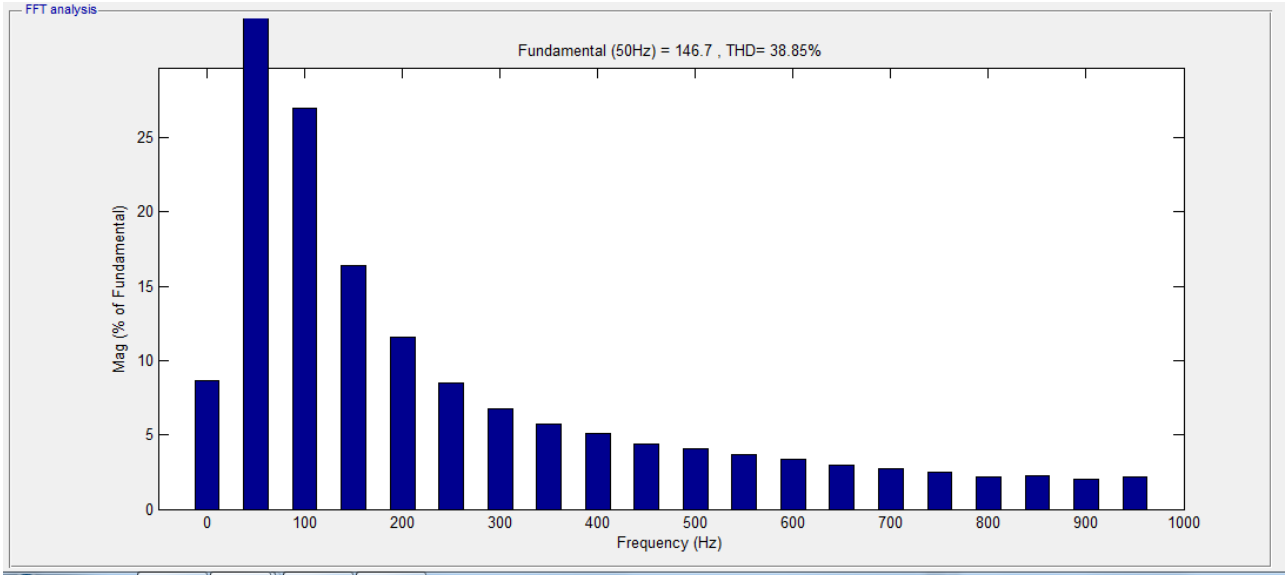

Fig 11. FFT ananlysis of line current without multilevel application

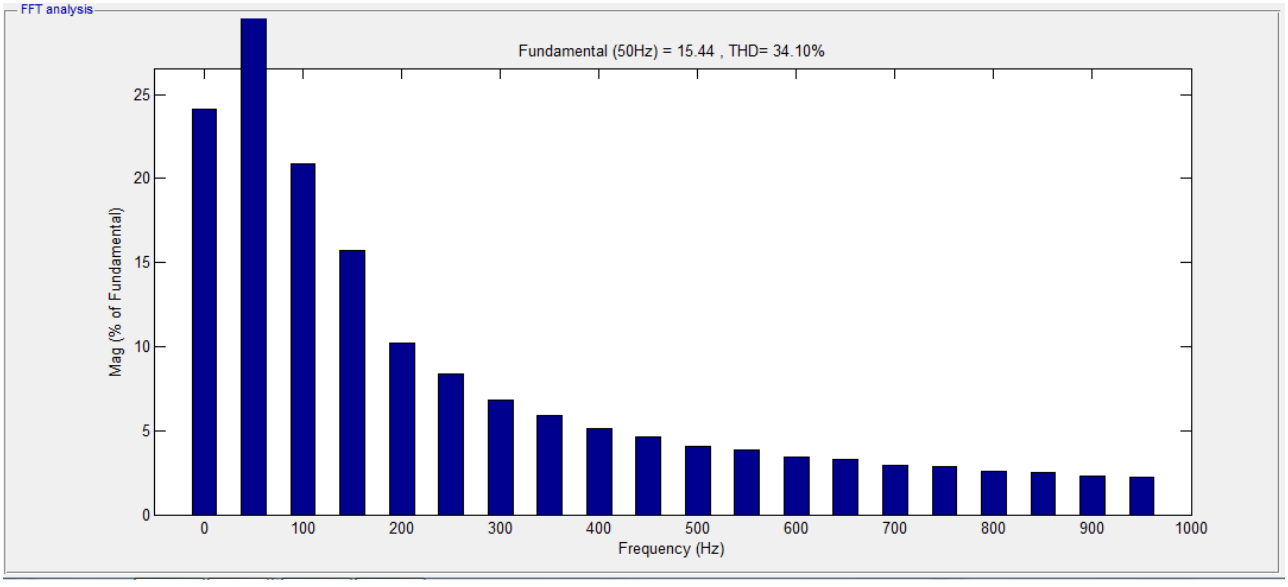

Fig 12. FFT ananlysis of line current for multilevel (3 level) inverter circuit

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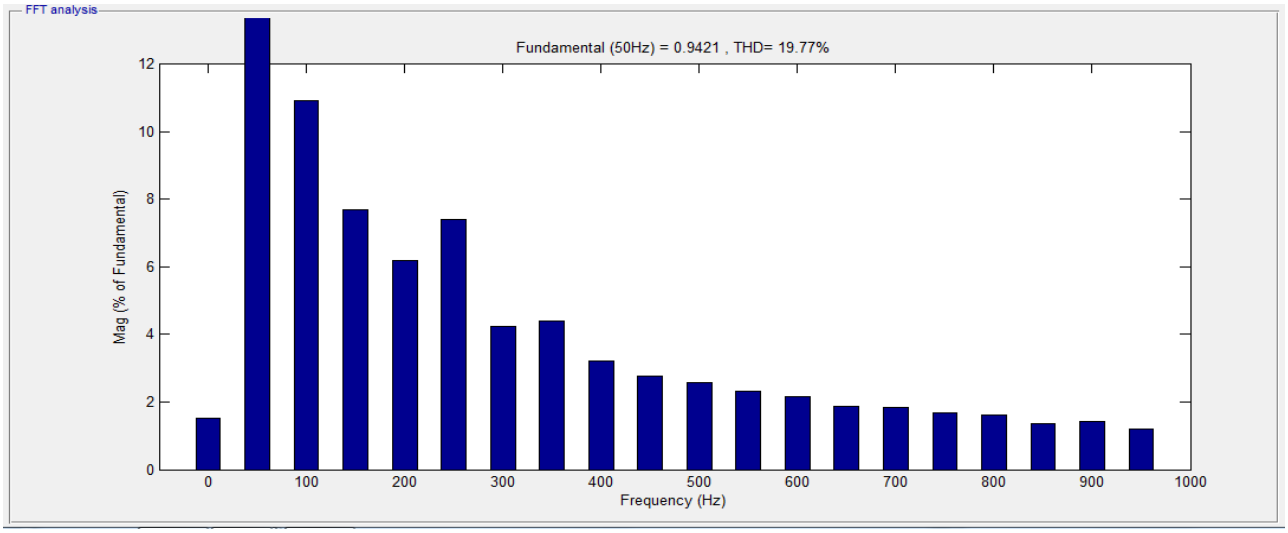

Fig 13. FFT ananlysis of line current for multilevel (5 level) inverter circuit

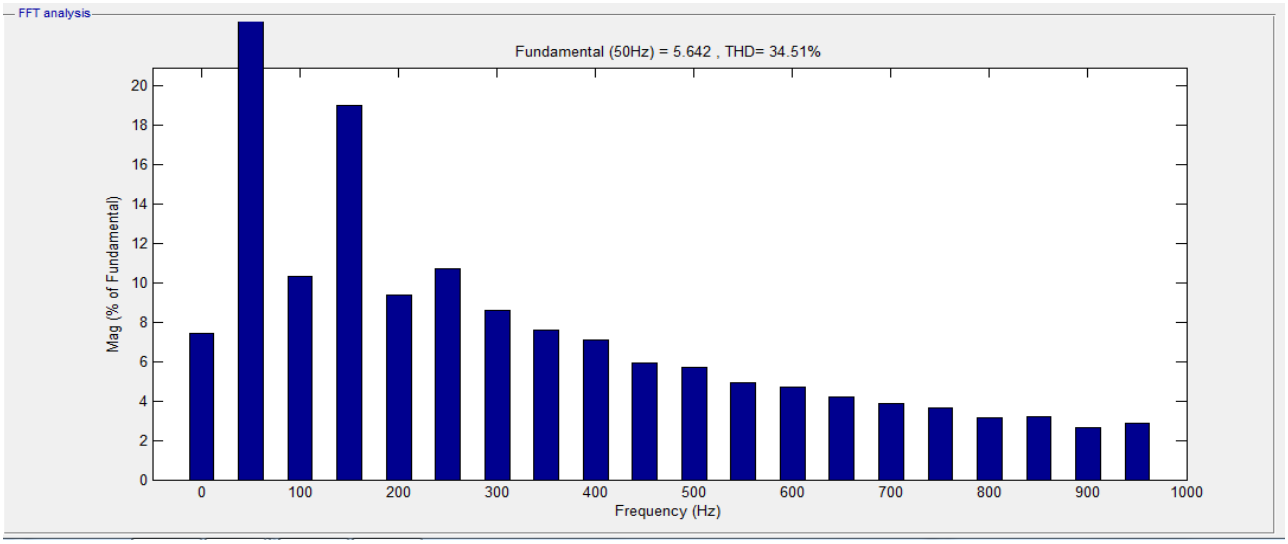

Fig 14. FFT ananlysis of line current for multilevel (7 level) inverter circuit

Results Anaylsis:

Levels	**THD%**
Traditional Inverter	38.85
7 level	34.57
5 level(Cascaded H Bridge)	**19.77**
3 level	34.10

Table 1 Comparison of %THD for different types.

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VII.CONCLUSION

DC- AC cascaded H bridge multilevel inverter has been implemented using matlab/simulink and tested for five level output. The application of multilevel concept reduces the harmonic distortion and produces a near sinusoidal waveform as shown in table 1.The application of cascaded H bridge results in further reduction of THD as shown in table. The application of this DC-AC boost inverter on HEV and EV applications removes the need of the bulky inductor present in DC-DC boost converter. Hence reducing magnetization losses and weight of the converter.

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BIOGRAPHY

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