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Design and Simulation of Low Noise Amplifier at 2.3 GHz Frequency for 4G Technology

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ABSTRACT*:* There has been a tremendous increase in the use of mobile phones in our day to day life. The quality of a communication system is mainly influenced by the sensitivity of the receiver. Requirements of Cellular Network application are limited power and moderate performance has forced the Wireless Cellular Network transceiver designers toward an adaptive transceiver structures. It has been studied that in INDIA 2.3 GHz frequency in TD-LTE Band 40 defined by International Telecommunication Union Radio-Communication Sector (ITU-R) is being used [5]. Looking at the receiver system of the cellular system it is found that a crucial receiver stage is having Low Noise Amplifier (LNA) as the first block after the antenna that should have a low Noise Figure (NF) as well as sufficient gain to provide high sensitivity. The designed Low Noise Amplifier gives 17.0787 dB gain and 0.7334 dB Noise Figure at 2.3 GHz Frequency. The simulation results are carried out by Advanced Design System.

KEYWORDS: 4G Technology, ADS Software, Gain, Low Noise Amplifier (LNA), Noise Figure (NF) and RF Front End.

I. INTRODUCTION

The trend and revolution of communication technology is increasing day by day, particularly in wireless communication. There has been a tremendous upgradation in the generation of communication. There are in total 43 LTE frequency bands, out of which the band 40 is designated as TD 2300 having frequency from 2.3 GHz to 2.4 GHz with center frequency 2.350 GHz and a bandwidth of 100 MHz, which is being used by the telecom industries of India to provide 4G services to the users [1]. As Indian Telecom industries provides 4G services at 2.3 GHz Frequency. LNA represent a basic building block of modern communication systems; it constitutes a part of a RF Front-End module as shown in Figure 1 and a key block in a receiver section. Noise Figure and Gain are the important parameters of the LNA which improves the sensitivity of the overall receiving system and hence the quality of service [5]. The LNA consists of main three stages: The Input Matching Network (IMN), the transistor and the Output Matching Network (OMN) [2] as shown in the Figure 2.

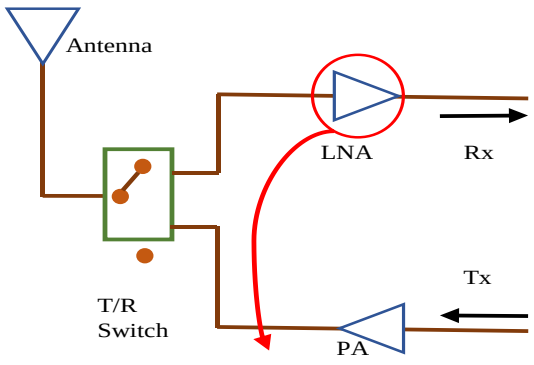

Figure 1: RF Front End

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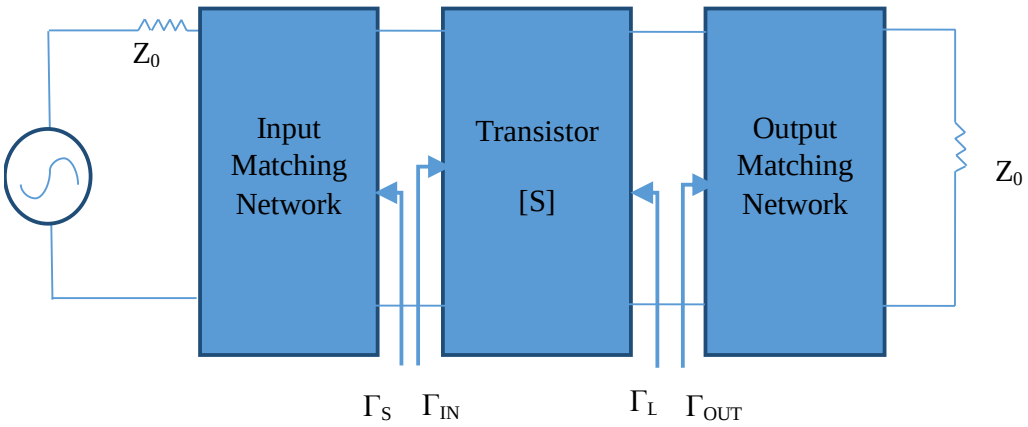

Figure 2: LNA Schematics

II. LITERATURE REVIEW

Table 1: Literature Review

Sr No.	Paper Title	Conclusion	References
1	Design Methodology of a Low Noise Amplifier for Wireless Communication	From this paper the systematic procedure for design methodology of LNA has been devised.	[3]
2	Design of a Front End Low Noise Amplifier for Wireless Devices	From this paper general topology of LNA is well understood as well as LNA is designed for 5 GHz to 6 GHz frequency having NF of 0.630 dB and Gain of 11.112 dB	[2]
3	Design of a 2.3GHz Low Noise Amplifier for WIMAX Application	In this paper the author has designed a LNA at 2.3 GHz frequency having NF of 1.102dB and Gain of 15.11dB	[4]

Table 1 shows the Literature review of Reference papers. Going through some related reference papers, Design methodology of LNA can be understood.

III. DESIGN FLOW OF LNA

The designing of the LNA is followed by various steps as shown in Figure 3 which represents the flow chart for designing the Low Noise Amplifier.

A. Step 1: Selection of a Transistor

Selection of the transistor is the crucial stage in LNA design. Each transistor has its maximum available gain (MAG) and minimum intrinsic noise figure (NF_{min}) at particular frequency. So a LNA which gives more gain than MAG and Noise figure less than NFmin cannot be designed. ATF-34143 transistor [8] is selected for LNA design as it is having values as per our targeted values.

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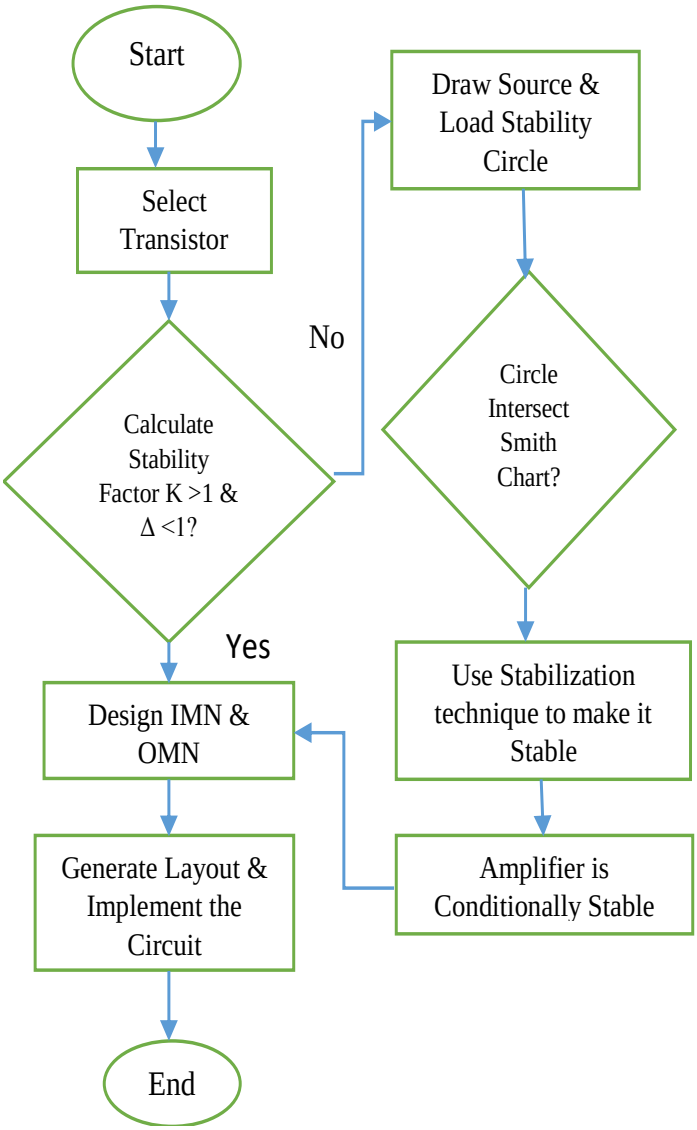

Figure 3: Flow Chart for LNA Design

B. Step 2: Stability Factor

There are different categories to know about the stability of the transistor.
K< 1 and Δ <1 → potentially stable system
K >1 and Δ <1 → unconditionally stable system.
For calculating the values of K and Δ the following equation [6] is used.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} [1]$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} [2]$$

Depending on the values of S-Parameter as shown in the Table 2, the values of K= 0.49 as shown in the Figure 4 obtained using ADS software and Δ = 0.36058. This shows that the value of K < 1 and Δ < 1, this results in potential unstable transistor.

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Table 2: S parameters at 2.3 GHz

Parameters	Values
S_{11}	0.7360 ∟-137.40°
S_{12}	0.0958 ∟017.60°
S_{21}	5.5870 ∟081.00°
S_{22}	0.2540 ∟-141.00°

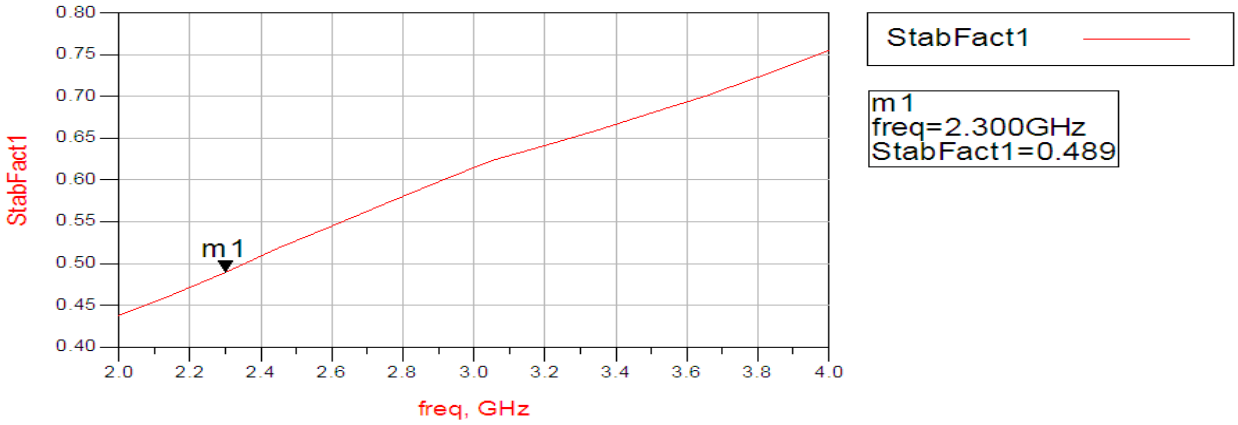

Figure 4: Plot of Stability Factor vs. Frequency

C. Step 3: Stability Circles

In order to plot the stability circle it is required to calculate the value of r_S and C_S for the input stability circle and for the output stability circle. It is required to calculate the value of r_L and C_L [6, 7].

$$r_S = \frac{|S_{12}S_{21}|}{||S_{11}|^2-|\Delta|^2|} \quad [3]$$

$$C_S = \frac{(S_{11}-S_{22}^{*}\,\Delta)^{*}}{|S_{11}|^2-|\Delta|^2} \quad [4]$$

$$r_L = \frac{|S_{12}S_{21}|}{||S_{22}|^2-|\Delta|^2|} \quad [5]$$

$$C_L = \frac{(S_{22}-S_{11}^{*}\,\Delta)^{*}}{|S_{22}|^2-|\Delta|^2} \quad [6]$$

Table 3: Values of radius and Center for obtainingInput-Output Stability Circles

Parameters	Values
r_s	1.300
C_s	1.968 ∟134.61°
r_L	8.1638
C_L	4.89 ∟-14.47°

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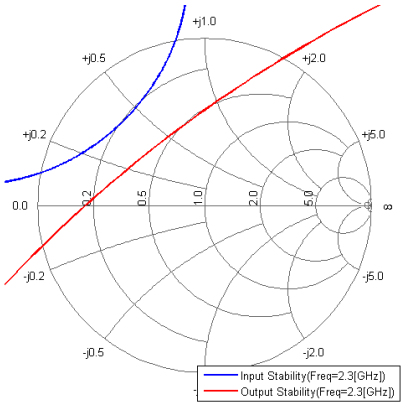

Figure 5: Graph of input and output stability circle

By using the values of radius and center as listed in Table 3, Figure 5 is drawn using ADS software where the blue arc represents the input stability circle and the red arc represents the output stability circle at 2.3 GHz frequency which proves that the transistor is potentially stable system. It is required that the input and output stability circle should not intersects the smith chart for the transistor to be unconditionally stable system.

D. Step 4: Stabilization Technique

In this we have used a resistive loading technique to make the transistor stable. It can be achieved by inserting a series or parallel resistor connected either to its input or output terminal. If the resistor is added in series at the input side, it would increase the NF and may affect the overall performance. Therefore, it is better to connect at output side of the transistor for enhancing the stability. The impedance circle that is tangent to the input stability circle is used to determine the value of input series resistance. Similar procedure is used for the output stability.
Shunt connection of 51.7097 Ω resistor at output side is done to gain Stability as shown in the Figure 6. As a result of the addition of the resistor there is the change in the S-Parameter values of the system as well as in the values of K and Δ.
The value of K =1.465 > 1 and Δ = 0.3001 < 1, this results in unconditionally stable transistor.

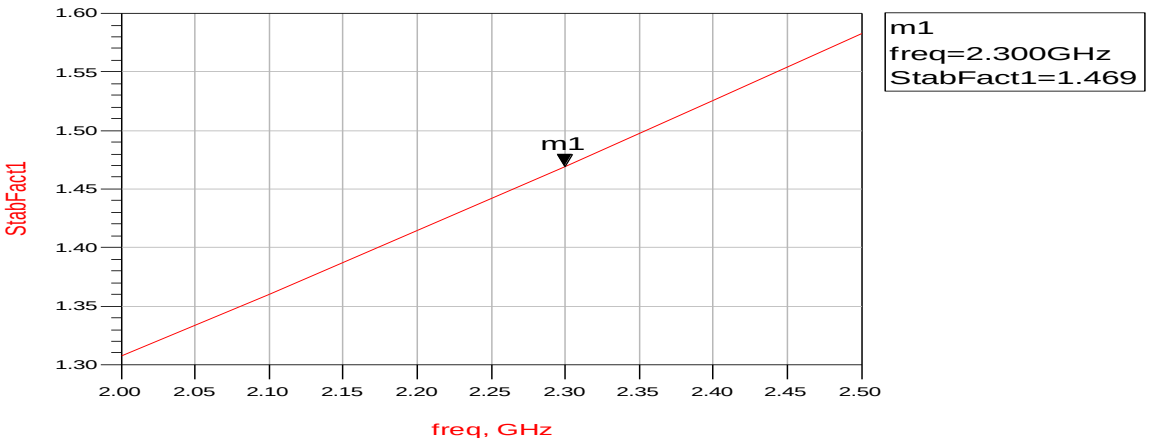

Figure 6: Graph of Stability Factor vs. Frequency obtained after Stabilization

Figure 6 represents the value of stability factor obtained after connecting the resistor in shunt at the output side of the transistor. The value of K is greater than one and value of Δ less than one. Also the input and the output stability circles are not intersecting the smith chart concluding that the system is now unconditionally stable system.

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E. Step 5: Available Gain and NF Circles

In order to design the IMN and OMN it is required to select appropriate Γ_S for which it is required to draw the Available Gain circles and the Noise Figure circles. Equations for drawing Gain and NF Circles [7] are as follows and there values are shown in Table 4 & 5 respectively. In these we have plotted available gain circles with varying gains from 15 dB to 18 dB and NF circles with varying noise figure value from 0.6 dB to 0.9 dB as shown in Figure 7.

$$C_a = \frac{g_a C_1^*}{1+g_a(|S_{11}|^2-|\Delta|^2)} \quad [7]$$

$$\text{Where } C_1 = S_{11} - \Delta S_{22^*} \quad [8]$$

$$r_a = \frac{\left|1-2K|S_{12}S_{21}|g_a+|S_{12}S_{21}|^2 g_a 2\right|^1/2}{|1+g_a(S_{11}2-|\Delta|^2)|} [9]$$

$$C_{Fi} = \frac{\Gamma_{opt}}{1+N} [10]$$

$$\text{Where, } N = \frac{F-F_{min}}{4R_N/z_0}\left|1+\Gamma_{opt}\right|^2 [11]$$

$$r_{Fi} = \frac{1}{1+N}\sqrt{N^2+N\left(1-\left|\Gamma_{opt}\right|^2\right)} [12]$$

Table 4: Available Gain circles Center and Radius

Available Gain Circle (dB)	Center	Radius
15	1.825∟151.402°	0.14677
16	1.845∟151.400°	0.14470
17	1.862∟151.398°	0.16055
18	1.878∟151.401°	0.17390

Table 5: Noise Figure Circles Center and Radius

Noise Circle (Fi) dB	N	Center	Radius
0.6	0.5888	0.4270∟74.000°	0.5126
0.7	1.1776	0.3120∟74.002°	0.6526
0.8	1.7664	0.2452∟73.940°	0.7292
0.9	2.3552	0.2000∟74.003°	0.7779

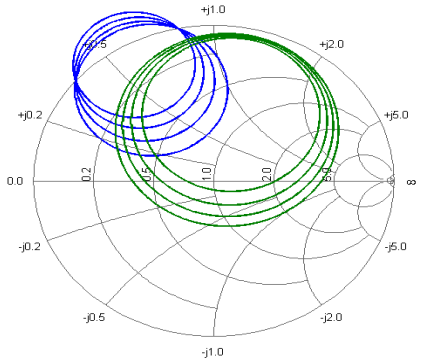

Figure 7: Graph of Available Gain and NF circles

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F. Step 6: Selection of Γ_S

The noise figure of the device is 0.55 dB and after adding the resistor for the stability, it increase the NF is about 0.6 dB. Keeping the 0.1 dB margin, we have plotted the noise figure circle for 0.7 dB on the Smith chart. Also, we have drawn few available gain circles with varying gains and intersecting with the 0.7 dB noise figure circle. We found the maximum available gain as 17 dB for the 0.7 dB noise figure. Figure 8 depicts the available gain circle and noise figure circle on the Smith chart. The intersection region of the two circles gives the stable region and one can select a source reflection coefficient from the region. The value of selected from the region is 0.5962 ∠ 143.2°

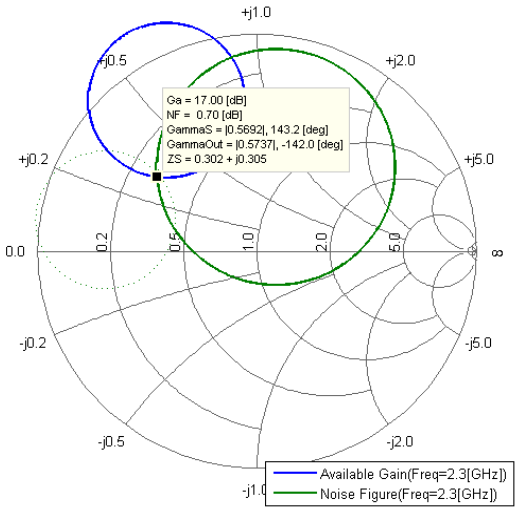

Figure 8: Smith Chart representing value of Γ_S and NF

G. Step 7: Matching Networks

Impedance matching is needed to provide maximum power transfer between the source or RF energy and its load. Otherwise reflected power from the load side will distrub the overall performance of the receiver. The maximum power is delivered to the load when the impedance of the load is equal to the complex conjugate of the impedance of the source [6]. The input matching network is designed to transform the input impedance of 50 Ω to the source impedance and the output matching network is designed to transform the load impedance to 50 Ω termination. It can be designed using a LC matching network, stub and quarter wave transform. Among of these we have selected LC matching because it is easy to implement as only two components are required. The Input Matching Network are designed to transforms the impedance from 0.395 + 0.1479j Ω to 50 Ω at 2.3 GHz operating frequency.Conceptually one can start the process by looking at the impedance 0.12645-0.143j Ω and back through the matching network to reach 50 Ω impedance. One needs to travel along the constant resistance circle and then along the circle of constant conductance to obtain the series inductor and the shunt capacitor, respectively.

Reflection coefficient of the output matching network is simulated and the result is shown in Figure 9 for a frequency range from 0 to 4.6 GHz. It can be observed from the plot in Figure 10 that the value of input reflection coefficient is zero at 2.3 GHz frequency, indicating a perfect match with sourrce impedance. The same procedure will apply for output matching network. The arrangement for the output matching network is shown in Figure 11. In Figure 12, plotting of an output reflection coefficient for a frequency range from 0 to 4.6 GHz has been done. It shows output reflection coefficient is zero at 2.3 GHz frequency. Input matching network consisting a series capacitor of 1.499642 pF and parallel inductor of 2.54505 nH and output matching network consisting a parallel capacitor of 2.38358 pF and series inductor 812.227 pH has been obtained.

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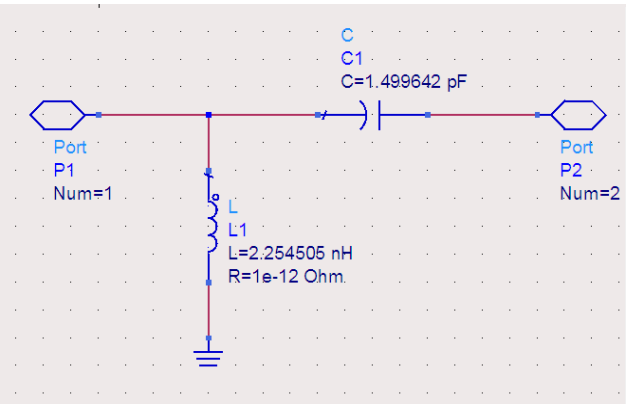

Figure 9: Input Matching Network

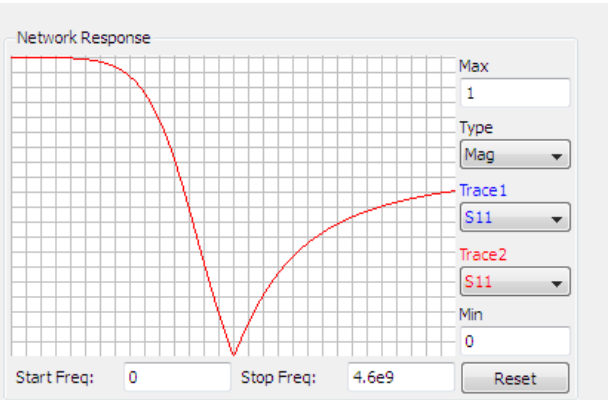

Figure 10: Network response after adding L and C for IMN

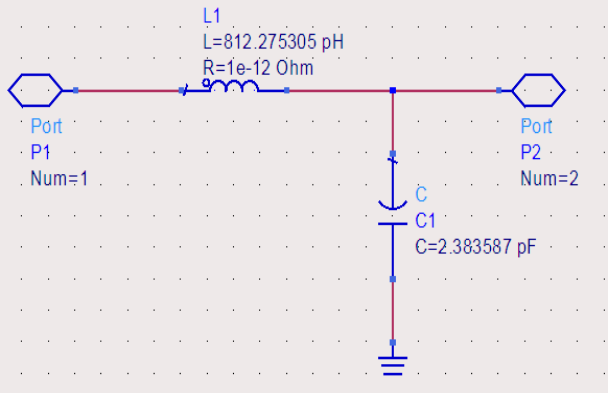

Figure 11: Output Matching Network

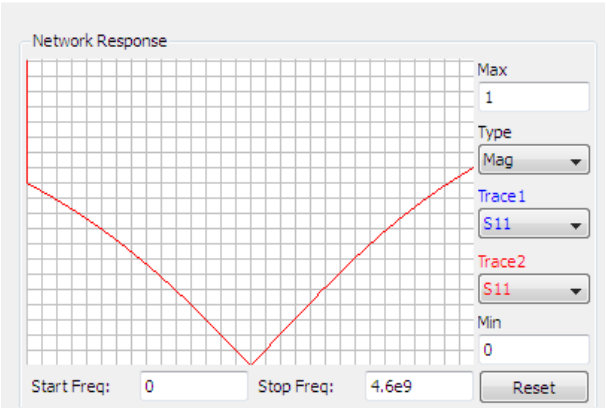

Figure 12: Network Response after adding L and C for OMN

IV. RESULTS AND DISCUSSION

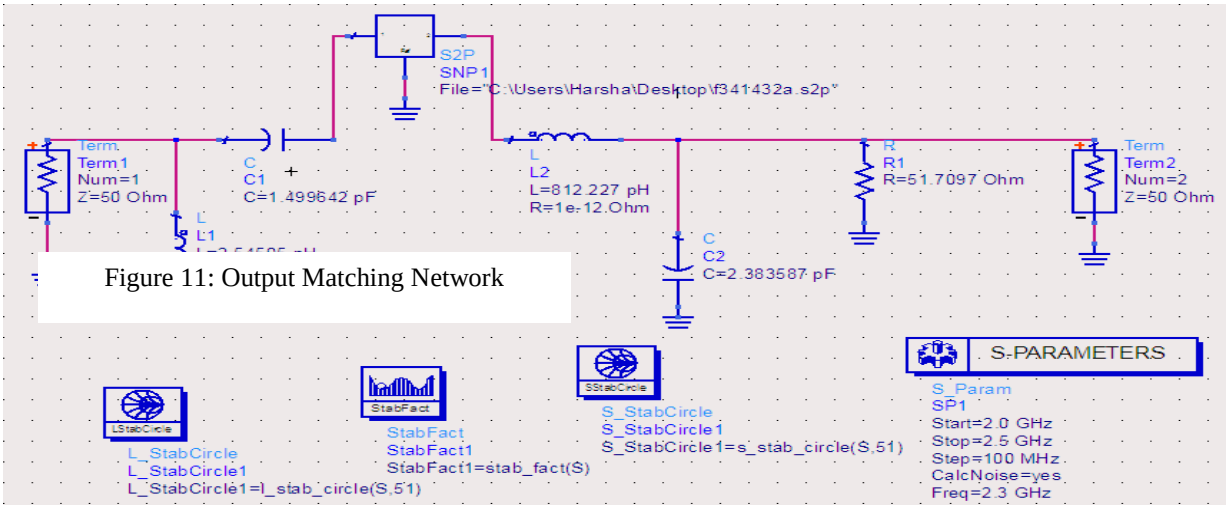

Figure 11: Output Matching Network

Figure 13: Complete Designed Circuit in ADS

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The complete LNA design followed by a Stability Factor, Stabilization and Matching Networks are shown in the Figure 13.

The simulated results of LNA such as gain and NF are shown in Figure 14. In this, gain is represented by blue line and NF is represented by green line. It shows that at 2.3 frequency gain value is 17.07 dB and NF value is 0.7334 dB.

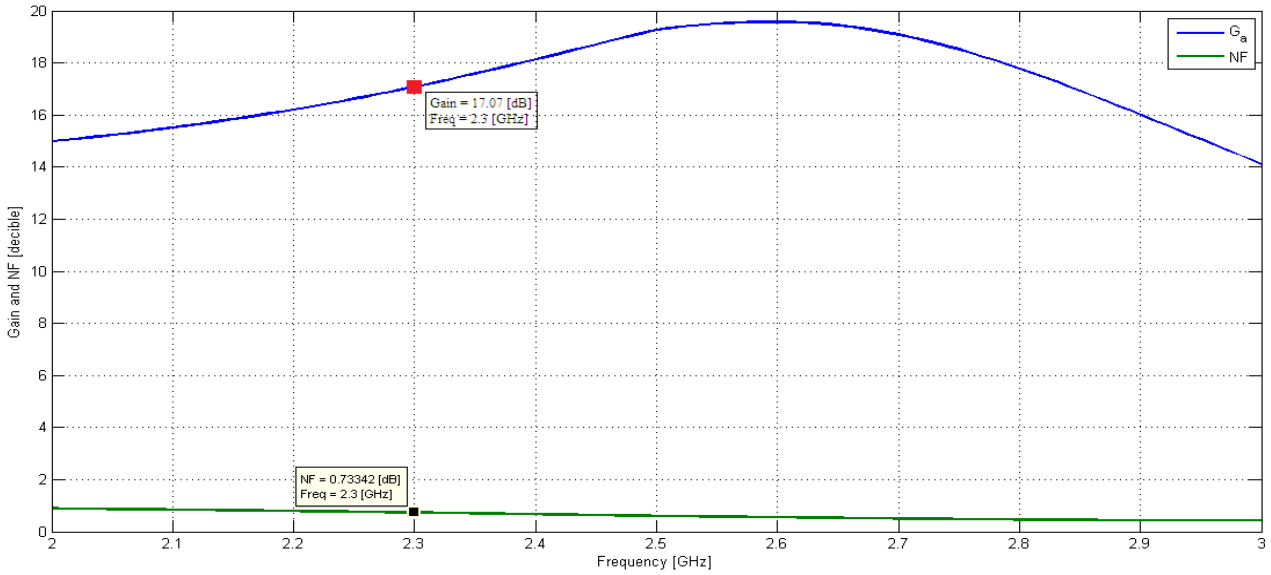

Figure 14: Graph of Frequency vs. Available Gain and NF

IV. CONCLUSION

In this paper, we have designed and simulated a Low Noise Amplifier for cellular phone 4G Network at 2.3 GHz frequency. The designed LNA provides with the Gain of 17.0787 dB and the Noise Figure of 0.7334 dB. This helps in reducing the overall effect of noise and increasing the quality of signal obtained by the receiver hence improving the sensitivity.

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