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Categorization of Traps in Recessed Gate Normally –Off MOSHEMT on InAlN/GaN

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ABSTRACT: In this paper, HEMT based on GaN is lay bare for high frequency applications. GaN based devices have significant advantages in power density, thermal characteristics, and voltage range over those based on conventional compound semiconductors or Silicon. With GaN, as in other materials systems there are significant advantages in cycle time and strength of design from use of TCAD.Traps and trap-related upshots in recessed-gate normally-off InAlN/GaN-based MOSHEMT with Al2O3 gate dielectric were characterized. Hysteresis in ID-VG was observed at elevated temperature (~120°C) due to the traps. To understand the traps, current transient in drain was investigated at given gate and drain pulses with different temperatures. Two groups of time constants were extracted: one is nearly constant and the other is decreased with temperature. Using extracted exponential trap density profile from frequency dependent conductance method [4], we could understand C-V behavior with frequency. It was shown that raps inside InAlN layer are a main cause for the decrease of capacitance at high frequency in inversion region. The pulsed I-V characteristics also show frequency dependence.

KEYWORDS: traps;recess;detraps;transient

I. Introduction

InAlN/GaN high electron mobility transistor (HEMT) is one of the strong candidates for next-generation power and microwave devices [1]. Recently, the metal-oxide-semi conductor heterostructure field-effect transistor (MOSHFET) using the recessed-gate was proposed to reduce the gate current and realize the normally-off characteristics [2]. However, problems of dispersion upshots and instabilities due to the presence of traps still prevent the wide usage of this new device. Previously, various methods have been used to study the electrical traps in InAlN/GaN HEMTs. However, relatively few studies have been made about the traps and trap-related upshots in InAlN/GaN MOSHFETs with a recessed-gate. In this paper, we investigate the traps and trap-related upshots in recessed-gate InAlN/GaN MOSHFETs using various characterization methods including the current transient spectroscopy, frequency dependent conductance method, C-V, and pulsed I-V[3], [4]. we have investigated the trapping and detrapping characteristics of GaN HEMTs before and after device degradation through a new current transient analysis methodology. In fresh devices, we can identify trapping occurring in the GaN buffer and also at the surface or inside the InAlN barrier. We have also found that electrical degradation introduces new traps with a broad spectrum of detrapping time constants in the drain side of the device, either inside the InAlN barrier layer or at the device surface. In contrast,buffer trapping is not affected by electrical degradation.

II. DEVICE FABRICATION

Fig.1 depicts schematic cross sectional view of the fabricated InAlN/GaN MOSHFETs with a recessed-gate, respectively. The structure from the top of the epi-layers has a 3 nm GaN capping layer, a 30 nm InAlN, a 3 µmGaN, and buffer layers grown on 8-inch Si (111) substrate. A recess structure was formed under a gate electrode by etching the capping layer and InAlN layer, and forming the 20 nm-thick Al_2O_3layer using the ALD method as shown. As expected, a

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lot of threading dislocations due to lattice mismatch between Si substrate and GaN material are observed in a TEM image.

Fig. 2 shows the transfer and output curves of the fabricated device having a channel width of 100 µm, which well demonstrates a normally-off operation with a turn-on voltage (Von) of 1 V. This device has a very small gate leakage current of around 10 pA. The on-current reaches up to 0.12 A/mm at given V_{GS} of 4.5 V and V_{DS} of 6 V. Fig.3 compares the drain current (I_D) hysteresis of fabricated recessed-gate InAlN/GaN MOSHFETs at different temperatures (27 and 120°C). From the figure, the hysteresis is observed clearly at a high temperature (120°C), which demonstrates the existence of the traps. The I_D at 120°C for a given gate bias (V_G) is smaller than that at 27°C due to the electron mobility decreased by phonon scattering.

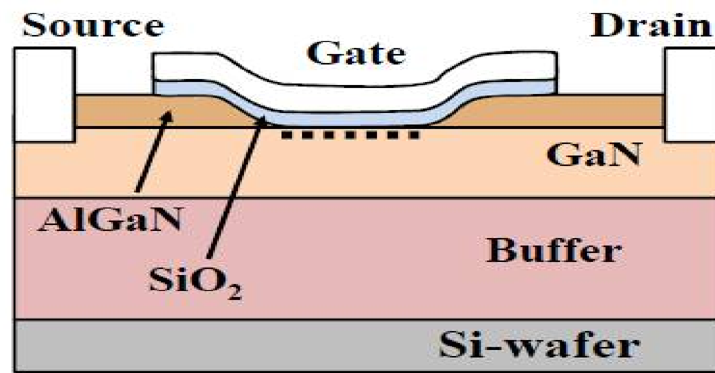

Fig.1. Schematic cross sectional view of the fabricated AlGaN/GaN MOSHFETSs with recessed gate respectively. The structure from the top of the epi-layers has a 3 nm GaN capping layer, a 30 nm AlGaN, a 3µm GaN, and buffer layers grown on 8-inch Si (111)

The AlGaN/GaN high electron mobility transistor (HEMT) is one of the strong candidates for next-generation power and microwave devices [1]. Recently, the metal-oxide-semiconductor heterostructure field-effect transistor (MOSHFET) using the recessed-gate was proposed to reduce the gate current and realizes the normally-off characteristics [2]. However, problems of dispersion effects and instabilities due to the presence of traps still prevent the wide usage of this new device. Previously, various methods have been used to study the electrical traps in AlGaN/GaN HEMTs. However, relatively few studies have been made about the traps and trap-related effects in AlGaN/GaN MOSHFETs with a recessed-gate. In this paper, we investigate the traps and trap-related effects in recessed-gate AlGaN/GaN MOSHFETs using
Various characterization methods including the current transient spectroscopy, frequency dependent conductance method, *C-V*, and pulsed *I-V* [3], [4].

III. SIMULATION DEVICE STRUCTURE

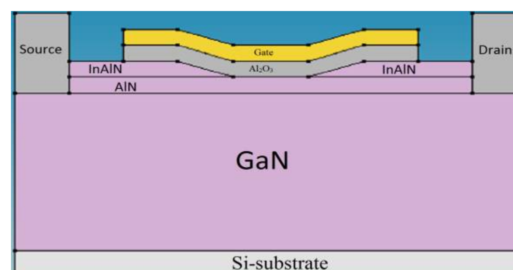

Fig. 2. Schematic cross-sectional view of recess gate InAlN/GaN MOS-HEMT built on silicon substrate

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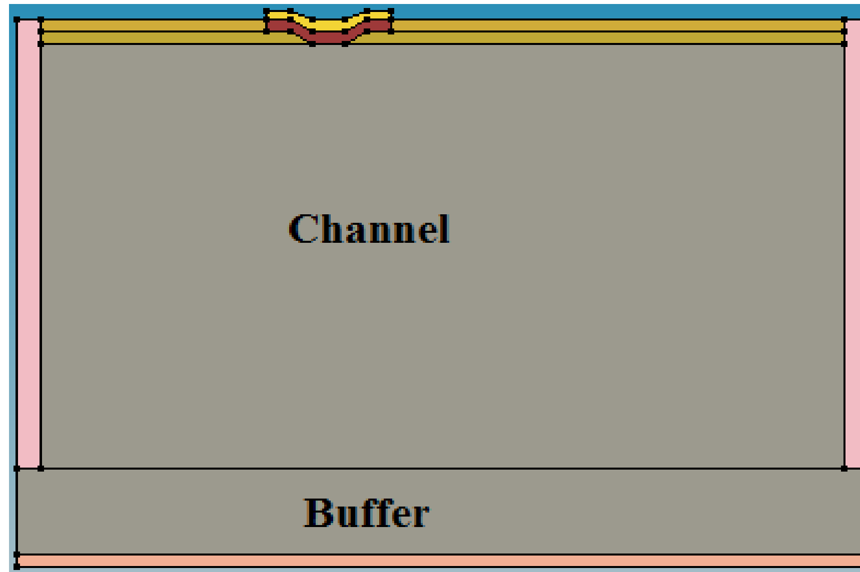

Fig.3. SENTAURUS Structure Editor in TCAD with encoded Script.

However, problems of dispersion upshots and instabilities due to the presence of traps still prevent the wide usage of this new device. Earlier methods have been used to study the electrical traps in InAlN/GaN HEMTs. In fresh devices, it is identified trapping occurring in the GaN buffer and also at the surface or inside the InAlN barrier. It is found that electrical degradation introduces new traps with a broad spectrum of detrapping time constants in the drain side of the device, either inside the InAlN barrier layer or at the device surface. In contrast, buffer trapping is not affected by electrical degradation.

When the drain bias is small, the drain current decreases with time. However, the current increases abnormally when drain bias is large and T is relatively low. It seems that applied drain pulse detraps in part the trapped electrons near the recessed-gate so that the drain current increases. Extracted τs can be categorized into two groups depending on the dependence also studied the recovery process from a current collapse event in a fresh device. Current collapse was induced by applying a voltage pulse of certain duration and monitoring the subsequent ID transient. The τin group 1 hardly varies with T, but the τ in group 2 significantly decreases with increasing T. Interestingly, the traps extracted from the drain bias transient have T dependence only, which is similar to the group 2 of the gate bias transient.

However, at high f, electrons in the channel cannot move near the gate oxide to respond V_G variation due to slower charging/discharging times of traps, which leads to reduced gate capacitance. Since the effect of traps is reflected on the property of the low frequency noise, we measured low frequency noise by changing VG from -0.5 V to 3.9 V at a fixed V_D of 0.5 V as shown in Fig.4 The frequency dependence is also observed in pulsed I-Characteristics. The drain currents are measured for pulsed gate bias which is changed from -2 V to 4 V and get back to -2 V without any break (a round-trip pulsed biasing). Note that I_D collapse due to the electron trapping from the gate into the InAlN surface is not occurred because high-quality gate oxide was formed with a thickness of 20 nm. The traps related to the group 2 seem to be located near the interface between the gate oxide and the GaN, and InAlN layer. Transient drain current behavior with gate and drain bias pulse was systematically investigated. Spacer AlN is used to reduce the scattering of electrons, to get regular response of drain current and the traps and the effects caused by traps occurs in recessed gate will be characterize by investigating transients occurs in the drain current by varying temperature.

IV. RESULTS AND DISCUSSIONS

DC Characteristics

The AlInN/GaN high electron mobility transistor (HEMT) is one of the strong candidates for next-generation power and microwave devices [1]. Recently, the metal-oxide-semi conductor heterostructure field-effect

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transistor (MOSHFET) using the recessed-gate was proposed to reduce the gate current and realize the normally-off characteristics. we investigate the traps and trap-related effects in recessed-gate AlInN/GaN MOSHFETs using various characterization methods including the current transient spectroscopy, frequency dependent conductance method, *C*-*V*, and pulsed *I*-*V* [3], [4].

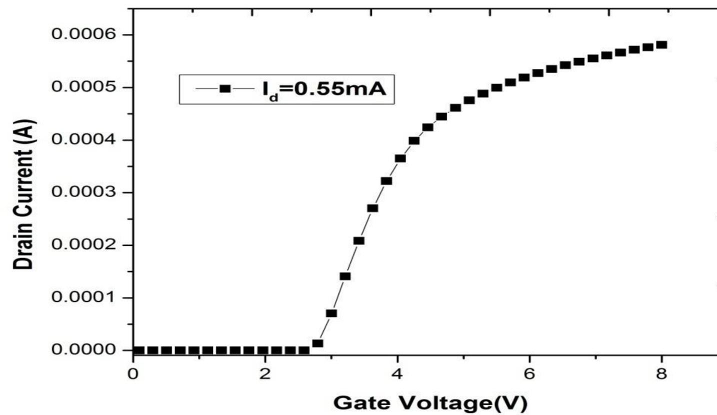

Fig 4: I_D-V_G curves and the gate leakage at V_D = 0.5 V.

Fig. 4 shows the transfer and output curves of the fabricated device having a channel width of 100 nm, which well demonstrates a normally-off operation with a turn-on voltage (*V*on) of 1 V. This device has a very small gate leakage current of around 10 pA. The on-current reaches up to 0.35 A/mm at given V_{GS} of 4.5 V and V_{DS} of 6 V.

Fig. 5 compares the drain current (I_D) hysteresis of fabricated recessed-gate AlInN/GaN MOSHFETs at different temperatures (27 and 120°C). From the figure, the hysteresis is observed clearly at a high temperature (120°C), which demonstrates the existence of the traps. The *I*D at 120 °C for a given gate bias (V_G) is smaller than that at 27 °C due to the electron mobility decreased by phonon scattering.

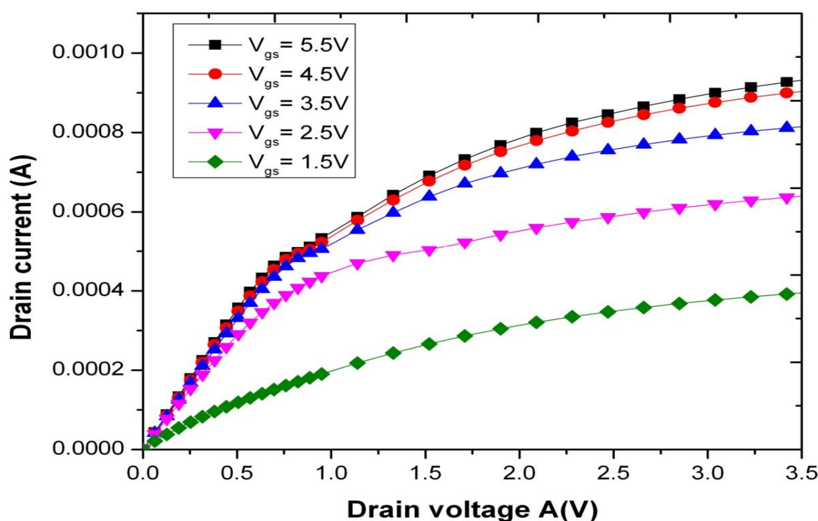

Fig 5: I_D-V_D curves under different temperatures (a) 27 °C and (b) 120 °C. A hysteresis in the drain current is observed in high temperature condition.

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The frequency dependent conductance method shows the frequency response of the trap with various V_{Gs} [4]. Peak amplitude and peak *f* are related to the density of trap states and the characteristic time of traps respectively. The extracted trap density (D_{it}) which is shown in Fig. 6 ,7 by changing E_T-E_C extracted from the τ. The D_{it} increases exponentially as close to the conduction band (E_C). At an E_T-E_C of -0.4 eV, the D_{it} is ~1×1012 cm-2eV-1.

Characterising of On Current and Off Current

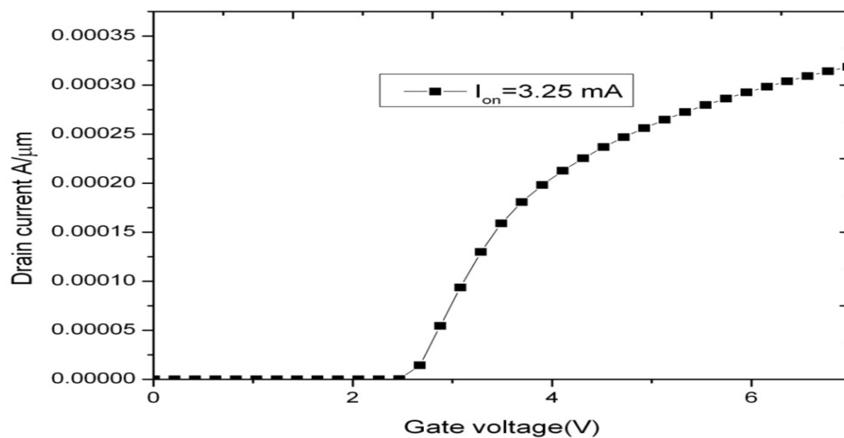

Fig 6**:** Transfer characteristics of AlInN/GaN MOS-HEMT on-current. The drain-to source voltage is 0.1 V. The channel length and channel width were 2 µm and 200 µm, respectively with the on current value(I_{on}=3.25mA)

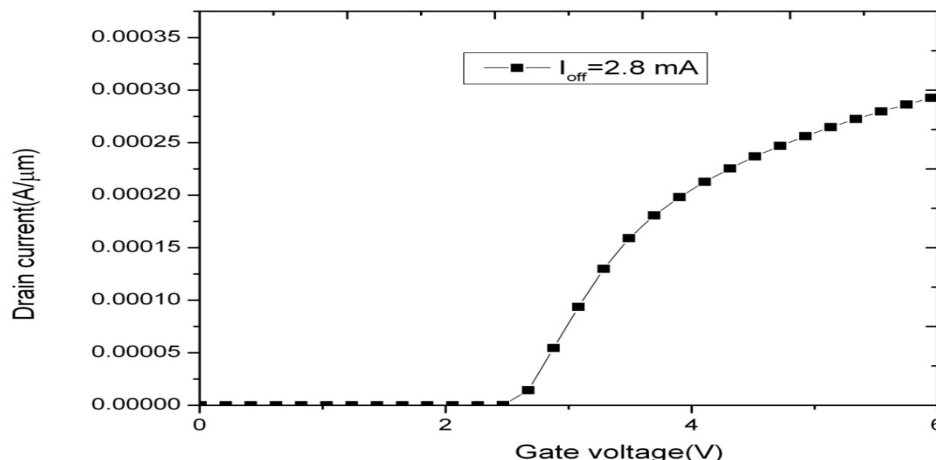

Fig 7**:** Transfer characteristics of AlInN/GaN MOS-HEMT. The drain-tosource voltage is 0.1 V. The channel length and channel width were 2 µm and 200 µm, respectively with the off current value(I_{off}=2.8mA)

Trap Density

we extracted trap density (D_{it}) which is shown in Fig. 8 by changing E_T-E_C extracted from the . The D_{it} increases exponentially as close to the conduction band (E_C). At an E_T-E_C of -0.4 eV, the D_{it} is ~1$10^{12}$ $cm^{-2}eV^{-1}$. The frequency dependent conductance method shows the frequency response of the trap with various V_{Gs}

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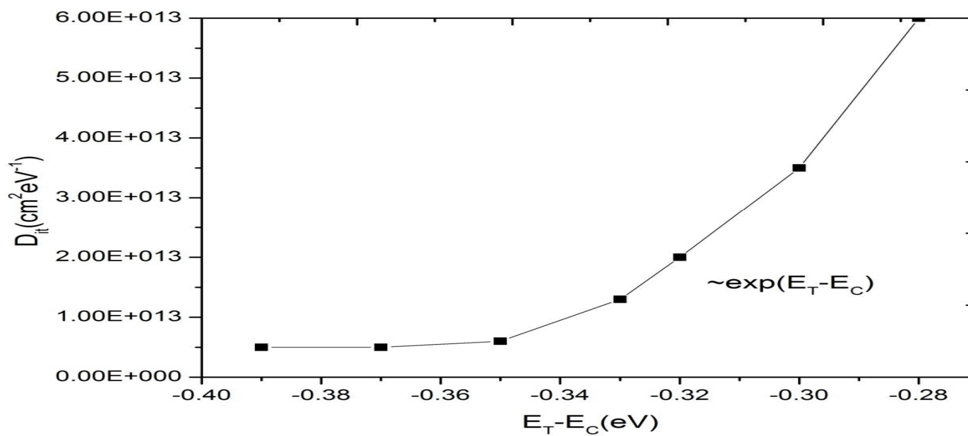

Fig 8: Extracted trap density from frequency dependent conductance method. *D*it nearby the conduction band fits well with exponential function.

***C-V* characteristics**

Fig. 9 shows gate capacitance versus V_G as a parameter of *f*.As a control, dotted lines represent the *C-V* curves of the MOSHEMT without the gate recess. Both devices show significant difference in *C-V* with *f* due to the traps in the AlInN layer. The control device has a threshold voltage (V_{th}) of ~ -11 V so that the gate capacitance (C_G) starts to increase near V_{th}. As V_G increases more than V_{th}, the C_G increases slightly at 1 kHz, but the C_G is nearly constant at 1 MHz, since the channel electrons moves easily to a part of the AlInN layer for a given V_G at 1 kHz.

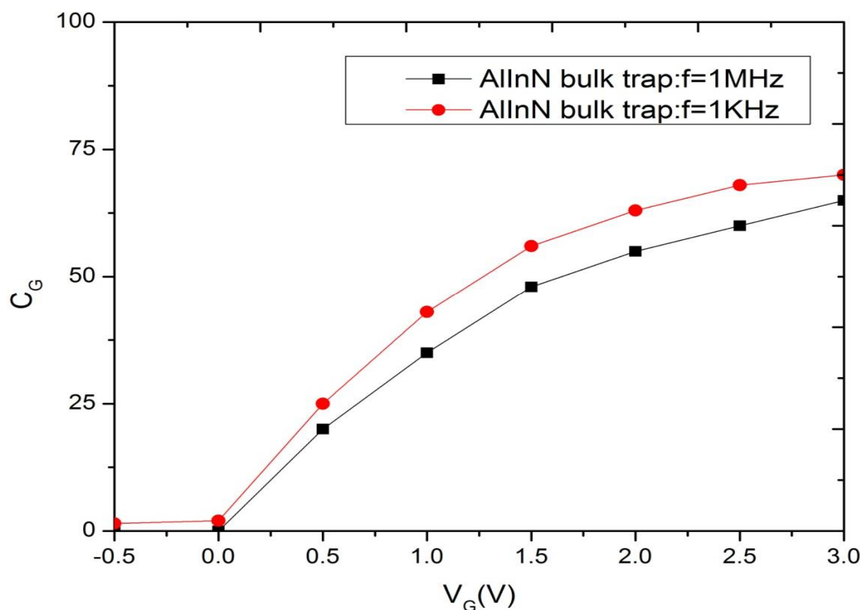

Fig 9: *C-V* characteristics of two types of devices with and without gate recess region as a parameter of frequency. *C*G is measured while the source is floated.

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V.CONCLUSION

Characterized traps and trap-related effect in normally-off InAlN/Gan-based MOSHEMT with $Al_2 0_3$gate oxide. Transient drain current behavior with gate and drain bias pulse was systematically investigated. Traps were extracted using frequency dependent conductance method. Significant capacitance decrease in inversion region of device at a frequency of 1 MHz was attributed to the traps in InAlN layer.Herein the current transient spectroscopy, frequency dependent conductance method, *C-V*, and pulsed *I-V* methods are used to characterize the traps by observe the traps. In this work Spacer has used to reduce the scattering of electrons, to get regular response of drain current and the traps and the effects caused by traps occurs in recessed gate will be characterize by investigating transients occurs in the drain current by varying temperature and observed the trap density with drain current.

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