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Power Reduction in H.264 /Audio Video Codec: A Survey

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ABSTRACT: H.264/AVC video compression standard provides high coding efficiency, but it has high complexity and consumes more power. This paper explains advantages of H.264 audio video codec and why this H.264 technology should be on the shopping list of every business. Digital video streams, especially at high definition (HD) resolution, represent huge amounts of data. In order to achieve real-time HD resolution over typical Internet connection bandwidths, video compression is required. The amount of compression required to transmit 1080p video over a three megabits per second .As compared to other standards (MPEG, H.261, H.262 and H.263) H.264/Audio video codec standard reduces the power as 50mw to 75mw using partial MB (Macro Block) reordering and lossless frame recompression technique. This power will be further reduced to 25mw to 50mw using pipelining technique as a proposed method.

KEYWORDS: HD,MB,MPEG,ME,MC,AVC

I. INTRODUCTION

The latest video compression standard, H.264 (also known as MPEG-4 Part 10/AVC for Advanced Video Coding), is expected to become the video standard of choice in the coming years. H.264 is an open, licensed standard that supports the most efficient video compression techniques available today. Without compromising image quality, an H.264 encoder can reduce the size of a digital video file by more than 80% compared with the Motion JPEG format and as much as 50% more than with the MPEG-4 Part 2 standard. This means that much less network bandwidth and storage space are required for a video file. In another way, much higher video quality can be achieved for a given bit rate. Jointly defined by standardization organizations in the telecommunications and IT industries, H.264 is expected to be more widely adopted than previous standards.H.264 has already been introduced in new electronic gadgets such as mobile phones and digital video players, and has gained fast acceptance by end users. Service providers such as online video storage and telecommunications companies are also beginning to adopt H.264. In the video surveillance industry, H.264 will most likely find the quickest traction in applications where there are demands for high frame rates and high resolution, such as in the surveillance of highways, airports and casinos, where the use of 30/25 (NTSC/PAL) frames per second is the norm. This is where the economies of reduced bandwidth and storage needs will deliver the biggest savings. H.264 is also expected to accelerate the adoption of megapixel cameras since the highly efficient compression technology can reduce the large file sizes and bit rates generated without compromising image quality. There are tradeoffs, however. While H.264 provides savings in network bandwidth and storage costs, it will require higher performance network cameras and monitoring stations.

II. COMPRESSION TECHNIQUES

Lossless Compression:
Lossless compression explains how the data is stored without resulting in any loss of information. A zip file uses lossless compression, so that when they are unzipped, the original files are recovered. Since a single bit error in a PowerPoint file or an application can render it unusable, lossless compression is mainly used to maintain data integrity. In both of these examples the compression ratios are only perhaps 2:1 or 5:1.
LossyCompression:

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The MP3 file format for music uses lossy compression technique. While MP3 files are not exact copies of music stored on a CD, they have been good enough to have basically rendered audio CD obsolete. In the case of video, lossy compression is valuable, since there is much more information in images than the eyes or brain can absorb. By understanding how we process visual information, lossy compression algorithms can reduce the amount of data that is transmitted in a way that has negligible impact to the viewer.

Redundancy Encoding:

In most video images, there are some elements that are relatively uniform, such as a blank whiteboard or a wall. Video compression algorithms take advantage of spatial redundancy by grouping pixels into blocks. When blocks are relatively uniform, they can be represented by far fewer bits than if each pixel were represented individually. Also, there are usually periods when there is very little or no change from one frame to another – such as the background behind a speaker in a video call. Video compression algorithms take advantage of temporal redundancy by only transmitting the differences between consecutive frames.

III. H.264/AVC

H.264 is the result of a joint project between the ITU-T's Video Coding Experts Group and theISO/IEC Moving Picture Experts Group(MPEG).The goal ofH.264 Advanced Video Coding (AVC) Standard to provide high quality video at considerably lower bit rates than previous standards. ITU-T is the sector that coordinates telecommunications standards on behalf of the International Telecommunication Union. ISO stands for International Organization for Standardization and IEC stands for International Electro technical Commission, which oversees standards for all electrical, electronic and related technologies. H.264 is the name used by ITU-T, while ISO/IEC has named it MPEG-4 Part 10/AVC since it is presented as a new part in its MPEG-4 suite. The MPEG-4 suite includes, for example, MPEG-4 Part 2, which is a standard that has been used by IP-based video encoders and network cameras.

Goals of H.264:

- Implementations that deliver an average bit rate reduction of 50%, given a fixed video quality compared with any other video standard.
- Error robustness so that transmission errors over various networks are tolerate.
- Low latency capabilities and better quality for higher latency
- Straightforward syntax specification that simplifies implementations
- Exact match decoding, which defines exactly how numerical calculations are to be made by an encoder and a decoder to avoid errors from accumulating

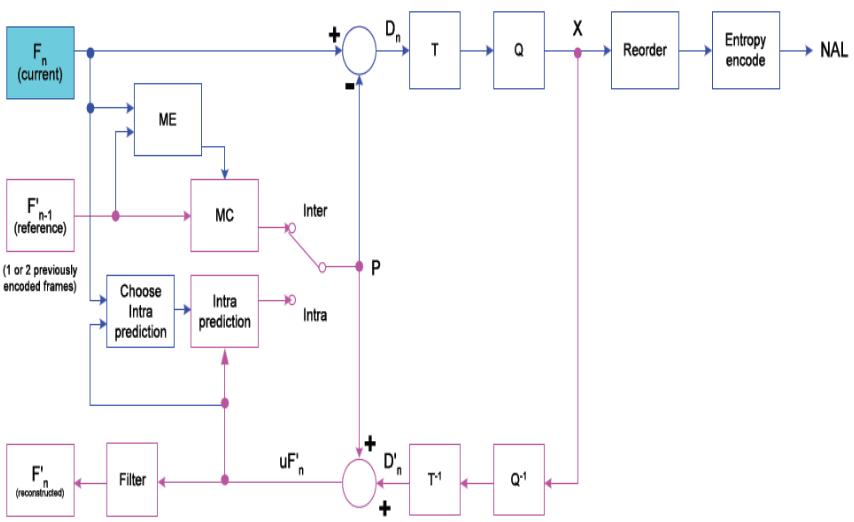

Figure1:H.264/ AVC Encoder

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H.264 Advanced Video Coding (AVC) Standard:

1. H.264 encoded video is captured at the correct resolution and bit rate for transmission from the encoding camera.
2. An uncompressed video is captured at the correct resolution for display from the encoding camera.
3. At the far end, received video must be decoded or uncompressed.
4. Finally, uncompressed video must be resized for display.

In common with earlier standards (such as MPEG1, MPEG2 and MPEG4), the H.264 standard does not explicitly define a CODEC (encoder / Decoder pair). Rather, the standard defines the syntax of an encoded video bit stream together with the method of decoding this bit stream. In practice, however, a compliant encoder and decoder are likely to include the functional elements. The important changes in H.264 occur in the details of each functional element.

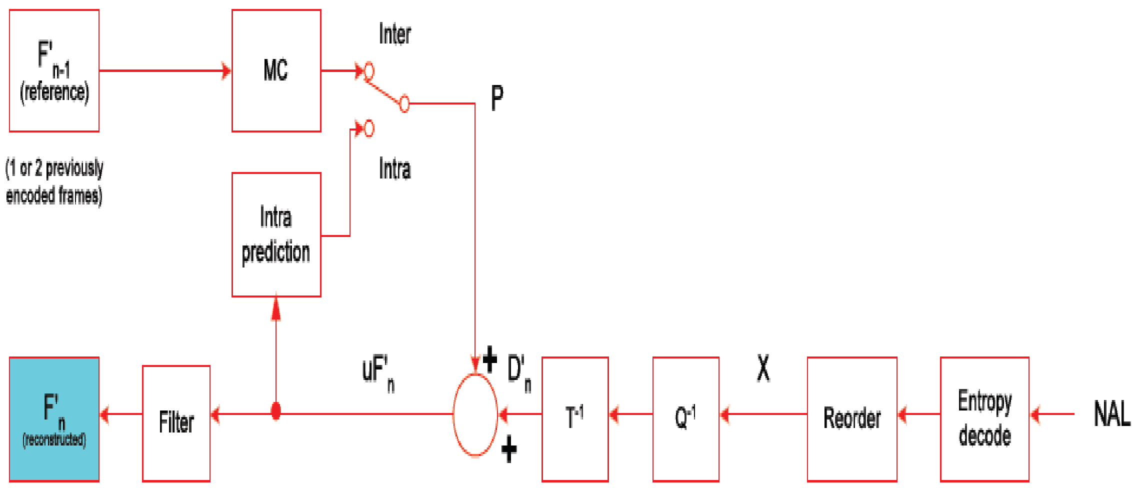

Figure2: H.264/AVC Decoder

IV.ANALYSIS AND DESIGN SPACE EXPLORATION

The considerations of hardware design are analyzed with the H.264/AVC compression algorithms. The major challenges are described as follows.

Computation Complexity and Bandwidth Requirement:
According to the profiling, H.264/AVC requires much more computation complexity than previous coding standards. This will greatly increase the hardware cost especially for the HDTV applications. The bandwidth requirement of H.264/AVC encoding system is also much higher than previous coding standard.The MRF-ME contributes the most traffic for loading reference pixels. Neighboring reconstructed pixels are required by intra prediction, and are also required by deblocking filter. Besides, Lagrangian mode decision and context-adaptive entropy coding have data dependencies between neighboring MB, and transmitting related information contribute considerable bandwidth as well. An efficient memory hierarchy combined with data sharing and Data Reuse (DR) scheme must be designed to reduce the system bandwidth.

Sequential Flow:
The H.264/AVC reference software adopts much sequential process to enhance the compression performance. It is hard to efficiently map the sequential algorithm to parallel hardware. For system architecture, we partition the sequential encoding process prediction, reconstruction, and then entropy encoding) into several tasks and process them in MBbased pipelining structure, which improves the hardware utilization and the throughput. For module architecture, this problem is critical for ME since ME is the most computationally intensive part and requires the most degrees of parallelism. The inter Lagrangian mode decision takes MV costs into consideration. The MV of each block is generally

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medium predicted by left, top, and top-right neighboring blocks. The cost function can be computed only after prediction modes of neighboring blocks are determined which also causes inevitable sequential processing. The modified hardware-oriented algorithms can be designed to enable parallel processing.

Loops:

In traditional video coding standard, there is a frame-level reconstruction loop generating the reference frames for ME and MC. In H.264/AVC, the intra prediction requires the reconstructed pixels of the left and top neighboring blocks, which induce the MB-level and block-level reconstruction loops. For the MB-level reconstruction loop as shown in Fig. 1 (a), the reconstructed pixels of MB-a, MB-b, and MBc are used to predict the pixels in MB-x for I16MB. Not until MB-a, MB-b, and MB-c are reconstructed can MB-x be predicted.

Data Dependency:

The new coding tools improve the compression performance with many data dependencies. The frame level data dependencies contribute the considerable system bandwidth. The dependencies between neighboring MBs constrain the solution space of MB pipelining, and those between neighboring blocks limit the possibility of parallel processing.

Abundant Modes:

There are many algorithms of H.264/AVC that have multiplex modes. For example, there are 17 different modes for intra prediction while 259 kinds of partitions for inter prediction. Six kinds of 2-D transform, 4×4/2×2 DCT/IDCT/Hadamard transform, are involved in reconstruction loops. The reconfigurable processing engine, reusable prediction core, and appropriate pipeline system design are important to efficiently support all these functions.

TABLE I : CHIP FEATURES OF H.264/AVC DECODER

Technology	TSMC 0.18 μm1P6M CMOS
Pad/Core Voltage	3.3/1.8 V
Core Area	2.19×2.19 mm2
Logic Gates	21.743 K (2-input NAND gate)
SRAM	9.98 Kbyte
Profile	Baseline
Operating Frequency	120/1.5 MHz for DTV1024P 30fps/QCIF
Power Consumption	186.4/1.18 mW

V. PREVIOUS WORKS

MPEG-4:

MPEG-4, compared to other existing coding standards like MPEG-2 and H.26x, targets a much broader set of applications, with an accompanying increased number of more complex algorithms as well as coding modes. This extended functionality requires a flexible and extensible platform. However, the computational complexity of MPEG-4 applications exceeds that of state-of-the-art media processors, especially for profiles suitable for digital TV broadcast. Furthermore, the increasing demand to combine audiovisual material with (advanced) graphics within the application domain of TV and set-top boxes enhances the complexity of these systems severely. For the adopted architecture template, an effective HW/SW partitioning was performed based on the MPEG-4 application analysis in terms like amount of parallelism, throughput requirements, the control complexity and the reuse potential. This analysis resulted in a feasible mapping of the MPEG-4 decoding application onto the architecture template. This template features a two-level hierarchical communication structure in order to increase the flexibility without alleviating the required bandwidth to the off-chip memory. The MPEG algorithm gives to the decoder the freedom of choice in terms of size of Search and Reference blocks. During the block matching, what means to find the block that better closes with the Reference block; most pixels will be used multiple times. So we can hope to reuse the data read from memory trying the improvement of the computational prediction of the memory bandwidth necessary to data input.

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H.261: Video Coding and Decoding (CODEC):

H.261 is video coding standard by the ITU. It was designed for data rates which are multiples of 64Kbit/s, and is sometimes called p x 64Kbit/s (p is in the range 1-30). These data rates suit ISDN lines, for which this video codec was originally designed for. H.261 transport video stream using the real-time transport protocol, RTP, with any of the underlying protocols that carry RTP. The coding algorithm is a hybrid of inter-picture prediction, transform coding, and motion compensation. The data rate of the coding algorithm was designed to be able to be set to between 40 Kbits/s and 2 Mbits/s. INTRA coding where blocks of 8x8 pixels each are encoded only with reference to themselves and are sent directly to the block transformation process. On the other hand INTER coding frames are encoded with respect to another reference frame. The inter-picture prediction removes temporal redundancy. The transform coding removes the spatial redundancy. Motion vectors are used to help the codec compensate for motion. To remove any further redundancy in the transmitted bit stream, variable length coding is used. H261 supports motion compensation in the encoder as an option. In motion compensation a search area is constructed in the previous (recovered) frame to determine the best reference macro block. H261 supports two image resolutions, QCIF (Quarter Common Interchange format) which is (144x176 pixels) and CIF (Common Interchange format) which is (288x352).

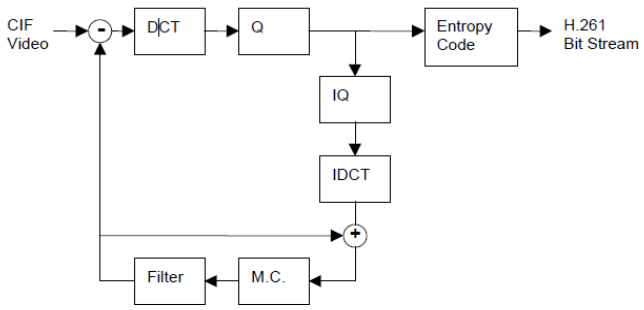

Figure3: H.261 Encoder

The video multiplexer structures the compressed data into a hierarchical bit stream that can be universally interpreted. The hierarchy has four layers:

1. Picture layer: corresponds to one video picture (frame)
2. Group of blocks: corresponds to 1/12 of CIF pictures or 1/3 of QCIF
3. Macro blocks: corresponds to 16x16 pixels of luminance and the two spatially corresponding 8x8 chrominance components.
4. Blocks: corresponds to 8x8 pixels

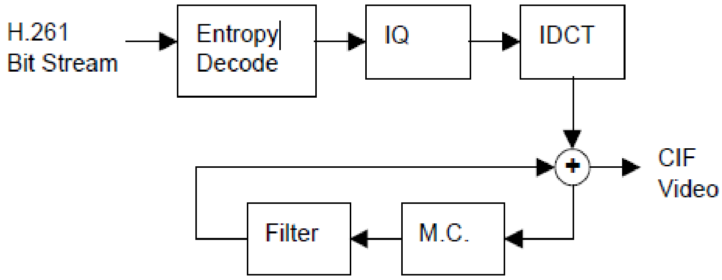

Figure4: H.261 Decoder

H.263 AVC

A low power full-search block matching (FSBM) motion estimation design for the H.263+ low bit rate video coding was implemented. The features of H.263+ such as half-pixel precision and some advanced modes (advance

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prediction mode, PB-frame mode and reduced resolution update mode) are taken into consideration. This architecture can deal with different block size and searching range in a single chip without any latency. We use a 1-D and 2-D mixed architecture to fulfill this goal. To achieve the purpose of low power and reduce the design period, we use dual supply voltage levels in this chip. This chip is realized by TSMC 0.6um single-poly triple-metal CMOS technology. The operation frequency is set at 60MHz to meet the requirement of the real time processing in the reduced resolution update mode in H.263. The power consumption is 424mW at 60MHz and the throughput is 36 frames per second with CIF format at 60MHz. The IU and HU are used to calculate the MAE in integer pixel and half-pixel precision individually. In IU, we use 64 processing elements (PE) that is a tradeoff between speed and area. The current and previous frame data come from the off chip memory and don't include in our architecture.

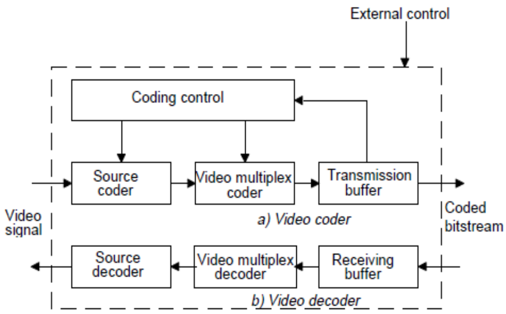

Figure.5: H.263 Decoder

Table II. Chip specification of H.263

PE number	64
Frame size	176_144 & 352_288
Searching range	16_16 & 32_32
Block size	8_8, 16_16 & 32_32
Frame rate	30 to 120 frames/sec
Technology	TSMC 0.6um CMOS SPTM
Number of transistors	267208
Number of I/O pads	113
Core size	(6702.8_6366.2) um
Die size	(6344.8_6008.2) um
Package	120 CQFP
Clock rate	60MHz

VI.RESULTS OF PREVIOUS WORKS

The H.261 /AVC has high power consumption of 992.4mw at a bit rate of 40kbps-2Mbps and in H.262 standard power is reduced as 736mw at a bit rate of 1-25 Mbps. At high resolution (1408×1152) of H.263 bit rate is improved as 20kbps-4Mbps and it consumes 424mw power. In an existing Method of H.264 power is reduced as 50mw to 75mw at 60MHZ with a bit rate of 64 kbps up to 25 Mbps using partial MB reordering and lossless frame recompression technique. This power is further reduced in H.264/AVC using pipelining is proposed.

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Table III. Resolution, Bit rate and power consumption of Compression Standards

ITU-T Recommendation	Target Resolutions	Target Bit Rates	Target Applications	Power consumption
H.261	352×288 (CIF) 176×144 (QCIF)	40 kbps - 2 Mbps	ISDN videophones	992.4mw
H.262	720×480 720×576 1280×720 1920×1080	1 - 25 Mbps	SD/HD Broadcast, DVD, HDV	736mw
H.263	128×96 176×144 352×288 704×576 1408×1152	20 kbps – 4 Mbps	Videoconferencing MMS Streaming Internet Video	424mW
H.264	128×96 up to 4,096×2,304	64 kbps up to 25 Mbps	Videoconferencing Broadcast Blu-ray Disc DV & Mobile phone cameras	50mw -75mw

VI.CONCLUSION

H.264 presents a huge step forward in video compression technology. It offers techniques that enable better compression efficiencies resolution and bit rates due to more accurate prediction capabilities, as well as improved resilience to errors. It provides new possibilities for creating better video encoders that enable higher quality video streams, higher frame rates and higher resolutions at maintained bit rates (compared with previous standards), or, conversely, the same quality video at lower bit rates. With support from many industries and applications for consumer and professional needs, H.264 is expected to replace other compression standards and methods in use today. H.264 /AVC consume less power of50mw-75mw at 60MHZ frequency. The power will be further reduced using pipelining technique as a proposed method. H.264 has been applied in diverse areas such as high-definition DVD (e.g. Blu-ray), digital video broadcasting including high-definition TV, online video storage (e.g. YouTube), third-generation mobile telephony, in software such as QuickTime, Flash and Apple Computer's MacrOS X operating system, and in home video games.

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