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Design of Active Filter to Minimize the Effect of Long Cables On Inverter Fed Induction Motor

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ABSTRACT: Inverter fed Induction motor drive systems are widely used in industrial applications because of their energy efficiency and flexible control. The motor is subjected to over voltages due to long cable length, fast rise/fall time of inverter pulses and impedance mismatch between cable and motor. The overvoltage causes premature failure of the motor insulation. The proposed active filter reduces the voltage surge and increase rise/fall time of the voltage at the motor terminals. In this paper an active filter is designed and simulated for 3-phase PWM Inverter Fed 1-hp Induction Motor drive using Simulink for different cable lengths.

KEYWORDS: Overvoltage,Filters,PWM,Induction Motor.

I. INTRODUCTION

Three phase induction motors are most widely used motors in industrial automation. It is often required to control the output voltage of the inverter for the constant voltage/frequency (V/F) control of an induction motor. PWM (Pulse Width Modulation) provides constant V/F control of an induction motor. The output voltage waveform from a PWM IGBT inverter typically has a carrier frequency in the range of 1-20kHz and the rise/fall times of the inverter output are typically in the range of 0.05 to 0.06μs. Due to fast switching pulses, the transmission line effect and the reflection which occur at the rate of the switching frequency of the inverter, high peak voltage can be experienced at the motor terminals. The characteristic impedance of induction motor is normally 50 to 100 times greater than the characteristic impedance of cable, so the voltage is reflected back towards the inverter. The absolute peak voltage is equal to the sum of the incident peak voltage travelling toward the motor plus the reflected peak voltage[1]-[4].

Thus the overvoltage at the motor terminals depends on the distance between the motor and inverter as well as on the impedance mismatch between the cable and motor surge impedance and switching frequency of the inverter. This overvoltage cause premature failure of the motor [4].The objective of this paper is to study overvoltage phenomena and to reduce the voltage surges and increase rise/fall time of the voltage at the motor terminals. There are two remedial measures put in place to protect themotor against insulation damage. The first one is to use over sized motors or inverter-duty motors with enhanced insulation system that can withstand high dielectric stress. The second one is to use passive filter networks connecting to the entire drive system [7]–[8].The drawbacks of passive filters such as bulky in size and power loss can be reduced by using the active filter.The proposed active filter is designed and simulated using Simulink.

II. HIGH FREQUENCY MODEL OF CABLE AND INDUCTION MOTOR

To obtain the high frequency parameter of the cable, two types of tests have to be carried out for the measurement of short circuit and open circuit impedances. The high frequency model of cable is shown in Fig.1 that provides a sufficiently accurate response over the frequency range of the voltage pulse[5]. The proposed model for the ac motor input impedance is based on the high-

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frequency model, which has been successfully used in calculating the over voltage. The parameters of the model are the phase-to-neutral impedance (Z_{pn}) and phase-to-ground impedance (Z_{pg}). Fig.2 shows the per-phase high-frequency motor model that is used in the calculation of the over voltage analysis. Accurate modeling of induction motors in high-frequency range plays an important role in investigating the motor drive over voltage. Here, C_g is the winding-to-ground capacitance, R_g is the winding to ground resistance, R_t is turn to turn resistance, $L_t$is the turn to turn inductance, $C_t$is the turn-to-turn capacitance and R_e-parallel resistance[5].

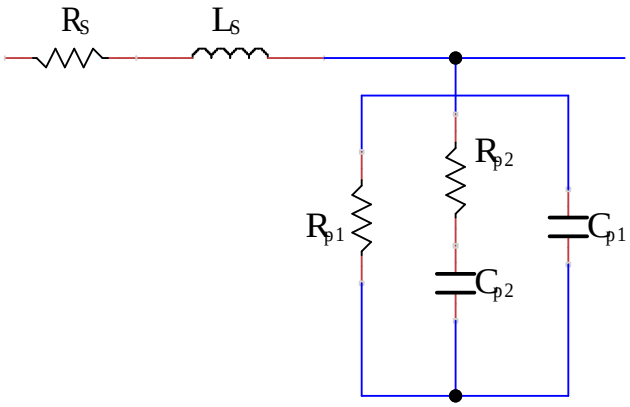

Fig.1:High frequency model of the power cable per unit length

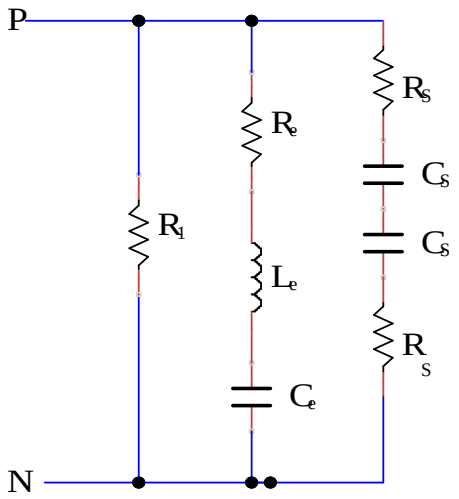

Fig.2: High frequency model of induction motor per unit phase

III. THE PROPOSED ACTIVE FILTER

Fig 3 shows the circuit of the proposed active filter. Terminalsv_{C1},v_{C2} and v_{C3} is connected to the cable terminals, while terminals v_{M1},v_{M2} and v_{M3} is connected to the motor terminals. Switches $S_1 - S_6$ in the proposed filter is switched at the fundamental frequency of the PWM pulses (less than100 Hz) transmitting towards inverter to the motor. Table 1 and Fig 4 shows the switching table of the six switches and gate signals respectively. Switches $S_1 - S_6$ are operated at low switching frequency,

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their switching losses are negligible. A general rule is applied for comparing the value of the fundamental components of v_{C1},v_{C2} and v_{C3}. When$V_{C1} > V_{C2}$, S_1 is turned OFF and S_4 is turned ON. When$V_{C1} < V_{C2}$, S_1 is turned ON and S_4 is turned OFF. When $V_{C1} = V_{C2}$, the states of S_1, S_4 remain unchanged. When$V_{C2} > V_{C3}$, S_3 is turned OFF and $S_6$is turned ON. When$V_{C2} < V_{C3}$, S_3 is turned ON and S_6 is turned OFF. When$V_{C2} = V_{C3}$, the states of S_3, S_6 remain unchanged. When$V_{C3} > V_{C1}$, S_2 is turned ON and S_5 is turned OFF. When$V_{C3} < V_{C1}$, S_2 is turned OFF and S_5 is turned ON. When$V_{C3} = V_{C1}$, the states of S_2, S_5 remain unchanged.

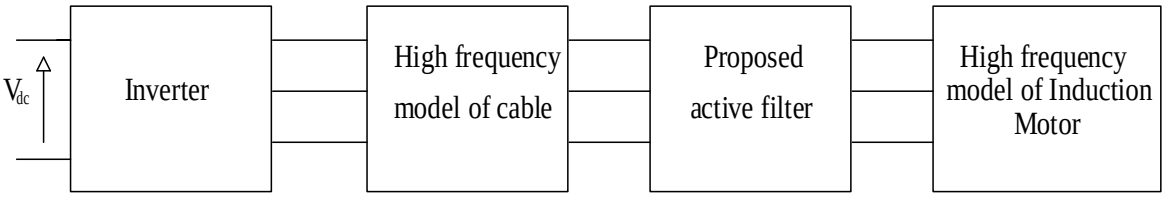

Fig. 3: Block diagram of proposed system

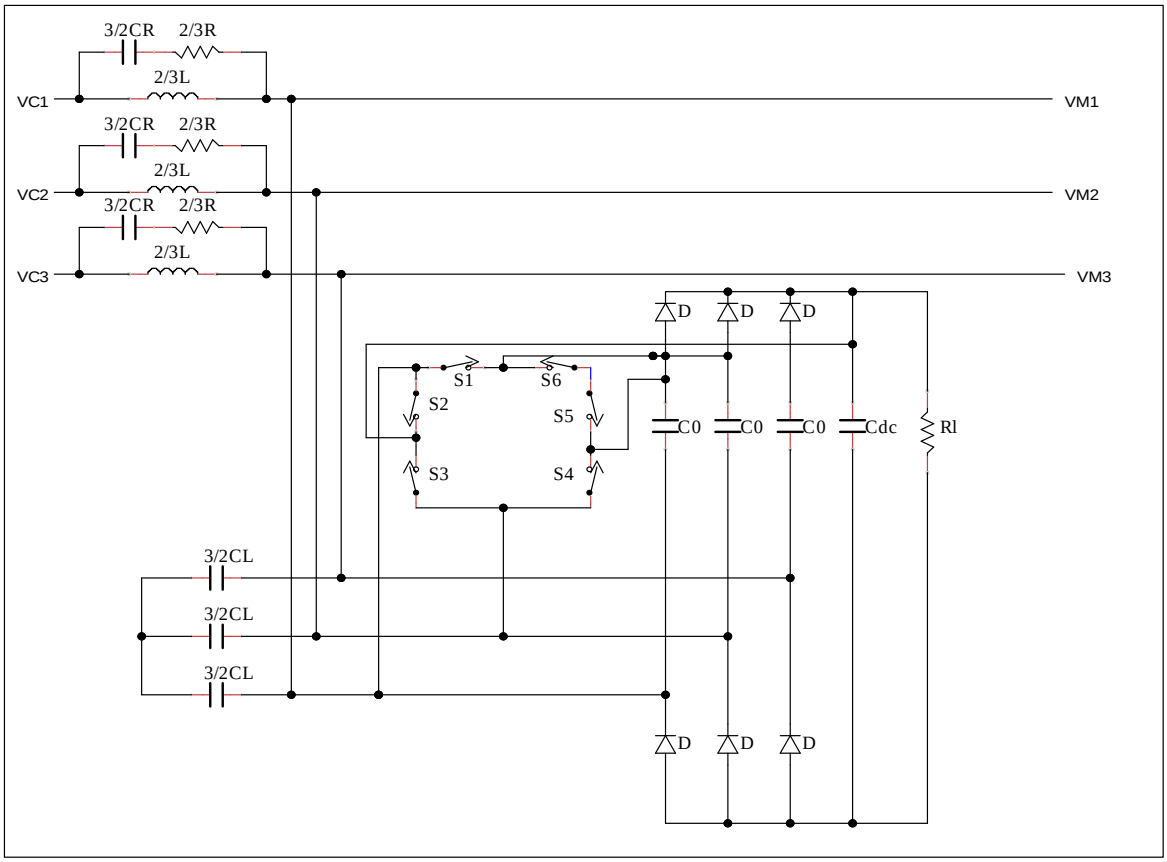

Fig 4: Proposed active filter

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VC1-VC2	**S1**	**S4**
+	OFF	ON
-	ON	OFF
0	Unchanged	Unchanged
VC2-VC3	**S3**	**S6**
+	OFF	ON
-	ON	OFF
0	Unchanged	Unchanged
VC3-VC1	**S2**	**S5**
+	ON	OFF
-	OFF	ON
0	Unchanged	Unchanged

Table 1: Gate Signals of the six switches

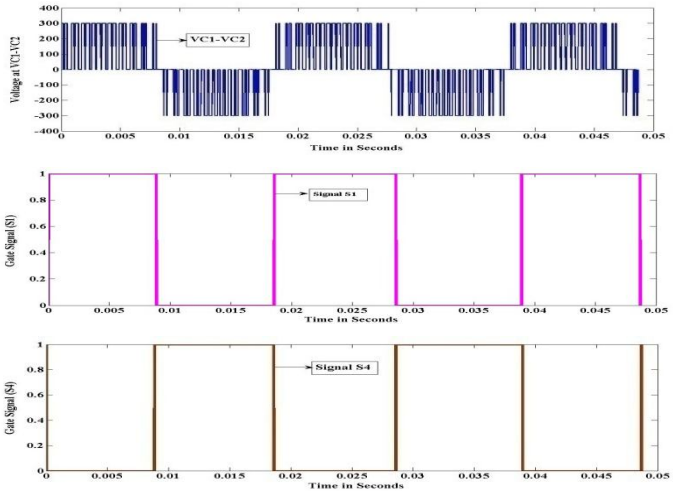
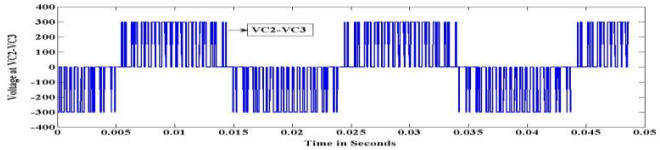


Fig 5(a): Voltage waveforms of (VC1-VC2) and gate signals to the switches S1,S4



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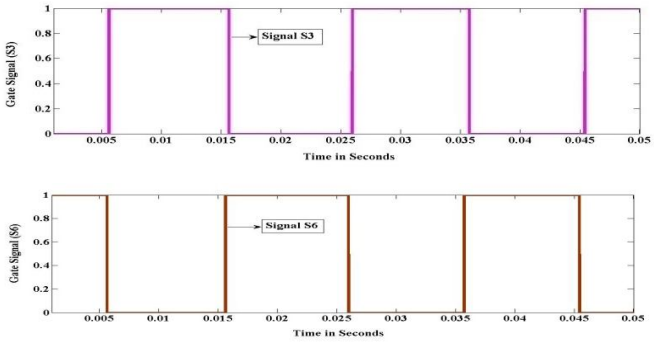

Fig 5(b):Voltage waveforms of(VC2-VC3) and gate signals to the switches S3,S6

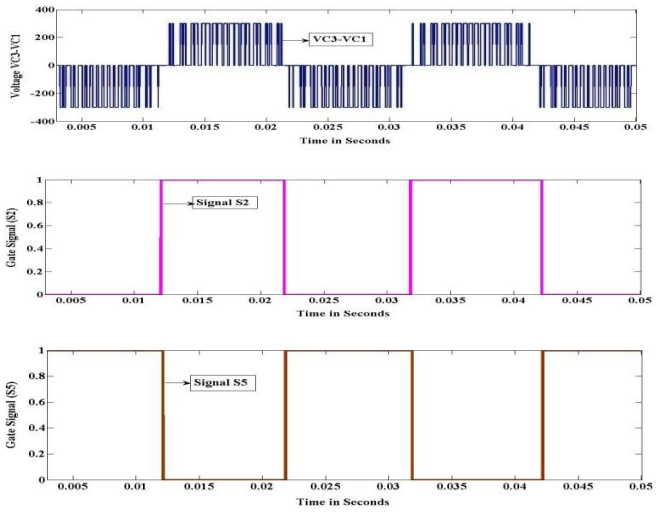

Fig 5(c):Voltage Waveforms of (VC3-VC1) and gate signals to the switches S2,S5

IV. WORKING PRINCIPLES OF ACTIVE FILTER

The transformation of the components, C_R, R, L, and C_L, from the three-phase to the single-phase equivalent circuit shown in fig.5 is based on the method described in [6].The operating principles of active filter is explained by eight operating modes in one switching cycle of the inverter output voltage pulses as shown in fig.6.The operations of each mode are described as follows

MODE 1 [t_0, t_1]

Within the rise time t_{01} of the incoming voltage pulse, the input circuit formed by C_R,R,L and C_L is designed to match the characteristic impedance of the cable Z_0 in order to minimize the reflected voltage at the interface between the cable and filter input. The values of C_R,R,L and C_L are designed to make i_{in} nearly proportional to v_{in}. That is,

$$i_{in}(t) \cong \frac{v_{in}(t)}{Z_0} \qquad (1)$$

C_L and C_R are being charged by i_{in}. At t_0, $i_{in}(t_0) = 0$ A, $i_L(t_0) = 0$ A,$v_{CR}(t_0) = 0$ A, $v_{CR}(t_0) = 0$ v, and $v_M(t_0) = v_{CL}(t_0) = 0$ v. Due to the $L\frac{di}{dt}$ effect, $i_L \approx 0$. It can be shown that

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$$v_{in}(t) = \frac{V_{dc}}{t_{r,inv}}(t_1 - t_0) \quad (2)$$

$$i_{in}(t) = \frac{V_{dc}}{R\, t_{r,inv}}(t_1 - t_0) \quad (3)$$

$$v_{CR}(t) = \frac{V_{dc}}{2RC_R t_{r,inv}}(t_1 - t_0)^2 \quad (4)$$

$$i_L(t) \approx 0 \quad (5)$$

$$v_{CL}(t) = \frac{V_{dc}}{2RC_L t_{r,inv}}(t_1 - t_0)^2 \quad (6)$$

Where, $t_{r,inv}$ is the rise time of the voltage pulses generated bythe inverter and V_{dc} is the amplitude of the inverter output pulse. The duration of this mode t_{01} is

$$t_{01} = t_1 - t_0 = t_{r,inv} \quad (7)$$

By using (3) – (7)

$$i_{in}(t_1) = \frac{V_{dc}}{R} \quad (8)$$

$$v_{CR}(t_1) \frac{V_{dc}}{2RC_R} t_{r,inv} \quad (9)$$

$$i_L(t_1) \approx 0 \quad (10)$$

$$v_{CL}(t_1) = \frac{V_{dc}}{2RC_L} t_{r,inv} \quad (11)$$

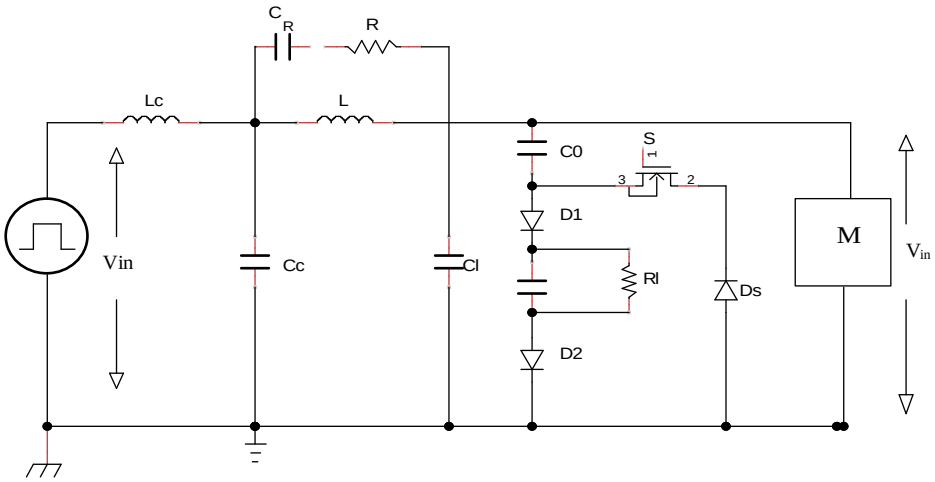

Fig 6: Single phase equivalent circuit of the proposed filter

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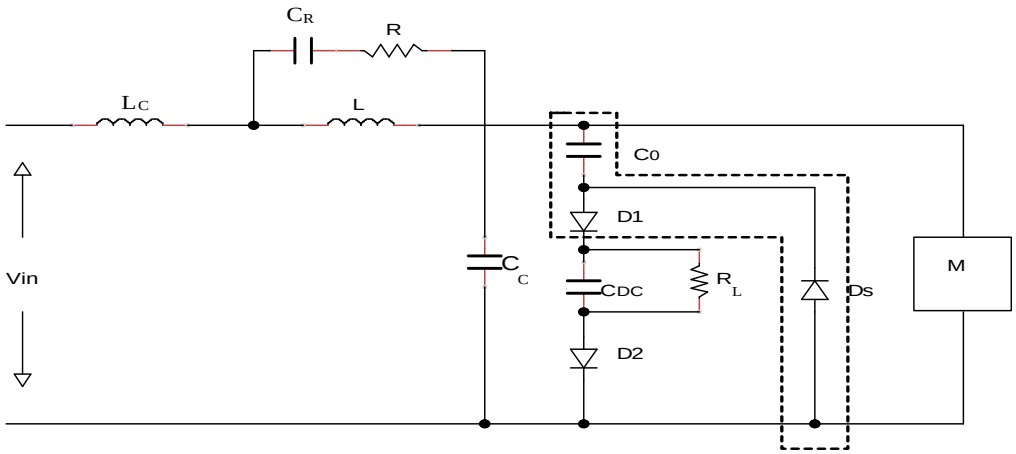

Fig 7: (a) Mode 1[t_0,t_1], Mode2 [t_1,t_2] , Mode 4 [t_3, t_4], Mode 5 [t_4, t_5], Mode 6 [t_5, t_6] and Mode 8 [t_6, t_7]

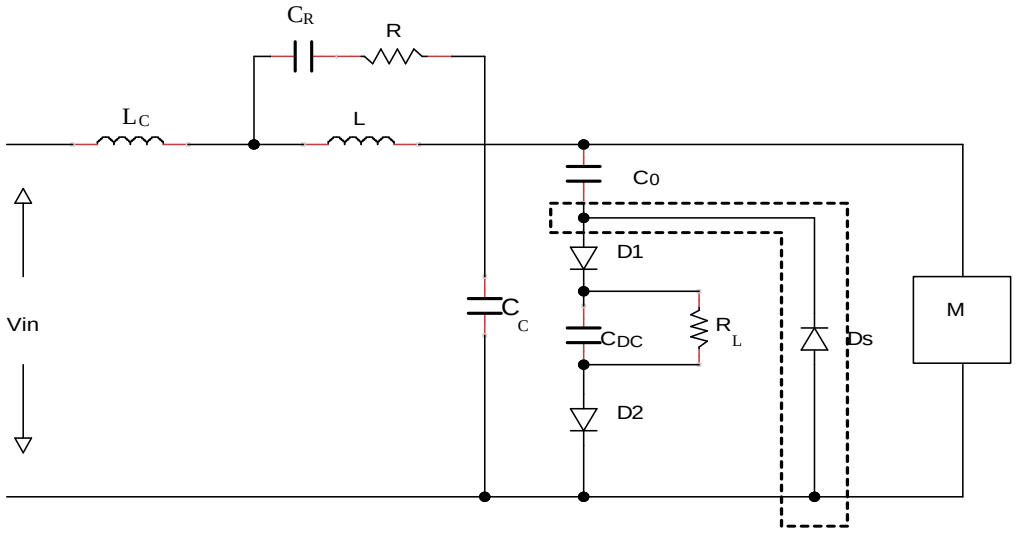

Fig 7 (b): Mode 3 [t_2, t_3]

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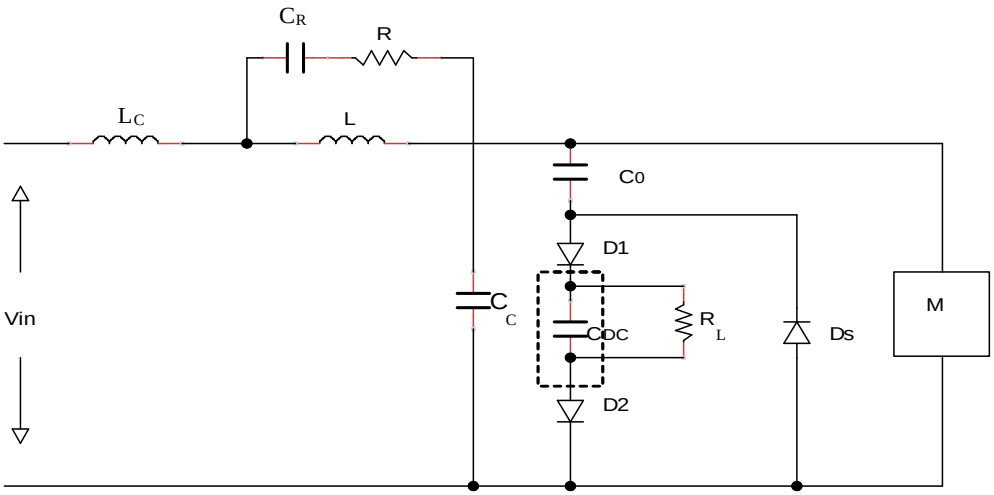

Fig 7(c): Mode 7 $[t_6, t_7]$

MODE 2 $[t_1,t_2]$

According to (1), i_{in} is nearly constant. It flows through C_R,R and L to charge up C_L. Thus

$$v_{in(t)} = V_{dc} \quad (12)$$

$$i_{in}(t) = \frac{V_{dc}}{R} \quad (13)$$

$$v_{CR}(t) = -\frac{V_{dc}}{6RLC_RC_L}t - t_1)^3 + \frac{V_{dc} - v_{CL}(t_1)}{2\,L\,C_R}(t - t_1)^2 \frac{i_{in}(t_1)}{C_R}(t - t_1) + v_{CR}(t_1) \quad (14)$$

$$i_L(t) = \frac{1}{L}\{-\frac{V_{dc}}{6RLC_RC_L}(t - t_1)^2 + [V_{dc} - v_{CL}(t_1)](t - t_1)\} \quad (15)$$

$$v_{CL}(t) = \frac{V_{dc}}{RC_L}(t - t_1) + v_{CL}(t_1) \quad (16)$$

This mode ends when $v_{CL}(t_2) = V_{CDC} - V_{C0} = V_{max}$, which is the designed maximum voltage across the motor. The duration of this mode t_{12} is

$$t_{12} = t_2 - t_1 = t_r - t_{r,inv} \quad (17)$$

Where, t_r is the designed rise time of the voltage pulses across the motor terminals based on (13) – (17)

$$i_{in}(t_2) = \frac{V_{dc}}{R} \quad (18)$$

$$v_{CR}(t_2) = -\frac{V_{dc}}{6RLC_RC_L}(t_r - t_{r,inv})^3 + \frac{V_{dc} - v_{CL}(t_1)}{2LC_R}(t_r - t_{r,inv})^2 + \frac{i_{in}(t_1)}{C_R}(t_r - t_{r,inv}) + V_{CR}(t_1) \quad (19)$$

$$i_L(t_2) = \frac{1}{L}\{-\frac{V_{dc}}{2RC_L}(t_r - t_{r,inv})^2 + [V_{dc} - v_{CL}(t_1)]t_r - t_{r,inv}\} \quad (20)$$

$$V_{CL}(t_2) = V_{max} \quad (21)$$

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MODE 3 [t_2, t_3]

The diode D_{12} conducts v_{CL} is clamped at V_{max}, as the voltage across C_0 and C_{DC} are relatively constant. $C_R$is discharging, i_L is decreasing as $V_{max} > v_{in}$ (i.e., V_{dc}). The energy stored in C_R and C_0 is transferred to C_{DC}.

Thus

$$i_{in}(t) = i_L(t) = \frac{V_{dc}-V_{max}}{L_c + L}(t - t_2) + i_{in}(t_2) \quad (22)$$

$$v_{CR}(t) = \left[\frac{L(V_{dc}-V_{max})}{L_C + L} - V_{CR}(t_2)\right](1 - e^{-\frac{t-t_2}{C_R R}}) \quad (23)$$

$$v_{CL}(t) = V_{max} \quad (24)$$

This mode ends when $i_{in}(t_3) = i_L(t_3) = 0$. By using (22), the duration of this mode t_{23} is

$$t_{23} = t_3 - t_2 = \frac{V_{dc}\,(L_c + L)}{R(V_{max}-V_{dc})} \quad (25)$$

$$v_{CR}(t_3) \approx 0 \quad (26)$$

$$v_{CL}(t_3) = V_{max} \quad (27)$$

MODE 4 [t_3, t_4]

D_{12}turns OFF naturally as $v_{CL}(t) < V_{CDC} - V_{C0}$. Resonance occurs between C_L and L. Thus

$$i_{in}(t) = i_L(t) = [V_{dc} - v_{CL}(t_3)]x\frac{\sqrt{C_R}}{L_C + L}\sin[\frac{t-t_3}{\sqrt{(L_C + L)C_R}}] \quad (28)$$

$$v_{CR}(t) \approx 0 \quad (29)$$

$$v_{CL}(t) = [V_{dc} - v_{CL}(t_3)]x\{1 - \cos[\frac{t-t_3}{\sqrt{(L_C + L)C_R}}]\} + V_{max} \quad (30)$$

This mode ends at t_4 before v_{in} starts reducing from V_{dc} to zero. The duration of this mode t_{34} is

$$t_{34} = t_4 - t_3 \quad (31)$$

$$i_{in}(4) = i_L(t_4) = 0 \quad (32)$$

$$v_{CR}(t_4) = V_{dc} \quad (33)$$

$$v_{CL}(t_4) = V_{dc} \quad (34)$$

MODE 5 [t_4, t_5]

The voltage v_{in} is reducing from V_{dc} to zero. The energy stored in C_L will be released to the cable through C_R,R and L. Thus

$$v_{in}(t) = V_{dc} - \frac{V_{dc}}{t_{f,inv}}(t - t_4) \quad (35)$$

$$i_{in}(t) = -\frac{V_{dc}}{2RC_R t_{f,inv}}(t - t_4) \quad (36)$$

$$v_{CR}(t) = \frac{V_{dc}}{2RC_R t_{f,inv}}(t - t_4)^2 \quad (37)$$

$$i_L(t) \approx 0 \quad (38)$$

$$v_{CL}(t) = V_{dc} - \frac{V_{dc}}{2RC_L t_{f,inv}}(t - t_4)^2 \quad (39)$$

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Where $t_{f,inv}$ is the fall time of the voltage pulses generated by the inverter. This mode ends when $v_{in}(t_5) = 0$. The duration of this mode t_{45} is

$$t_{45} = t_5 - t_4 = t_{f,inv} \quad (40)$$

By using (36) – (40)

$$i_{in}(t_5) = -\frac{V_{dc}}{R} \quad (41)$$

$$v_{CR}(t_5) = -\frac{V_{dc}}{2RC_R} t_{f,inv} \quad (42)$$

$$i_L(t_5) \approx 0 \quad (43)$$

$$v_{CL}(t_5) = -\frac{V_{dc}}{2RC_L} t_{f,inv} \quad (44)$$

MODE 6 $[t_5, t_6]$

The energy stored in C_L is released to the cable. Its discharging current is limited by C_R, R and L. Thus

$$v_{in}(t) = 0 \quad (45)$$

$$i_{in}(t) = -\frac{V_{dc}}{R} \quad (46)$$

$$v_{CR}(t) = \frac{V_{dc}}{6RLC_RC_L}(t - t_5)^3 - \frac{v_{CL}(t_5)}{2LC_R}(t - t_5)^2 + \frac{i_{in}(t_5)}{C_R}(t - t_5) + v_{CR}(t_5) \quad (47)$$

$$i_L(t) = \frac{1}{L}\left[\frac{V_{dc}}{2RC_L}(t - t_5)^2 - v_{CL}(t_5)(t - t_5)\right] \quad (48)$$

$$v_{CL}(t) = -\frac{V_{dc}}{RC_L}(t - t_5)^2 + v_{CL}(t_5) \quad (49)$$

This mode ends when $v_{CL}(t_6) = -V_{C0} = V_{dc} - V_{max}$. The duration of this mode is

$$t_{56} = t_6 - t_5 = t_f - t_{f,inv} \quad (50)$$

Where t_f is the designed fall time of the voltage pulses across the motor terminals.

$$i_{in}(t_6) = -\frac{V_{dc}}{R} \quad (51)$$

$$v_{CR}(t_6) = \frac{V_{dc}}{6RLC_RC_L}(t_f - t_{f,inv})^3 - \frac{v_{CL}(t_5)}{2LC_R}(t_f - t_{f,inv})^2 + \frac{i_{in}(t_5)}{C_R}(t_f - t_{f,inv}) + v_{CR}(t_5) \quad (52)$$

$$i_L(t_6) = \frac{1}{L}\left[\frac{V_{dc}}{2RC_L}(t_f - t_{f,inv})^2 - v_{CL}(t_5)(t_f - t_{f,inv})\right] \quad (53)$$

$$v_{CL}(t_6) = V_{dc} - V_{max} \quad (54)$$

MODE 7 $[t_6, t_7]$

D_{Si} conducts v_{CL} is clamped at $-V_{c0}$. The capacitor C_0 absorbs the incoming energy to maintain v_{CL} at a low level. Thus

$$i_{in}(t) = i_L(t) = \frac{V_{max} - V_{dc}}{L_c + L}(t - t_6) + i_{in}(t_6) \quad (55)$$

$$v_{CR}(t) = \left[\frac{L(V_{max} - V_{dc})}{L_c + L} - v_{CR}(t_6)\right](1 - e^{-\frac{t - t_6}{C_R R}}) \quad (56)$$

$$v_{CL}(t) = V_{dc} - V_{max} \quad (57)$$

This mode ends when $i_{in}(t_7) = i_L(t_7) = 0$. Using (55), the duration of this mode is

$$t_{67} = t_7 - t_6 = \frac{V_{dc}(L_c + L)}{R(V_{max} - V_{dc})} \quad (58)$$

Based on (55) – (58)

$$v_{CR}(t_7) \approx 0 \quad (59)$$

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$$v_{CL}(t_7) = V_{dc} - V_{max} \quad (60)$$

MODE 8 $[t_6, t_7]$

D_{Si}turns OFF naturally. Resonance Occurs between C_L and L. Thus

$$i_{in}(t) = i_L(t) = -v_{CL}(t_7)\sqrt{\frac{C_R}{L_C + L}}\sin[\frac{t-t_7}{\sqrt{(L_C+L)C_R}} \quad (61)$$

$$v_{CR}(t) \approx 0 \quad (62)$$

$$v_{CL}(t) = -v_{CL}(t_7)\{1 - \cos[\frac{t-t_7}{\sqrt{(L_C+L)C_R}}]\} + V_{dc} - V_{max} \quad (63)$$

This mode ends at t_8 before the start of the next pulse. The duration of this mode t_{78} is

$$t_{78} = t_8 - t_7 \quad (64)$$

Using (61) – (64)

$$i_{in}(t_8) = i_L(t_8) = 0 \quad (65)$$

$$v_{CR}(t_8) \approx 0 \quad (66)$$

$$v_{CR}(t_8) = 0 \quad (67)$$

This completes one incoming pulse operation. It is noted that the amplitudes of the oscillation of the motor terminal voltage in Modes 4 and 8 are small. They can be approximated by $V_{max} - V_{dc}$ which is less than 10% V_{dc}.

V. DESIGN PROCEDURE

The values of the components are designed by using the following parameters.

1. V_{dc}: DC-link voltage of the inverter.
2. V_{max} : Maximum voltage of the pulse presented at the motor terminal.
3. t_r : Designed rise time of the motor voltage from 0V to V_{max}.
4. $t_{r,inv}$; Rise time of the voltage pulses from the inverter.
5. Z_o : Characteristics impedance of the motor cable.
6. f_s : Switching frequency of the inverter.
7. $\Delta V_{C0,max}$: Maximum voltage ripple on C_0.
8. $\Delta V_{CDC,max}$: Maximum voltage ripple on C_{DC}.

The values of the components are designed as follows:

Resistor R: The value of R is designed to be the same as Z_o in order to reduce the voltage reflection in Modes 1 and 2. Therefore

$$R = Z_o \quad (68)$$

Capacitor C_L: In Mode 2, the charging current of C_L is nearly constant at $\frac{V_{dc}}{Z_o}$ and v_{CL} is increased from zero to V_{max}. Thus

$$C_L \cong \frac{V_{dc}}{Z_o}(\frac{dv_{CL}}{dt})^{-1}$$

$$= \frac{V_{dc}t_r}{V_{max}Z_o} \quad (69)$$

Capacitor C_R and inductor L : The values of C_R and L are determined by minimizing the integral square error (ISE) between the actual charging current through C_L and the designed current of $\frac{V_{dc}}{Z_o}$ over the duration of Mode 2, i.e., t_r. That is,

$$ISE = \int_0^{t_r}(i_{in}(t) - \frac{V_{dc}}{Z_o})^2\,dt$$

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$$= V^2 dt \int_0^{t_r} [(\frac{t_r + RC_R}{Rt_r}) + \frac{1}{L}(t - \frac{t^2}{2t_r})]^2 dt \quad (70)$$

Where $C_R \in [1nF, 100nF]$ and $L \in [24\mu H, 72\mu H]$ with $t_r = 1\mu s$, $R=74\Omega$ and $V_{dc=}300V$. With $C_R=5nF$ and $L=38\mu H$, the value of ISE is minimum.

Capacitor C_0 : The value of C_0 is designed by considering its maximum voltage ripple $\Delta V_{C_{0,max}}$. Current if flowing through C_0 in Modes 3 and 7. The maximum duration of Mode3, $t_{23,max}$, is considered. It is assumed that the duration is one-nth of the switching period. N is chosen between 5and 20. Thus,

$$t_{23,max} = \frac{1}{nf_s} \quad (71)$$

By considering the waveform of i_{in} between t_2 and t_3 in Fig., 6, the average current through C_0, I_{C_0}, is equal to

$$I_{C_0} = \frac{1}{2}\frac{V_{dc}}{Z_o} \quad (72)$$

Thus, the value of C_0 is$C_0 = \frac{1}{2}\frac{V_{dc}}{Z_o}\frac{t_{23,max}}{\Delta V_{C0,max}}$

$$= \frac{V_{dc}}{2nf_s Z_o \Delta V_{C0,max}} \quad (73)$$

Resistor R_L : As D_{12} only conducts in Mode 3, its average current equals to the value in (72). Since the average current through R_L is the same as the one of D_{12}.

$$\frac{1}{2}\frac{V_{dc}}{Z_o} = \frac{V_{CDC}}{R_L}\frac{1}{f_s}\frac{1}{t_{23,max}}$$

$$R_L = \frac{2nZ_o V_{CDC}}{V_{dc}} \quad (74)$$

Where $V_{CDC=2V_{max}-V_{dc}}$.

Capacitor C_{DC} : The value of C_{DC} is designed by considering its maximum voltage ripple $\Delta V_{CDC,max}$. When $i_{CDC} > 0$, C_{DC} is being charged. This happens when the filter is operating in Mode 3 (i.e., $t_{23,max}$), i_{CDC} can be expressed as,

$$i_{CDC}(t) = \frac{V_{dc}}{R}\left(1 - \frac{t}{t_{23,max}}\right) - \frac{V_{CDC}}{R_L}, t \in [0, t_{23,max}] \quad (75)$$

The duration of charging C_{DC}, t_{ch} is,

$$t_{ch} = t_{23,max}(1 - \frac{V_{CDC}Z_o}{V_{dc}R_L}) \quad (76)$$

By using (75)-(76), the average charging current of C_{DC}, I_{CDC}, is equal to,

$$I_{CDC} = \frac{1}{t_{ch}}\int_0^{t_{ch}} i_{CDC}(t)dt = \frac{1}{2}(\frac{V_{dc}}{Z_o} - \frac{V_{CDC}}{R_L})t_{ch} \quad (77)$$

Thus, the value of $C_{DC} > I_{CDC}\frac{t_{ch}}{\Delta V_{CDC,max}}$

$$= \frac{(V_{dc}R_L - V_{CDC}Z_o)^2}{2V_{dc}R_L^2 Z_o nf_s \Delta V_{CDC,max}} \quad (78)$$

VI. RESULT OF THE SIMULATION MODEL

In SIMULINK, the three phase inverter fed induction motor is designed using high frequency model of the cable and induction motor as shown in figure 7. In the inverter model, Pulse Width Modulation technique and IGBT as a switch are used.

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The #8 gauges cable is connected in between the inverter and 3hp motor, and 300V pulse voltage is applied to the motor through the cable. The length of the cable is varied for 10m, 20m,40m,60m, 80m and 100m and the phase to phase voltages are observed at the motor and inverter terminals. Fig 8 shows voltage waveform at inverter and motor terminals without filter for a cable of 20m.

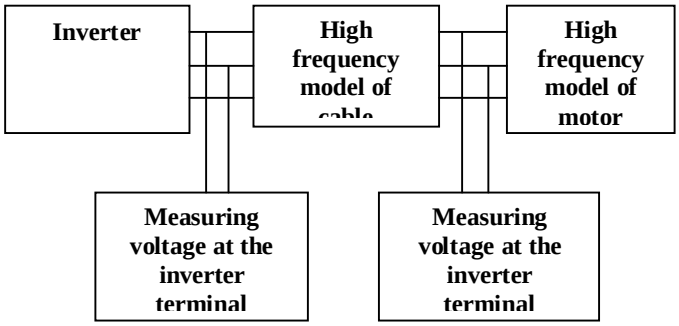

Fig 7: Model of inverter fed induction motor (Without Filter)

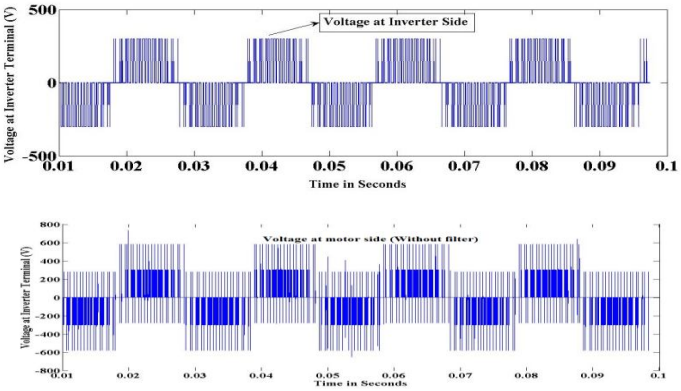

Fig 8: Voltage Waveform at Inverter and Motor terminal for 8 Cable Gauge of length 20m

The designed active filter is connected between high frequency model of cable and induction motor to avoid the overvoltage occurs at the motor terminal. Fig 9 shows the phase to phase voltage at the motor terminal for 8 gauge cable length of 20m with the proposed active filter.

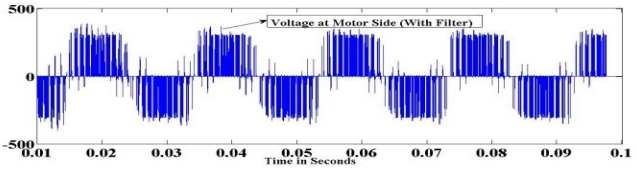

Fig 9: Voltage Waveform at Inverter and Motor terminal for 8 Cable Gauge of length 20m

VII. CONCLUSION

In this paper, a novel active filter has been proposed for PWM inverter fed induction motor. Results from the simulation have proven that mitigation of overvoltage can be achieved by the proposed filter for an induction motor drive fed by long cable. Design consideration for the proposed filter has been presented, in addition to the working principles of the active filter.

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