ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 11, November 2013

Harmonic Reduction in Cascaded Nine Level Inverter Using Genetic Algorithmic Switching Angles

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ABSTRACT: Harmonics are undesirable currents and voltages and the sources responsible for the undesirable harmonics are the nonlinear loads are rectifiers, inverters, solid state voltage regulators, cycloconverters and uninterrupted power supplies. In this paper, Total Harmonic Distortion (THD) minimization in the output voltage of multilevel inverters is discussed. In multilevel inverters with a fundamental frequency switching strategy (each switch turning on and off once per output cycle), the optimum switching angles can be selected so that the output THD is minimized. To obtain the optimum switching angles, an optimization algorithm is applied to the output voltage THD.

This paper demonstrates how the reduced harmonic distortion can be achieved for a new topology of multilevel inverters. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter, and can be extended to any number of levels. The modes of operation are outlined for nine level inverter, as similar modes will be realized for higher levels. Simulations of nine level of the proposed inverter topology along with corroborative experimental results are presented. This paper deals with the analysis and simulation of the nine level inverter. This paper presents the nine level inverter with harmonics reduction along with the reduction of switches. The harmonic reduction is achieved by selecting appropriate switching angles by Genetic algorithm. The functionality verification of the seven level inverter is done using MATLAB.

KEYWORDS: Genetic algorithm (GA), Total harmonic distortion (THD), multilevel inverter, THD minimization.

I. INTRODUCTION

Of late, high quality power is needed for medical, research and industrial applications to bring into being good quality results and for accurate evaluation. In this paper, an attempt has been made to improve the quality of power. A single phase nine level cascaded inverter with identical dc supply is designed to reduce the harmonic components of the output voltage. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of electromagnetic interference (EMI),[1][2]. The preferred output of a multilevel inverter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the inverter voltage waveform approaches a nearly sinusoidal waveform while using a low switching frequency scheme [3]. This results in low switching losses, and because several dc sources are used to synthesize the totaloutput voltage, each experiences a lower dv/dt compared to a single level inverter. Consequently, the multilevel inverter technology is a promising technology for high power electric devices such as utility applications. Multilevel voltage source inverter using cascaded inverters with separate dc sources (SDCSs), hereafter called a cascaded multilevel inverter appears to be superior to other multi-level structures in term of its structure that is not only simple and modular but also requires the least number of output voltage levels without undue increase in power circuit complexity. In addition, extra clamping diodes or voltage balancing capacitors are not necessary.

An important key in designing an effective and efficient cascaded H-bridge multilevel inverter is to ensure that the total harmonic distortion (THD) in the output voltage waveform is small enough. The level of the dc sources was assumed to be equal and constant, which is probably not to be case in application even if the sources are nominally equal. There are roughly three main types of transformer less multilevel inverter topologies, which have been studied and received

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considerable interest from high power inverter system manufactures: the flying capacitor inverter, the diode clamped inverter and the cascaded inverter. All share the same property, which is that the output filter can be dramatically reduced, and the usual bandwidth limit induced by the switching frequency can be reconsidered. Among these inverter topologies, the flying capacitor inverter is difficult to be realized because each capacitor must be charged with different voltages as the voltage level increases.

Moreover, the diode clamped inverter, also known as neutral clamped inverter is difficult to be expanded to multilevel because of the natural problem of the DC link voltage unbalancing. It consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three level converters has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The waveform obtained from the three level converters is a quasi-square wave output. Though the cascaded has the disadvantage to need DC sources, the modularized circuit layout and package are possible and the problem of the DC link voltage unbalancing does not occur, thus it can be easily expanded to multilevel. Due to these advantages, the cascaded multilevel inverter has been widely applied to such applications as High Voltage Direct Current Transmission (HVDC), static VAR compensators (SVC), stabilizer, high power motor drive and so on. This topology of inverter is suitable for high voltage and high power inversion because to its ability to synthesize waveforms with better harmonics spectrum and low switching frequency.

This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique. This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels. The modes of operation of a nine level inverter are presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on PWM with help of pulse generator. These angles are obtained from solving the waveform equations using Genetic Algorithm. Simulation of higher levels of the proposed inverter topology is carried out using MATLAB The validity of the proposed topology and the harmonic elimination method are verified experimentally for nine level inverter.

II. EXISTING SYSTEM OF NINE LEVEL INVERTER

A single phase of this inverter consists of four simple H-bridge inverters, each can produce three output voltages $+V_{dc}$, 0 or $-V_{dc}$, thus the whole inverter can produce nine voltage levels. Each H-bridge will be switched on and off only once each half cycle of the main harmonic. The harmonics produced by this way will be the main harmonic in addition to odd sine harmonics only. Figure 1 shows the structure of a single phase of this inverter. This multi-level inverter is made from several full-bridge inverters. The AC outputs for each different level of the full bridge inverters are connected in series so that the synthesized voltage waveform becomes the sum of the inverter outputs.

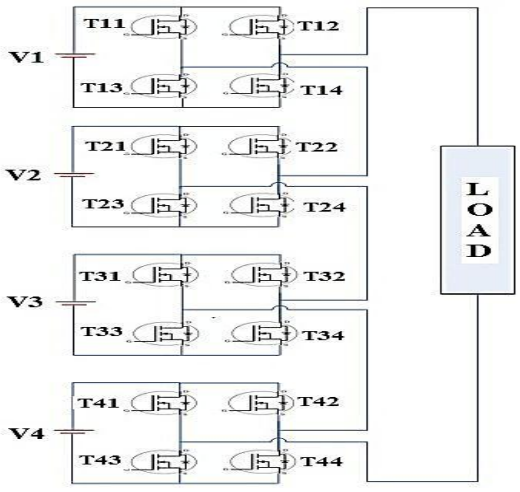

Figure 1 Conventional Nine level cascaded inverter

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The switching angles α1, α2, α3, and α4 are first calculated at different values of the main harmonics, so as to obtain zero values of the 5th, 7th, and 11th harmonics, using a selective harmonic elimination technique, [6][7]. All the undesired low order harmonics till the 11th harmonic are eliminated in the output voltage of the cascaded multilevel inverter.

III. PROPOSED SYSTEM OF NINE LEVEL INVERTER

The proposed nine level inverter has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. In this circuit, the inverter consists of four dc source. The ac terminal voltages of different level inverters are connected in series. By different combinations of the ten switches, T1-T10, each inverter level can generate four different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverters outputs. A single-phase nine level of such an inverter is shown in Figure 1.

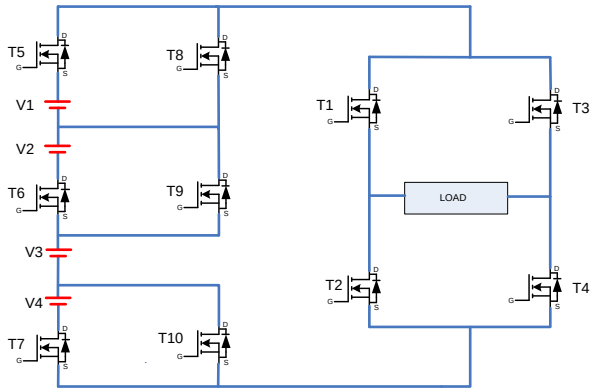

Figure 2 Power diagram of proposed Nine Level Inverter

The circuit diagram of a new nine level inverter has four main switches in H-bridge configuration T1 to T4, and two auxiliary switches T5, T6 and T7. Like other conventional multilevel inverter topologies, the proposed topology can be extended to any required number of levels. The inverter output voltage, load current, and gating signals are shown in Figure.3. The inverter can operate in three different modes according to the polarity of the load voltage and current. As these modes will be repeated irrespective of the number of the inverter levels, these modes are powering mode, freewheeling mode and regenerating mode.

CALCULATING THE SWITCHING ANGLES

The switching angles α1, α2, α3, and α4 are of the multilevel inverter are considered as variables and should be determined. V_{dc} is the voltage of the DC sources which are shown in Figure 4.13. Here, it is supposed that the voltages of all of the DC sources are equal. Each full-bridge inverter produces a three level waveform $+V_{dc}$,$-V_{dc}$ and the number of levels (L) is calculated by L = 2S+1. S is the number of DC sources that is equal to number of switching angles.

In this topology, the number of output phase voltage levels is defined by M = 2S+1, where s is the number of DC sources. Switching states of nine level inverter are summarized in table 1.

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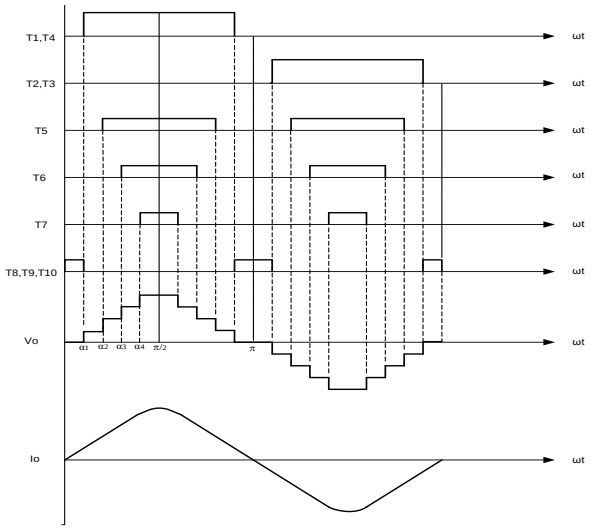

Figure 3 Output phase voltage waveform diagram

Output V_{out}	Switch State									
	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
0	0	0	0	0	0	0	0	**1**	**1**	**1**
V1	**1**	0	0	**1**	0	0	0	0	0	0
V1+V2	**1**	0	0	**1**	**1**	0	0	0	0	0
V1+V2 +V3	**1**	0	0	**1**	**1**	**1**	0	0	0	0
V1+V2 +V3+V4	**1**	0	0	**1**	**1**	**1**	**1**	0	0	0
0	0	0	0	0	0	0	0	**1**	**1**	**1**
V1+V2 +V3	0	**1**	**1**	**1**	**1**	**1**	0	0	0	0
V1+V2	0	**1**	**1**	**1**	**1**	0	0	0	0	0
V1	0	**1**	**1**	**1**	0	0	0	0	0	0
0	0	0	0	0	0	0	0	**1**	**1**	**1**

Table 1The Voltage level and switch states of proposed nine level Inverter

IV. FORMULATION OF THE PROBLEM

The Fourier series of the general quarter wave symmetric waveform, similar to that of Fig.3, with switching angles α1, α2, α3 and α4 per quarter cycle is given by

$$V_{out}(\omega t) = \sum_{m=0}^{\infty} a_{2m+1} \sin(2m+1)t \qquad (1)$$

$$\text{with } a_{2m+1} = \frac{4}{\pi} \int_{0}^{\frac{\pi}{2}} V_{out} \sin(2m+1)\omega t d\omega t$$

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$$= \frac{4}{\pi(2m+1)} \sum V_k \cos(2m+1)\alpha_k \quad (2)$$

Where $V_K$is the increase in voltage value from each switching angle to another. Assuming regular staircase waveform (V1=V2=.....=Vs=E), the amplitude of the harmonic voltage V_{2m+1} is given by the values of a_{2m+1} i.e.

$$V_{2m+1} = \frac{4E}{\pi(2m+1)} \sum_{k=1}^{S} \cos(2m+1)\alpha_k \quad (3)$$

For the nine level inverter four switching angles α1, α2, α3, α4 are available, and the first four non zero harmonics in the output line voltages of the three phase inv erter are

$$V_1 = \frac{4E}{\pi}[\cos\alpha 1 + \cos\alpha 2 + \cos\alpha 3 + \cos\alpha 4] \quad (4)$$

$$V_5 = \frac{4E}{5\pi}[\cos 5\alpha 1 + \cos 5\alpha 2 + \cos 5\alpha 3 + \cos 5\alpha 4] \quad (5)$$

$$V_7 = \frac{4E}{7\pi}[\cos 7\alpha 1 + \cos 7\alpha 2 + \cos 7\alpha 3 + \cos 7\alpha 4] \quad (6)$$

$$V_{11} = \frac{4E}{11\pi}[\cos 11\alpha 1 + \cos 11\alpha 2 + \cos 11\alpha 3 + \cos 11\alpha 4] \quad (7)$$

These four relations will be turned to be four equations that are solved to obtain the values of the switching angles α1, α2, α3, and α4; by setting:
V_1 = The required amplitude of the main harmonic,
V_5= 0, V_7= 0 V_{11}= 0.

V. GENETIC ALGORITHM TO CALCUATE OPTIMUM SWITCHING ANGELS

Genetic algorithm is a computational model that solves optimization problems by imitating genetic processes and the theory of evolution by using genetic operators like reproduction, crossover, mutation etc. Amounts of applications have benefited from the utilization of genetic algorithm. Genetic algorithm is still a novel technique for PWM-SHE technique. It imitates biological evolution by using genetic operators like reproduction, crossover, mutation, etc. Optimization in GA means maximization. In cases where minimization is required, the negative or the inverse of the function to be optimized is used. The switching angles are determined using GA.

The steps for formulating a problem and applying aGA are as follows:
1. Select binary or floating point strings.
2. Find the number of variables specific to the problem; this number will be the number of genes in a chromosome. In this application the number of variables is the number of controllable switching angles which is the number of H-bridges in a cascaded multilevel inverter. A nine-level inverter requires four H-bridges; thus, each chromosome for this application will have four switching angles, ie, (α1, α2, α3 and α4).
3. Set a population size and initialize the population. Higher population might increase the rate of convergence but it also increases the execution time. The selection of an optimum-sized population requires some experience in GA. The population in this paper has 20 chromosomes, each containing four switching angles. The population is initialized with random angles between 0 degree and 90degree taking into consideration the quarter-wave symmetry of the output voltage waveform.
4. The most important item for the GA to evaluate the fitness of each chromosome is the cost function. The objective of this study is to minimize specified harmonics; therefore the cost function has to be related to these harmonics. In this work the fifth and seventh harmonics at the output of a nine-level inverter are to be minimized. Then the cost function (f) can be selected as the sum of these two harmonics normalized to the fundamental,

$$f(\theta_1, \theta_2, \theta_3, \theta_4) = 100 \frac{|V_5| + |V_7|}{V_1} \quad (7)$$

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For each chromosome a multilevel output voltage waveform is created using the switching angles in the chromosome and the required harmonic magnitudes are calculated using FFT techniques. The fitness value (FV) is calculated for each chromosome inserting. In this case, The switching angle set producing the maximum FV is the best solution of the first iteration.

$$FV(\theta_1, \theta_2, \theta_3, \theta_4) = 100 \frac{|V_5| + |V_7|}{V_1} \qquad (8)$$

5. The GA is usually set to run for a certain number of iterations (100 in this case) to find an answer. After the first iteration, FVs are used to determine new off spring. These go through crossover and mutation operations and a new population is created which goes through the same cycle starting from FV evaluation. Sometimes, the GA can converge to a solution well before 100 iterations are completed. To save time, in this paper, the iterations have been stopped when the absolute value of the cost function goes below 1, in which case the sum of the fifth and the seventh harmonics is negligible compared to the fundamental. Note that after these iterations, the GA finds one solution; therefore, it has to be run as many times as the number of solutions required to cover the whole modulation index range. The algorithm to find the optimum switching angles is described through the flow chart shown in Figure. 4.
Comparison of switches used and THDs in the phase voltage of both the system is summarized in table 2.

VI. SIMULATION RESULTS

The feasibility of the proposed approach is verified using computer simulations. A model of the nine level inverter is constructed in MATLAB- Simulink software. Anew strategy with reduced number of switches is employed. For cascaded H bridge nine level inverter requires 16 switches to get nine level output voltage and with the proposed topology requires 10 switches. The new topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter. The schematic diagram of cascaded H bridge nine level inverter and proposed new nine level topology built in MATLAB-Simulink is illustrated in Fig. 5 and Fig. 6 respectively.

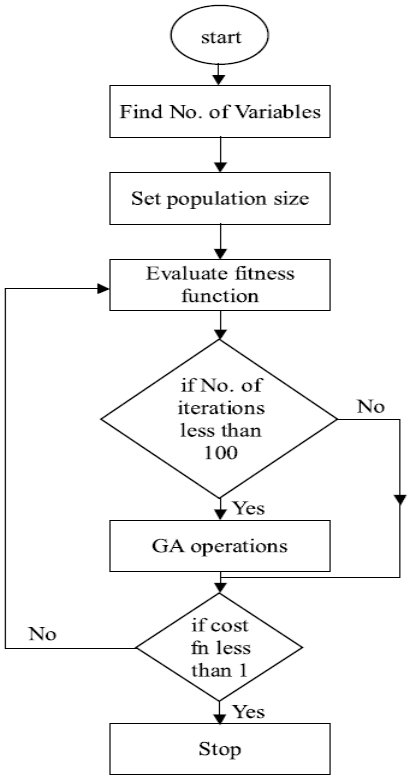

Figure 4 Flowchart of Genetic Algorithm.

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Table 2 Comparison of switches used and THDs

TYPE OF MULTILEVEL INVERTER	NO OF SWITCHES USED	THD_{Phase} (%)
CASCADED H BRIDGE (BASE PAPER)	16	10.27
CASCADED BRIDGE (Proposed)	10	9.03
% REDUCTION	37.50%	12.07%

The nine level inverter is simulated with the implementation of switch reduction scheme. The input voltage is given as 24V DC supply to the inverter and R and RL load. The output voltage waveform of nine level inverter is shown in Figure 7.

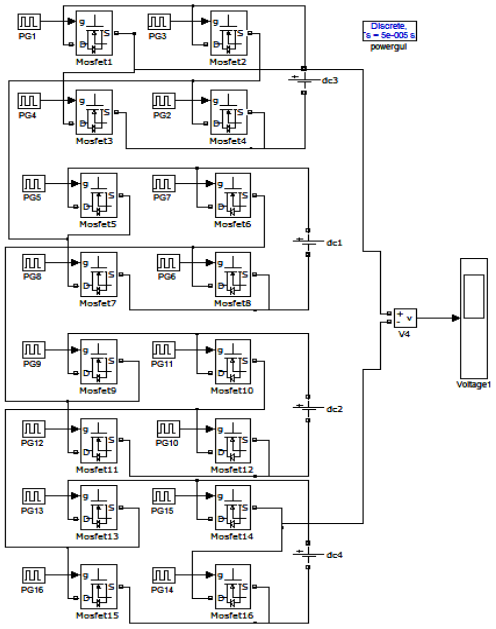

Figure 5 Simulation diagram for cascaded H bridge nine level cascaded inverter

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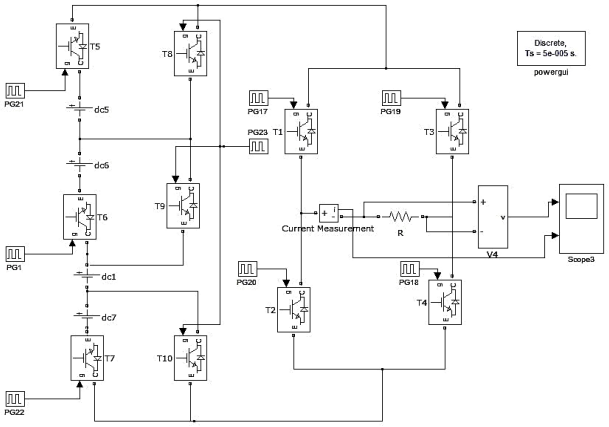

Figure 6Simulation diagram for proposed nine level cascaded inverter

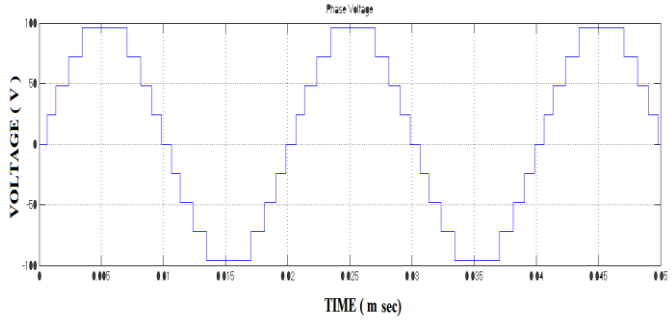

Figure 7 Output voltage waveform of nine level inverter

The output current waveform of nine level inverter on resistive load is shown in Figure 8.

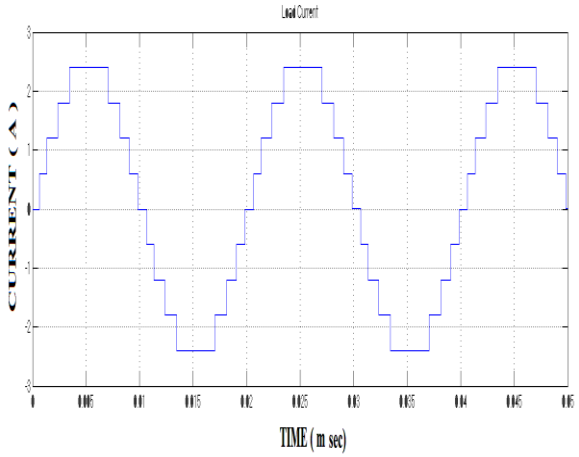

Figure 8 Output current waveform (Resistive Load)

The output current waveform of nine level inverter on inductive load is shown in Figure 9.

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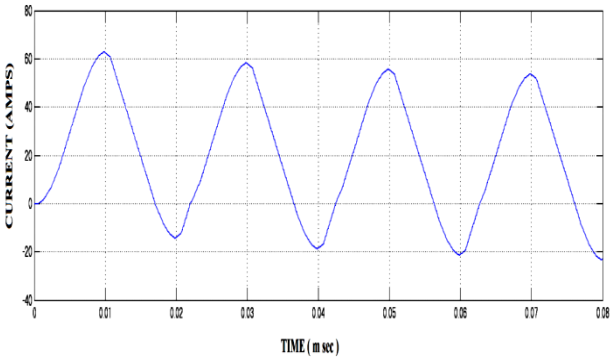

Figure 9 Output current waveform (inductive load)

The gate pulses generated from the control circuit for the switching devices shown in Figure 10.

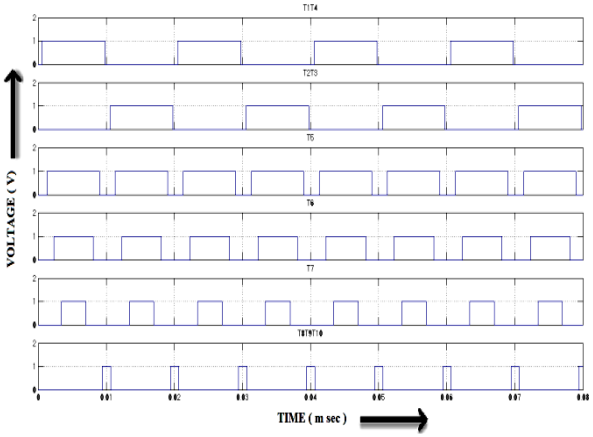

Figure 10 Gate pulse of switching devices

The frequency spectrum of output voltage is shown in Figure 11.

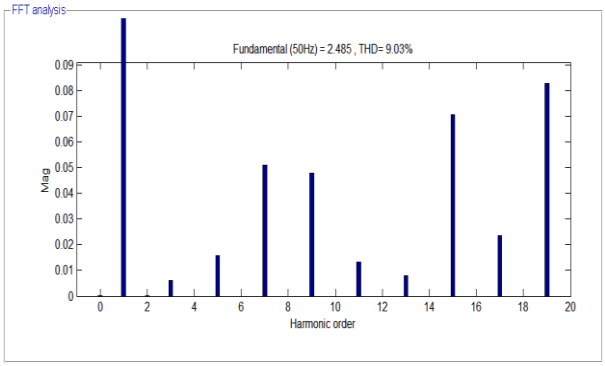

Figure 11 FFT analysis

The proposed topology has the advantage of its reduced number switches and harmonics are reduced with THD value of 9.03 at 96V is achieved. For proposed harmonic spectrum of the simulation system is as shown in the fig.11, which shows the results are well within the specified limits of IEEE standards. The results of both output voltage and FFT analysis are verified by simulating the main circuit using MATLAB.

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VII. CONCLUSION

A new family of multilevel inverters has been presented and
built in MATLAB-Simulink. It has the advantage of its reduced number of switching switches compared to conventional similar inverters. However, the high rating of its four main switches limits its usage to the medium voltage range. A Genetic algorithm switching angle is applied with the help of pulse generator and based on the theory of resultant has been applied for harmonic elimination of the new topology. Since the solution algorithm is based on solving polynomial equations, it has the advantage of finding all existed solutions, where the solution produces the lowest THD is selected. Other PWM methods and techniques are also expected to be successively applied to the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the output voltage THD.

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