



HARMONICS REDUCTION AND RIDE- THROUGH ADJUSTABLE SPEED DRIVES DURING SYMMETRICAL VOLTAGE SAG

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ABSTRACT: An increasing demand for high quality, reliable electrical power and increasing number of distorting loads may leads to an increased awareness of power quality both by customers and utilities. The most common power quality problems today are voltage sags, harmonic distortion and low power factor. Trading-off between the importance, the efficiency, the size, and the cost of any Voltage Sag Ride-Through system is the core of choosing the best topology. In addition, choosing the best topology for any give system depends on the interruption nature. For example, if the dominant interruption event is voltage sag; not a full outage, a ride-through system from the advanced hardware modification ASD's category is preferred. And vice versa, if the dominant event is a full outage, an ASD with ride through mechanism from the energy storage devices category is the best in order to maintain ride-through for long durations. In this paper, a voltage sag ride-through for an ASD from the advanced hardware modification category will be investigated. The proposed system utilizes a boost converter along with supercapacitor as an energy storage device to compensate the DC-link voltage during the symmetrical voltage sag condition. The boost convert is activated to compensate the difference between the reference voltage of the DC-link and the actual voltage once it receives a signal from the voltage sag detection system. An additional advantage of using boost converter is its ability to improve the shape of the supply currents waveforms during the steady state normal operation. Thus lower total harmonic distortion (THD) can be obtained. Based on the designed topology, simulation model in MATLAB 7.5 (Sim Power Block set) has been developed for voltage unbalance conditions with supercapacitor as an energy storage device. The designed control technique is modeled, simulated and successfully implemented in the laboratory. The extensive simulation results are provided to validate the proposed system.

Keywords: Electric Power Quality, Harmonics, Adjustable Speed Drives, Supercapacitor, THD.

I. INTRODUCTION

Power quality problem occurs as a non-standard voltage, current and frequency. The power quality has serious economic implications for customers, utilities and electrical equipment manufacturers. Modernization and automation of industry involves increasing use of computers, microprocessors and power electronic systems such as adjustable speed drives. [1-2]

Integration of non-conventional generation technologies such as fuel cells, wind turbines and photovoltaic with utility grids often requires power electronic inter-faces. The power electronic systems also contribute to power quality problem (generated harmonics). The electronic devices are very sensitive to disturbances and become less tolerant to power quality problems such as voltage sags, swells and harmonics. Voltage dips are considered to be one of the most severe disturbances to the industrial equipments. Voltage support at a load can be achieved by reactive power injection at the load point of common coupling. Due to the harmonics are occurring in the system it causes losses and heating of motor. [3-5]

In modern power systems, due to increase of non-linear loads, power quality has become a great concern. Nonlinear loads, which were only 15% of total loads in 1987, have increased to 50% in 2000 [6-7]. In the commercial industry, Copyright to IJAREEIE

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the main production line needs high quality electric power because it consists of several coupled motors working simultaneously together with precise speed. These power quality disturbances cause breaks at various workstations that require a long time to clean the machinery and resume production. [8-9]

The transient voltage variations are caused by lightning strikes, switching of power lines and capacitor banks, system faults, and large motor start-ups. Therefore, a good power quality monitoring system is essential for the commercial industries in order to decrease the downtime and increase the efficiency. Although, electric drives are sensitive to voltage distortions, they are also one of the major sources of current harmonics generation and power quality problems [9]. Electric drives draw non sinusoidal currents from the electrical power system [10, 11]. The current harmonics passing through the impedance of the power system create non-linear voltage drops and cause voltage distortions. In presence of harmonics, the load loss, eddy current loss, and other stray losses are increased. Possible problems include transformer overheating, motor failures, fuse blowing, capacitor failures, and mal-operation of controls [12].

THD is defined as the RMS value of the waveform remaining when the fundamental is removed. A perfect sine wave is 100%, the fundamental is the system frequency of 50 or 60Hz. Harmonic distortion is caused by the introduction of waveforms at frequencies in multiplies of the fundamental ie: 3rd harmonic is 3x the fundamental frequency / 150Hz. Total harmonic distortion is a measurement of the sum value of the waveform that is distorted. Harmonic distortion is caused by the high use of non-linear load equipment such as computer power supplies, electronic ballasts, compact fluorescent lamps and variable speed drives etc, which create high current flow with harmonic frequency components. The limiting rating for most electrical circuit elements is determined by the amount of heat that can be dissipated to avoid overheating of bus bars, circuit breakers, neutral conductors, transformer windings or generator alternators. [13-20]

Today, there are no clear product standards governing harmonics. IEEE 519-1992, Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems, is often referenced when discussing harmonic mitigation. However, this standard was developed to cope with harmonic issues in electrical transmission lines and power grids. IEEE 519-1992 is a systems standard which cannot be effectively applied to individual products. [21-22]

II. PROPOSED RIDE-THROUGH TOPOLOGIES

The objective of this section is to investigate the performance of an ASD's under three-phase symmetrical and unsymmetrical fault leading to balanced and unbalanced voltage sag at PCC. The proposed topology is designed by using supercapacitor as energy storage device along with boost converter across DC-Link as a ride-through alternative for ASD's.

The performance of ASD's under various fault conditions has been simulated using MATLAB Simulink Power System Block set tool box. The functional block diagram is shown in fig. 1.

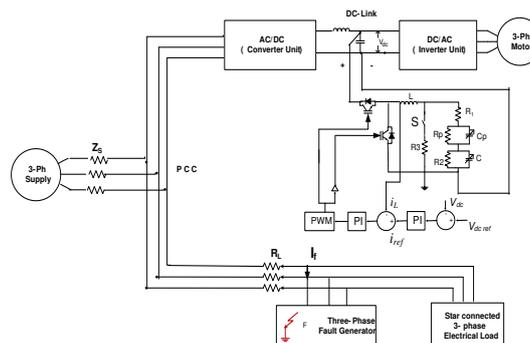


Fig. 1 Block Diagram of Proposed Technique.

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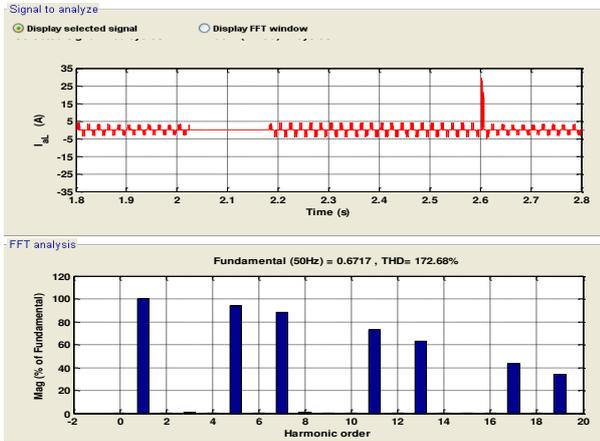


Fig. 3 Simulation Results showing three-phase source current (I_{aL}) and FFT analysis during symmetrical fault condition without providing any ride-through.

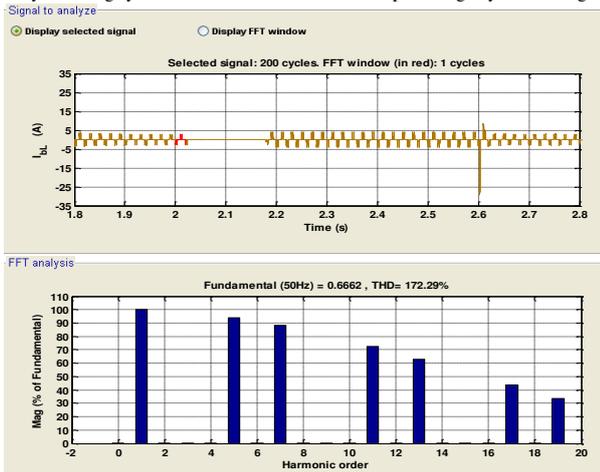


Fig. 4 Simulation Results showing three-phase source current (I_{bL}) and FFT analysis during symmetrical fault condition without providing any ride-through.

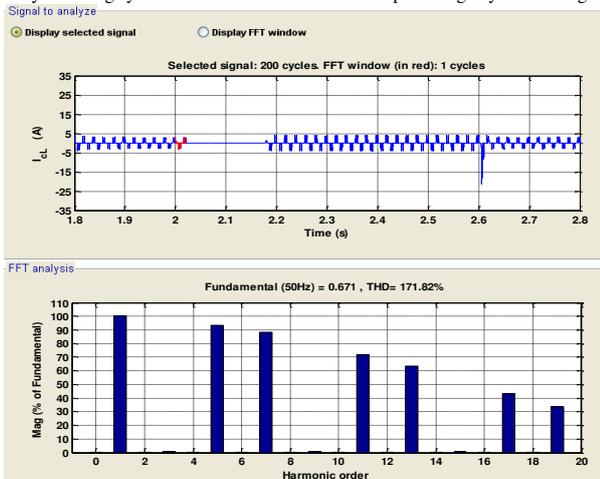


Fig. 5 Simulation Results showing three-phase stator source current (I_{cL}) and FFT analysis during symmetrical fault condition without providing any ride-through.

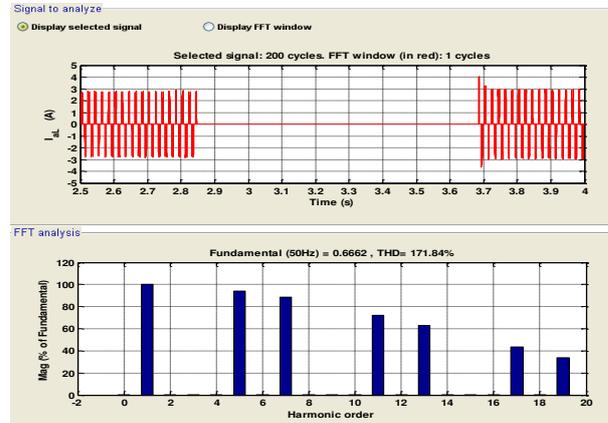


Fig. 6 Simulation Results showing three-phase source current (I_{aL}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

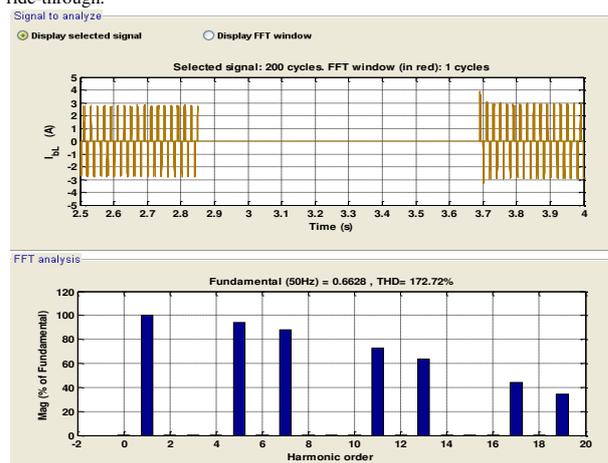


Fig. 7 Simulation Results showing three-phase source current (I_{bL}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

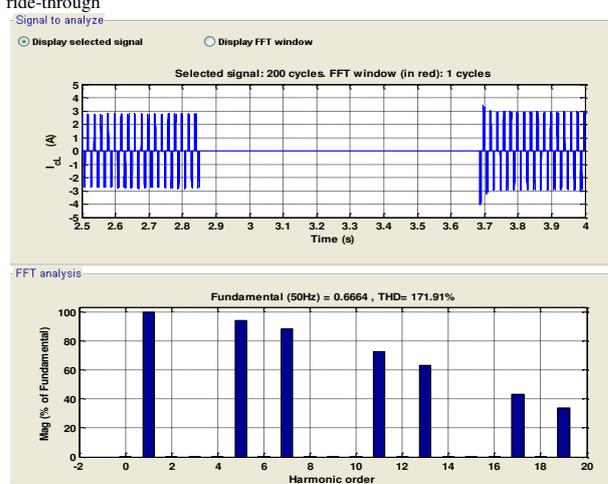


Fig. 8 Simulation Results showing three-phase source current (I_{aL}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

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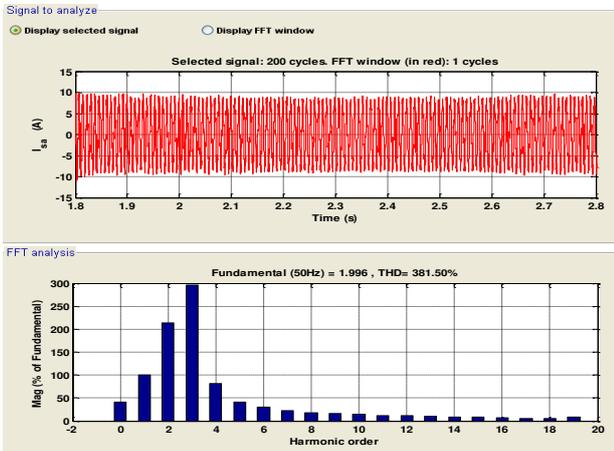


Fig. 9 Simulation Results showing three-phase stator current (I_{sa}) and FFT analysis during symmetrical fault condition without providing any ride-through.

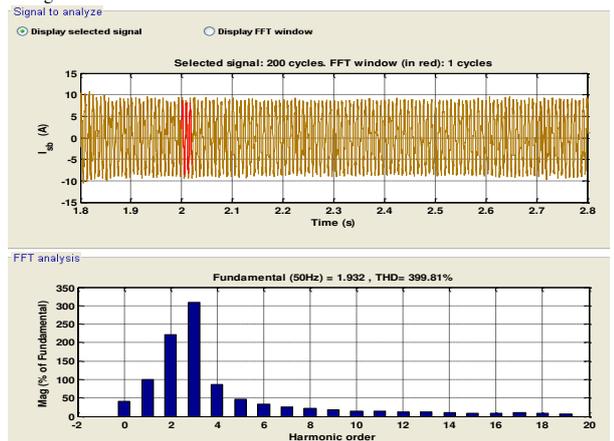


Fig. 10 Simulation Results showing three-phase stator current (I_{sb}) and FFT analysis during symmetrical fault condition without providing any ride-through.

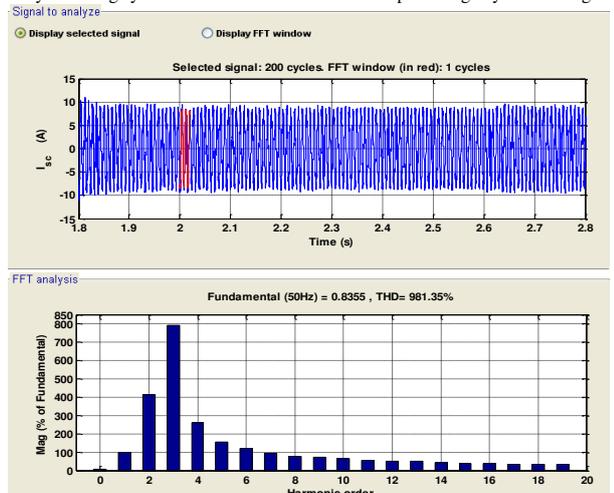


Fig. 11 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition without providing any ride-through.

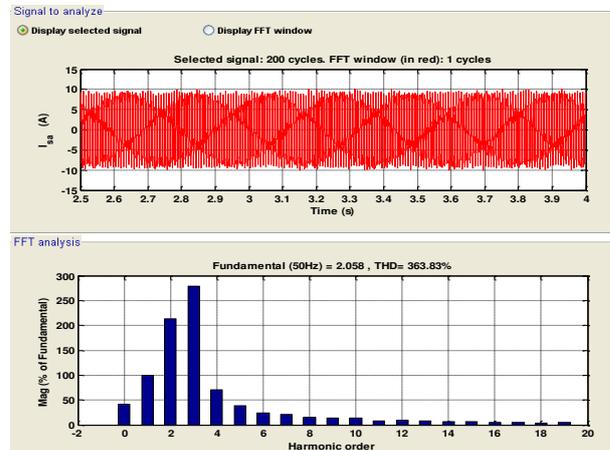


Fig.12 Simulation Results showing three-phase stator current (I_{sa}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

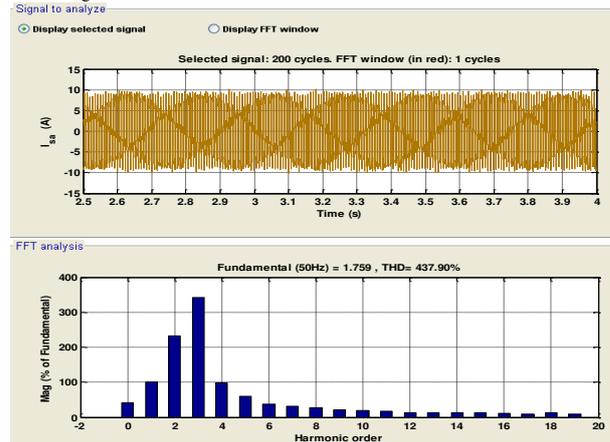


Fig.13 Simulation Results showing three-phase stator current (I_{sb}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

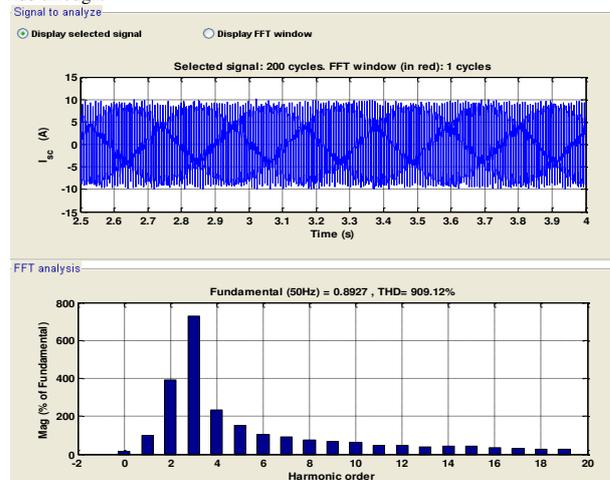


Fig. 14 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

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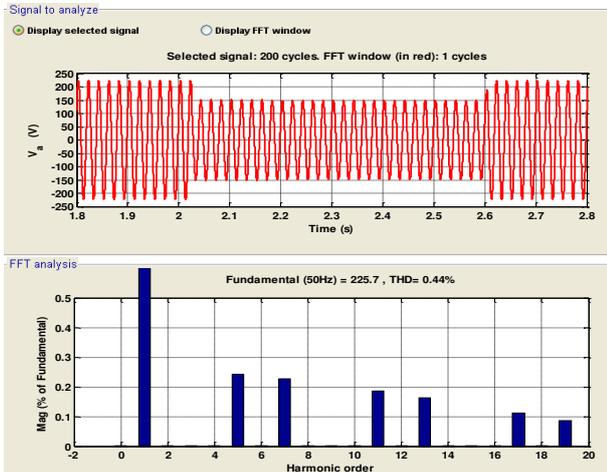


Fig. 15 Simulation Results showing three-phase stator voltage (V_a) and FFT analysis during symmetrical fault condition without providing any ride-through.

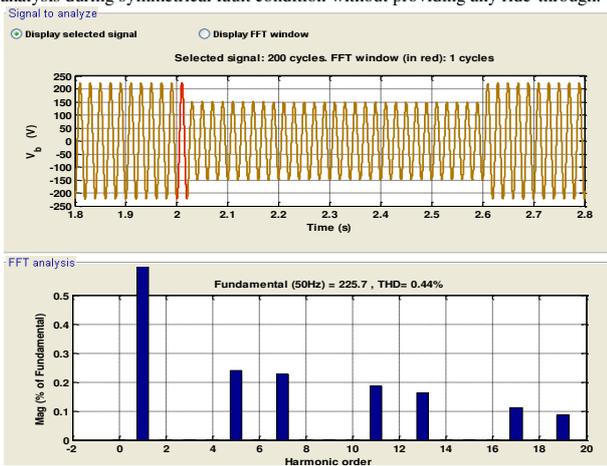


Fig. 16 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition without providing any ride-through.

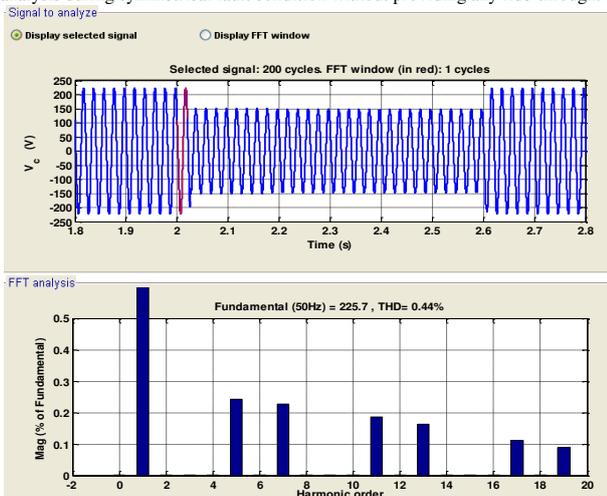


Fig. 17 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition without providing any ride-through.

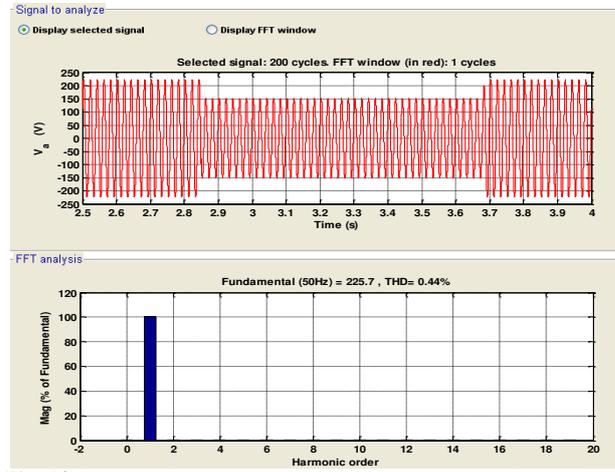


Fig. 18 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

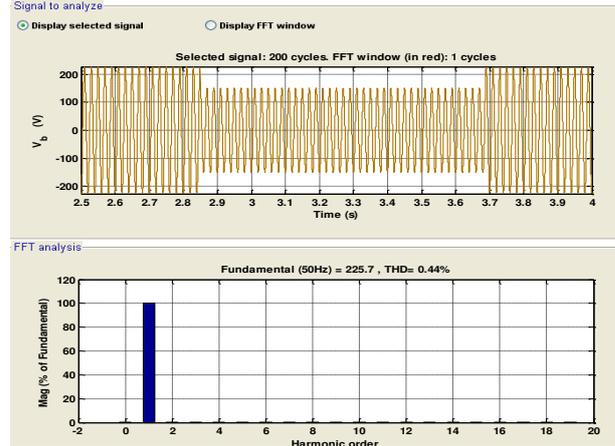


Fig. 19 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

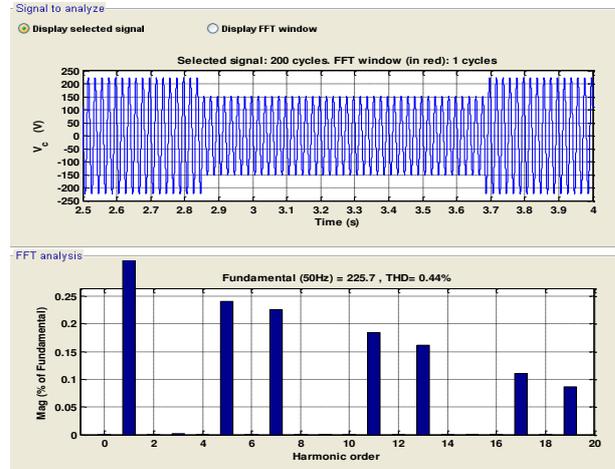


Fig. 20 Simulation Results showing three-phase stator current (I_{sc}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

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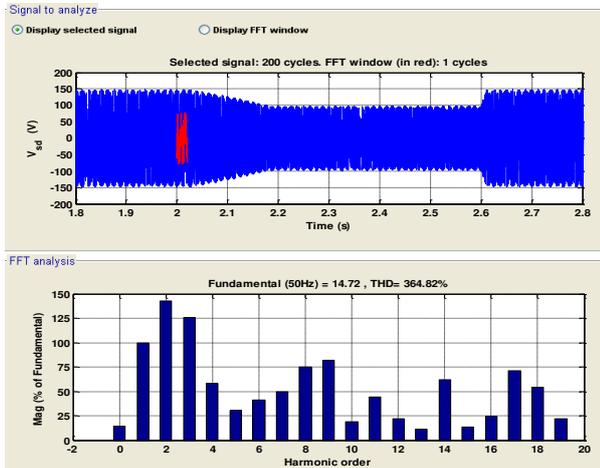


Fig. 21 Simulation Results showing three-phase stator Voltage in d-frame (V_{sd}) and FFT analysis during symmetrical fault condition without providing any ride-through.

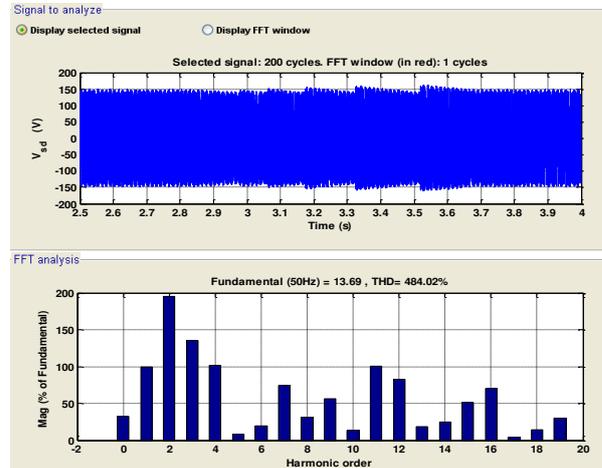


Fig. 24 Simulation Results showing three-phase stator Voltage in d-frame (V_{sd}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

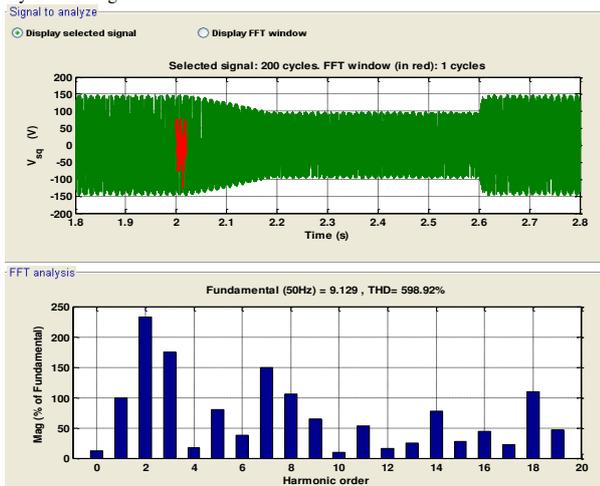


Fig. 22 Simulation Results showing three-phase stator Voltage in q-frame (V_{sq}) and FFT analysis during symmetrical fault condition without providing any ride-through.

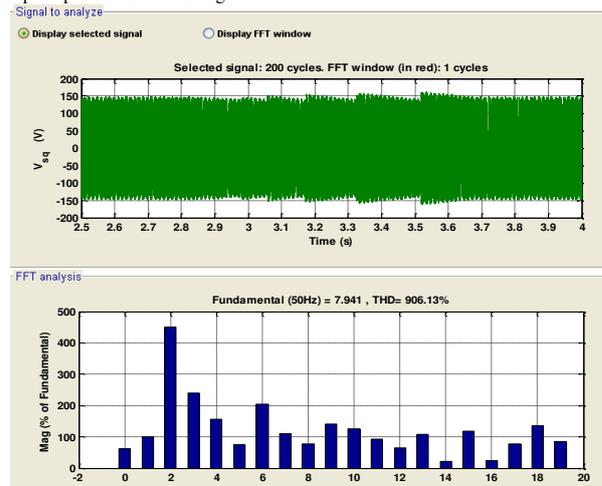


Fig. 25 Simulation Results showing three-phase stator Voltage in q-frame (V_{sq}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

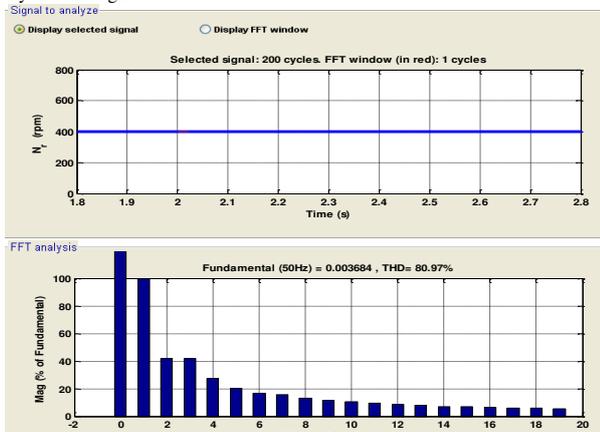


Fig. 23 Simulation Results showing rotor speed (N_r) and FFT analysis during symmetrical fault condition without providing any ride-through.

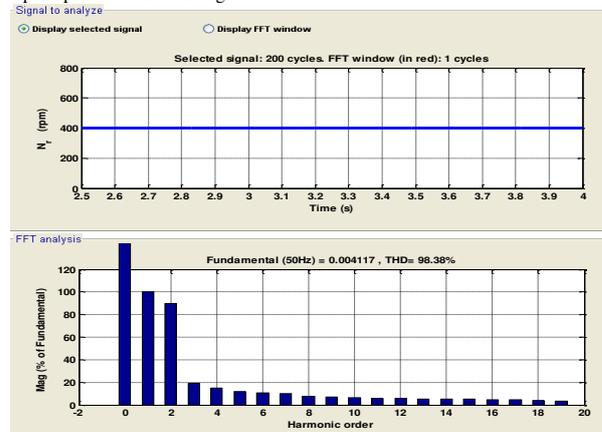


Fig. 26 Simulation Results showing rotor speed (N_r) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

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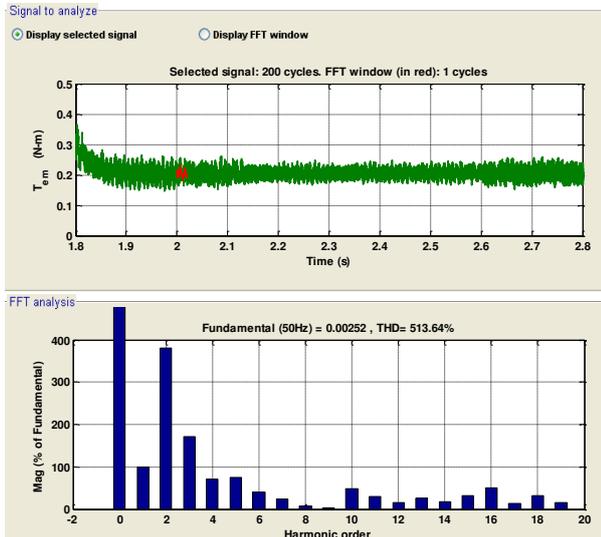


Fig. 27 Simulation Results showing Electromagnetic Torque (T_{em}) and FFT analysis during symmetrical fault condition without providing any ride-through.

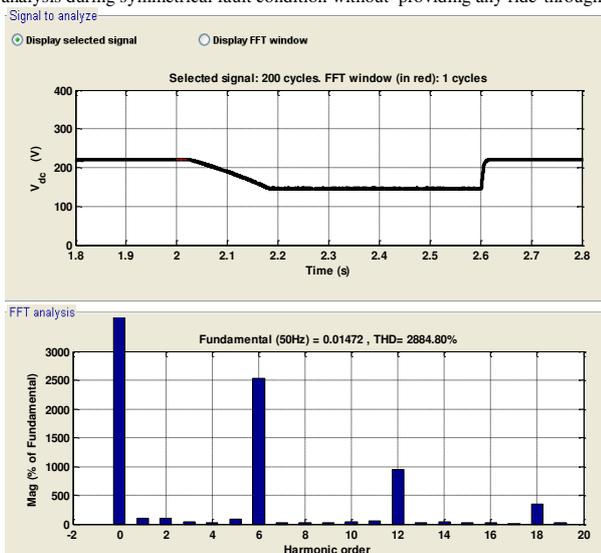


Fig. 28 Simulation Results showing DC-Link Voltage (V_{dc}) and FFT analysis during symmetrical fault condition without providing any ride-through.

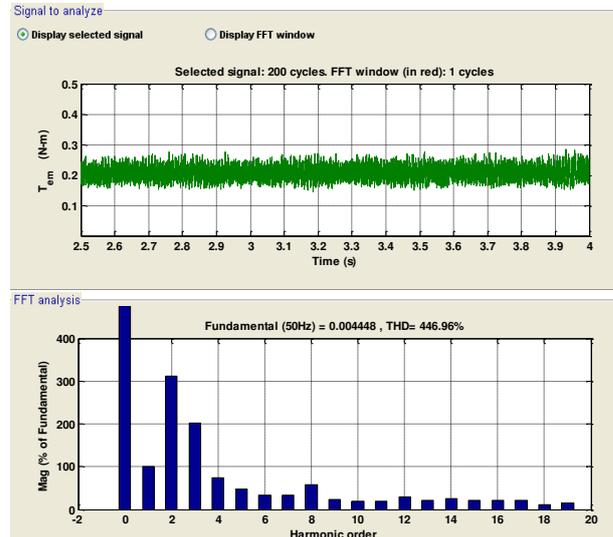


Fig. 29 Simulation Results showing Electromagnetic Torque (T_{em}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

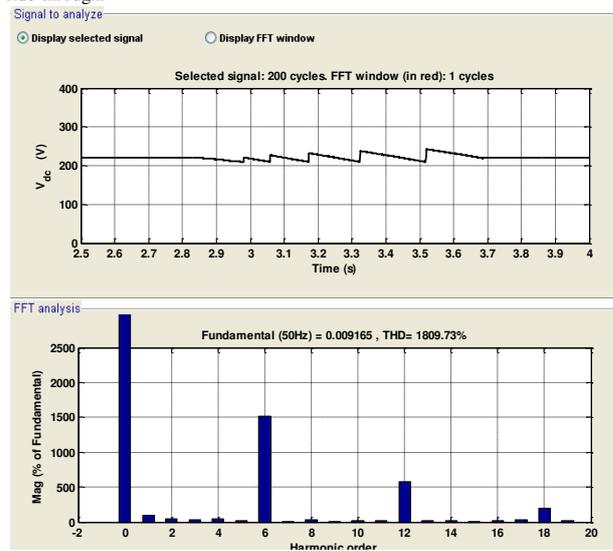


Fig. 30 Simulation Results showing DC-Link Voltage (V_{dc}) and FFT analysis during symmetrical fault condition with providing supercapacitor as ride-through.

VI. CONCLUSION

The proposed topology is capable of providing ride-through during both symmetrical and unsymmetrical voltage sags and also reduction in total harmonic distortion (THD). The effectiveness of the proposed topology has been verified by means of simulations based on MATLAB results. From these results it is clear that the supercapacitor's dynamic response is fast enough to respond to the load transient requirements and avoid the affects of the various power quality disturbances on the adjustable speed drives. The boost converter along with supercapacitor as an energy storage device maintains the DC-Link voltage thereby reduces the input inrush current. The main emphasis of this paper is that, the supercapacitor as an energy storage device may be employed during symmetrical fault condition so as to avoid the



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nuisance tripping of the ASD's and also lower the total harmonic distortion (THD). In addition, power factor correction can be established

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