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Design and Verification of Amba 3 APB Protocol by Using UVM Methodology

SONALI SANGODE, CHANDRAHAS SAHU

M. Tech (VLSI), Dept. of ET& T, SSTC, Bhilai, India

Asst. Professor, Dept. of ETC, SSTC, Bhilai, India

ABSTRACT: In these paper we have to design and verification of APB (AMBA) protocol in UVM methodology. By using this UVM Methodology gives advanced framework and building blocks to work with codes and its recognize the dynamic approach. Now, a days VLSI industries there are millions of transistors in a single chip is called system on chip (SOCs) and Intellectual Property (IP) are uses. The APB Protocols has associated with transistor signals and it indicates the clock signal, this design is created on Universal verification methodology (UVM) and also simulated and tested accurately.

KEYWORDS: ARM, AMBA FAMILY, APB, SOC Design, UVM_METHODOLOGY, Verification, VLSI.

1. INTRODUCTION

System on Chip (SOCs) designs many chips is called Advanced Microcontroller Bus Architecture (AMBA).It is an open stock chip that coordinated with all the SOCs and design in AMBA Protocol in that protocols Advanced Peripheral bus (APB) is the part of this family. It gives a lower cost terminal that enhance the lower power consumption and minimum terminal complexity. It is a lower bandwidth and it's not required for higher performance of pipelined concept, the APB has un pipe lined protocol here the signal conversions are rising edge of clock to approved the combination of APB Peripherals.

The APB Protocols rules that there is a single address single data concept or no arbiter because single master the data and address need to come on same clock cycle and each data have corresponding address. It takes minimum two clock cycle for every transfer. One of preparing the data and another for transfer the data from master to slave. The figure shows relation between APB Master and APB Slave.

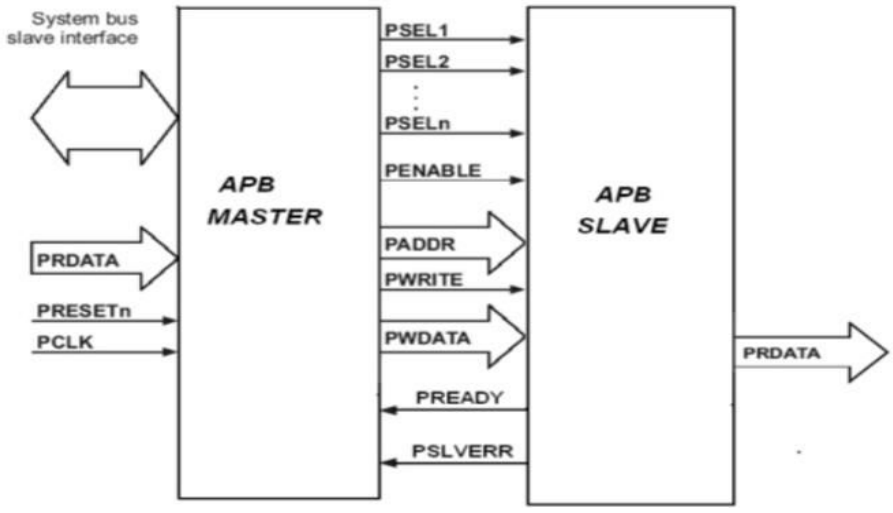

Figure 1: Relation between APB Master and ABP Slave

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APB SIGNAL DESCRIPITION

Signal	Source	Description
PCLK	Clock source	The rising edge of PCLK times all transfer on the APB.
PRESETn	Reset Source	The APB reset signal is active LOW
PADDR	APB bridge	This is the APB address bus. It can be up to 32 bit wide.
PSELx	APB bridge	Slave device is selected and the data transfer is required. There is a PSELx signal for each slave.
PENABLE	APB bridge	This Signal indicates the second and subsequent cycle of an APB operation.
PWRITE	APB bridge	Indicates the transfer direction PWRITE = 1 (write operation) And PWRITE = 0 (Read operation).
PWDATA	APB bridge	32 bit data, write data, PWRITE is high.
PREADY	Slave interface	The slave uses the signal to extend and APB transfer.
PRDATA	Slave interface	32 bit data, read data, PWRITE is LOW.
PSLVERR	Slave interface	This signal indicates a transfer failure.

OPERATIONS: Two types of Operations:

(1) Write Operation (2) Read Operation
(1) Write Operation: Two types of write operation are described in this section:
• With no wait states
• With wait states
• **With no wait states**
This operation begins with the address, write data, write signal and select signal all substitute after the rising edge of the clock. Figure shows a basic write operation with no wait states. The first clock cycle of the performance is called the Setup phase. After the following clock edge the enable signal is asserted **PENABLE**, and this indicates that the Access phase is occurred .The address, data and control signals all persist valid all over the Access phase. This performance completes at the end of this cycle. The enable signal, **PENABLE**, is affirmed at the end of the performance. The select signal, **PSELx**, also proceed LOW but the performance is to be followed instantly by another performance to the same peripheral.

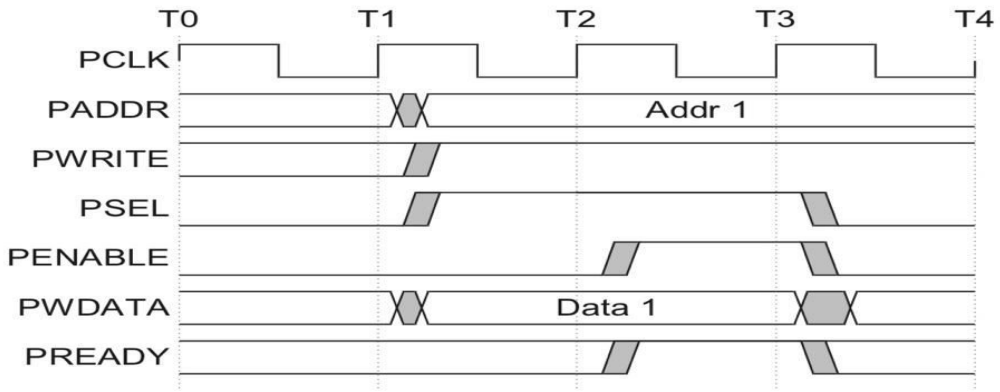

Figure 2: Write Operation with no wait states

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• **With wait states**

Figure shows the **PREADY** signal from the slave can enlarge the performance. During an Access phase, when **PENABLE** is HIGH, the performance can be enlarge by operate **PREADY is** LOW. The following signals remain constant for the further cycles:

• Address, **PADDR**
• Write signal, **PWRITE**
• Select signal, **PSEL**
• Enable signal, **PENABLE**
• Write data, **PWDATA**

PREADY can take any value when **PENABLE** is LOW. This ensures that peripherals that have a fixed two cycle access can tie **PREADY** HIGH.

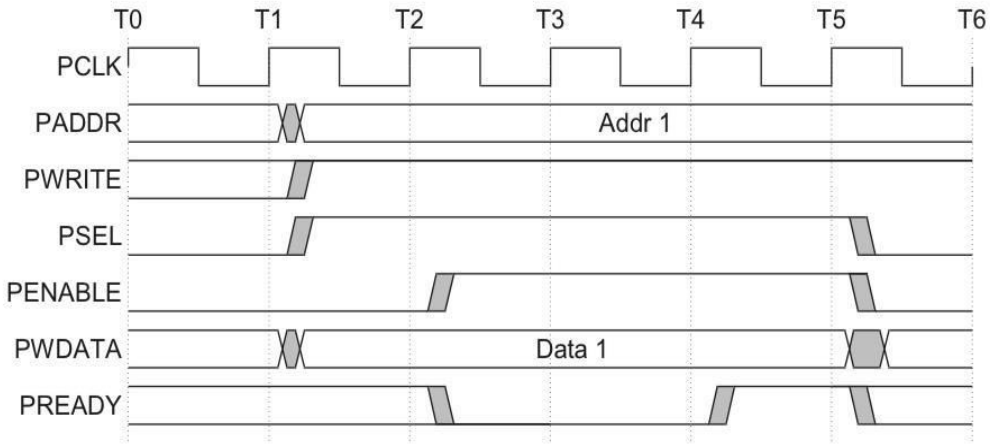

Figure 3: Write Operation with wait states

(2) Read Operation: Two types of read operation are described in this section:
• With no wait states
• With wait states
• **With no wait states**

Figure shows a read operation with no wait state. The timing of the address, write, select, and enable signals are express in Write operation . Now the slave must gives data before the end of the read operation.

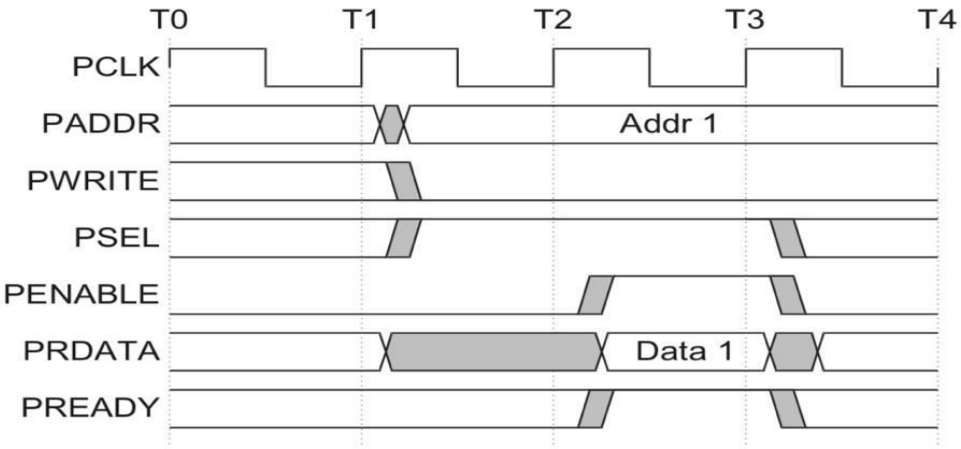

Figure 3: Read operation with no wait states

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• **With wait states**

Figure shows the **PREADY** signal can enlarge the performance. This performance is enlarged if **PREADY** is operate LOW during an Access phase. The protocol ensures that the following remain constant for the further cycles:

• Address, **PADDR**
• Write signal, **PWRITE**
• Select signal, **PSEL**
• Enable signal, **PENABLE**.

The two cycles are attach using the **PREADY** signal. Although attach any number of additional cycles, from zero upwards.

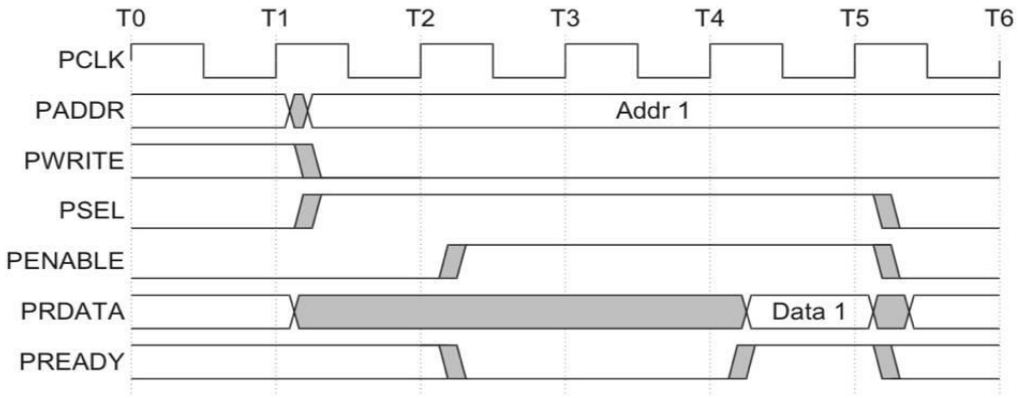

Figure 5: Read transfer with wait states

OPERATING STATES

This Operating state utilizes through the following states:

IDLE This is the default state of the APB.

SETUP If the transfer is required then the bus moves into the SETUP state, and it became a suitable select signal, **PSELx**, is declared .Only the bus remain SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

ACCESS The enable signal, **PENABLE**, is asserted in the ACCESS state. The address, Write, select and write data signals must remain stable during the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the **PREADY** signal from the slave

• If **PREADY** is held LOW by the slave then the peripheral bus remains in the ACCESS state.

•If **PREADY** is driven HIGH by the slave. Then the ACCESS state is exited and the bus returns to the IDLE state if no more transfer are required . Alternatively, the bus moves directly to the SETUP state. Figure shows the operational activity of the APB.

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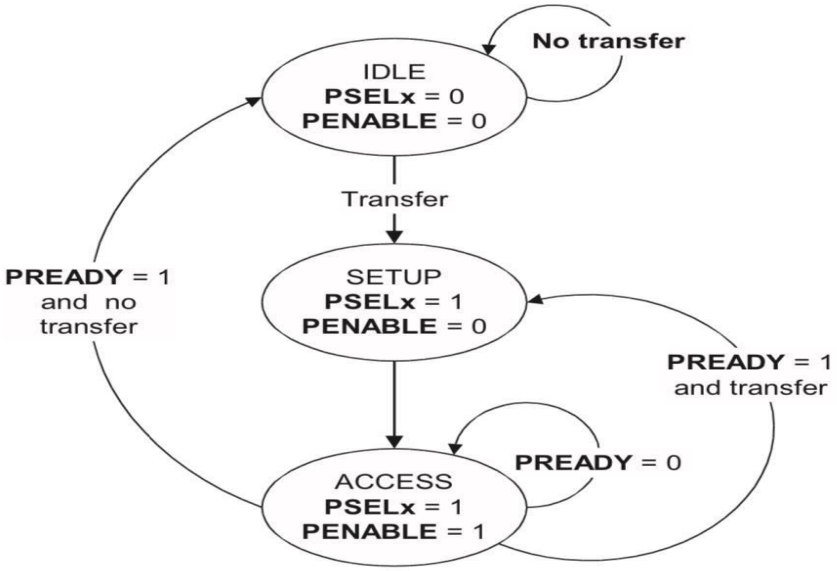

Figure 6: Design of Operating States

METHODOLOGY

The Universal Verification Methodology (UVM) and SYSTEM VERILOG (SV) is continuously take over by the environment. As SV is not sustainable in many industries and it does not prefer Macros The architecture as shown in figure 2. UVM Test bench Architecture. Here data is generated by master sequencer and send through driver to DUT. Slaves receive the data and send it to scoreboard. UVM Methodology describes that the test benches build up, design architecture, implemented components and simulated, the advantage of this SOC functional verification UVM is reached as the verification of multi master multi slave system its differentiate that the test from test bench and it's to develop the components of verification and easy to stimulus for factory mechanism.

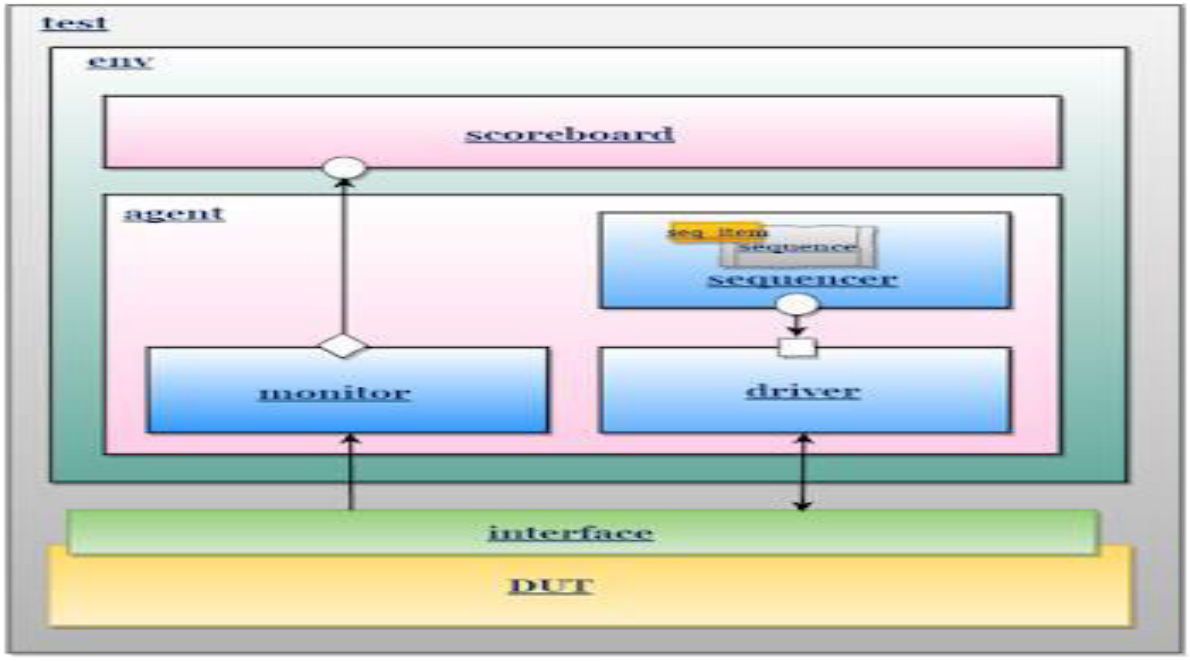

Figure: 7 UVM Test bench Architecture

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III. RESULT

In this paper we simulated APB Protocol Waveform, generates Schematic and FSM this project via QUESTASIM tool. Here, the Result is shown in below figure 5

WAVEFORM

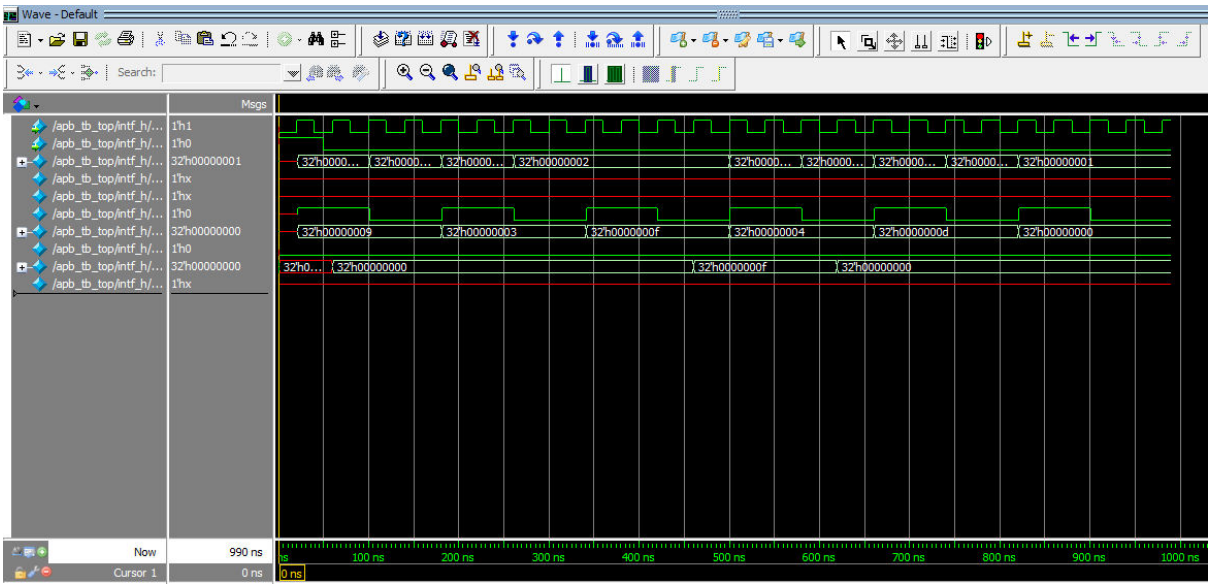

Figure: 3.1 Result of APB Protocol Waveform

FSM DESIGN

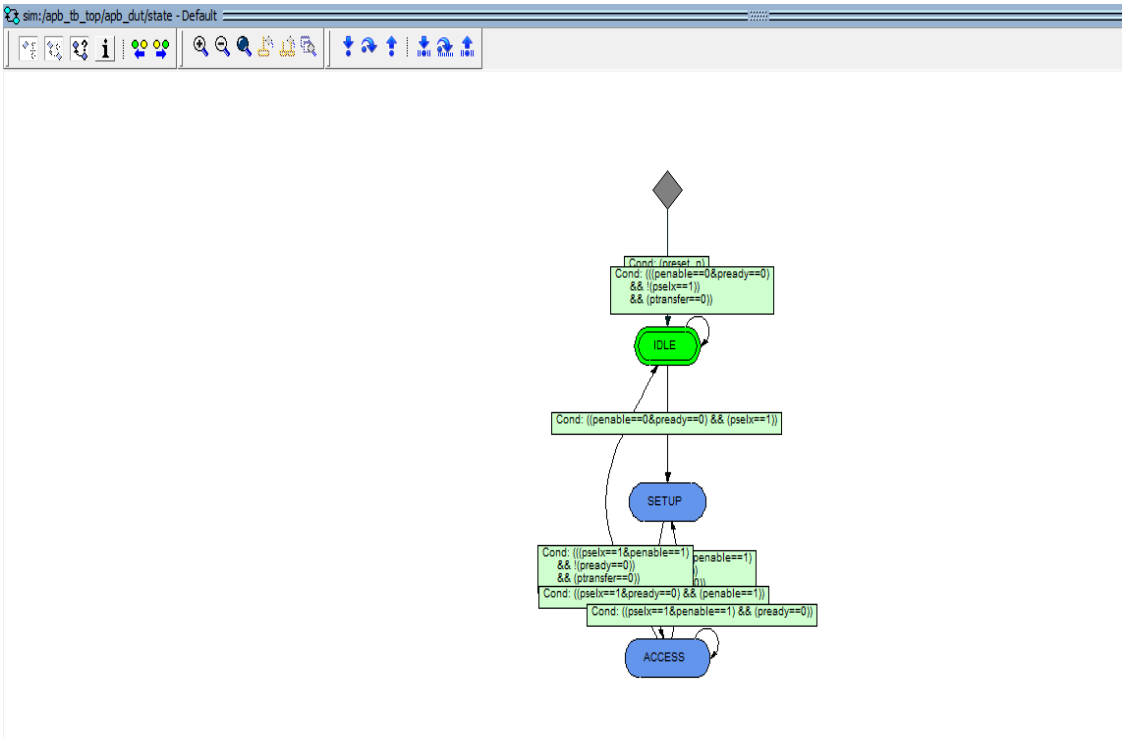

Figure: 3.2 Result of FSM Design

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SCHEMATIC DESIGN

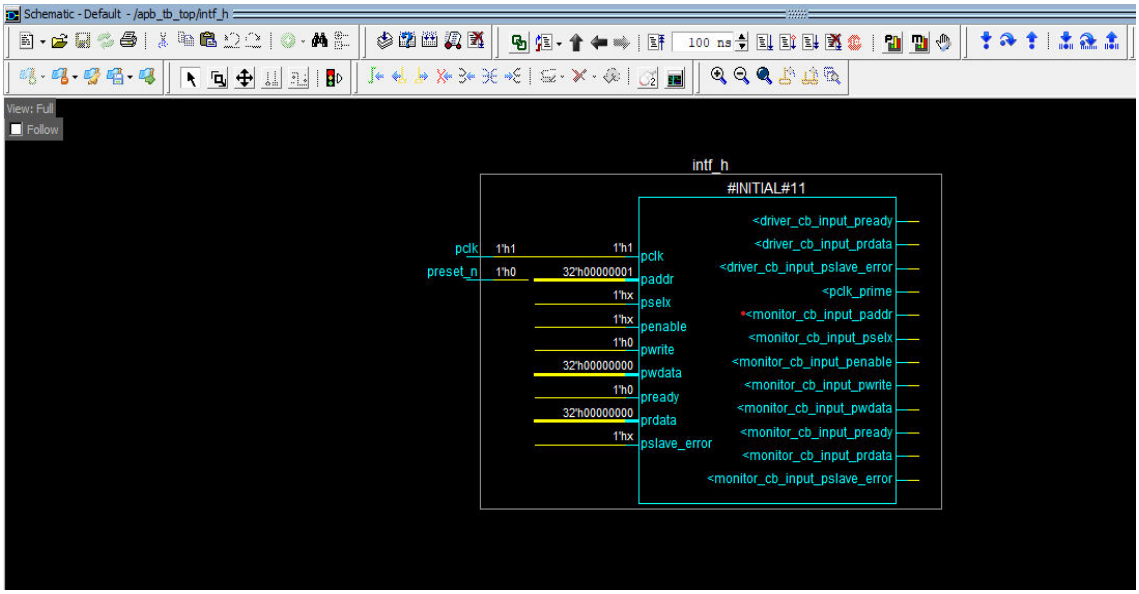

Figure: 3.3 Result of Schematic Design

IV. CONCLUSION

This paper gives an examiner of AMBA family APB Protocol is verified by using QUESTASIM. The Transcript, FSM and Schematic are added and Check the Final Result in Waveform as per the specification of Universal Verification Methodology (UVM).

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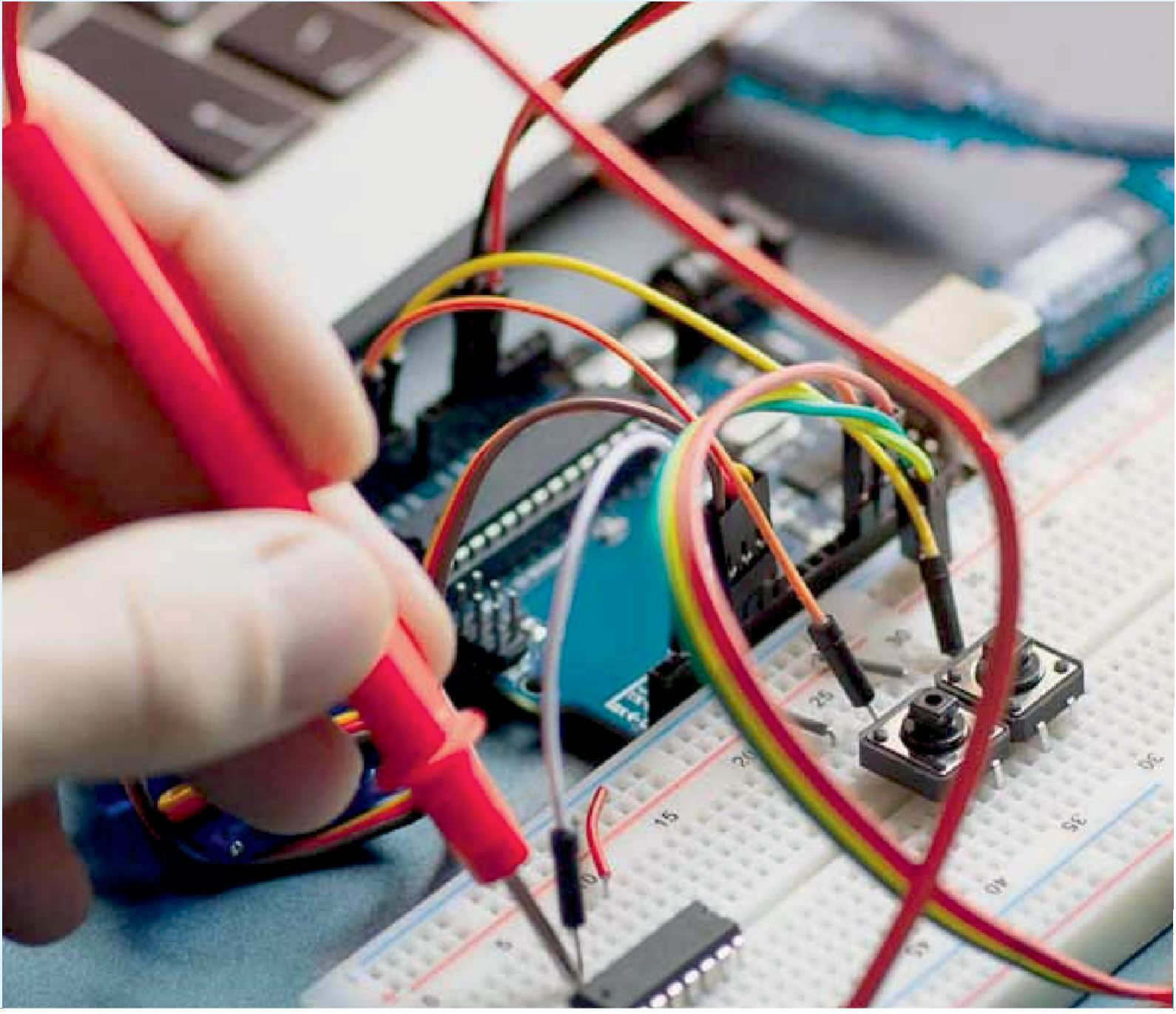

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