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# Modelling and Simulation of Fault Current Limiter in Single and Three Phase Line for Compensating Voltage Sag

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**ABSTRACT**: Voltage sag compensation is provided on both sides of the Point of Common Coupling (PCC) by using FACTS Devices (STATCOM, APF, DSTATCOM, DVR, UPFC) and FCL. The FACTS dev ices provide compensation on input side and FCL provides compensation on output side. A sensitive load is considered at output side of PCC. This paper presents a component called Fault Current Limiter (FCL) in three phase lines. The main objective of the designed component is to protect the sensitive load from the shunt faults. The compensation is being provided at output side of PCC. Load voltage reduces upon the occurrence of shunt fault. The planned structure prevents voltage sag and counter balance the phase-angle of the PCC once fault prevalence. As a result, different feeders which are interlinked to the sub-station PCC can have attentive power quality. During this paper a high performance 3-phase fault current electrical model is planned. The analysis and design is carried out in MATLAB with SIMULINK.

**KEYWORDS**: Sag, FCL, PCC, Three phase fault, single phase fault.

## I. INTRODUCTION

With the growing demand of electrical energy, there is a great desire for improving power quality of power system. Due to the rapid changes in development, the power system network became complex. Common power quality problems that appear in the network like voltage sag and malfunctioning of control equipment etc., affect the power transfer capability of the transmission and distribution system. With increase in sensitive loads in the network voltage sags creates a problem in the operation of equipment [1]. Voltage sag problems are predominant in the buses which are connected to radial feeders results in loss of voltage quality [2, 3]. It is a well-established fact that short circuit faults are major concerns for voltage sags in the system. Different topologies were proposed in [4] and [5] to improve power quality by controlling voltage sags in the networks. A new bridge type fault current limiter was proposed by Fei et.al. [6] for three phase systems and is based on self turn off devices. The dynamic voltage restorer (DVR) is also one of the most commonly used device voltage sag compensation in literature which injects the compensated voltage with magnitude and phase angle in series with the distribution feeders [7,8]. During the fault the voltage sag is proportional to the short circuit current level. The levels of fault current in different places have often exceeded the withstand capacity of existing power system equipment. Due to this the stability and reliability of the power system will be reduced [9]. Thus, the fault current of the power system is limiting to a safe level can greatly reduce the risk of failure to the power system equipment due to high fault current flowing through the system. Prediction of voltage sags in Industrial systems with highly reliable data for sensitive loads is discussed in [10] by Becker C., et. al. which proposed a new chapter in IEEE std 493. The levels of fault current are controlled by super conducting fault current limiter (SFCL) due to their variable impedance characteristics but the cost of super conductors is high. Therefore, the super conducting coil is replaced with non-superconducting coil in the FCL. The non conducting coil exhibits power loss which is negligible as compared with the total power provided by the radial feedersThis can also be attributed to the concern over power quality (PQ) as FCLs can be used to mitigate voltage sags caused by faults. For an exceptionally dependable power supply, the fault current limiter (FCL) is turning into a fundamental part in advanced based power system network. The current-constraining device is obliged to be acquainted into the power system network to enhance the fault current presence from climbing to its full prospective worth. This can additionally be credited to the more

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concern over power quality (PQ) as FCLs might be utilized to relieve voltage sags brought on by faults These will abstain from updating switchgears throughout framework development and enhance the PQ conveyed to customers. FCLs are required to give a constrained and maintained short circuit current present through the fault/flaw for a sufficient time (e.g., 1s) to empower legitimate coordination of defensive relays in optimal protection schemes

## II. PROPOSED SYSTEM OPERATION

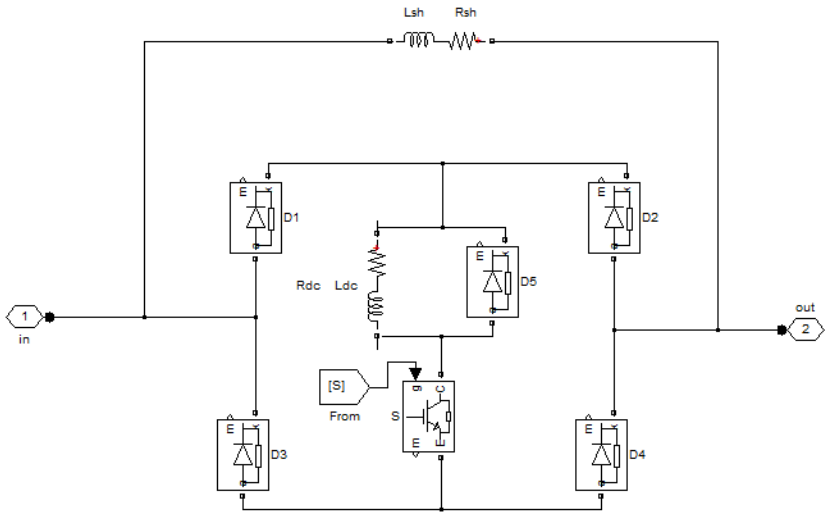


Fig 1 Proposed FCL technology

As Fig. 1 depicts the schematic diagram of proposed FCL topology which is comprised based on two following parts 1) One is bridge part that contains a un-controlled rectifier form in bridge manner as a coordination of small dc limiting reactor (Ldc). (Note here internal resistance (Rdc) is engaged too), a power electronic switch (may be IGBT or GTO) with a supportive diode for freewheeling action (D5). 2) Another component is shunt branch, acts as a limiter for enhancing the fault currents; it involves a shunt resistor and a shunt inductor (Rsh + iLsh). So many researchers introduced some structures for this type of applications [10], [11], [12] in that preferred more numbers of switching devices at bridge model instead of one power-electronic switch inside the bridge configuration. For this power electronic system requires a more complicated control scheme as well as more operation delay (turn off point at first zero cross-over), Ldc has a high value to excavate the fault current in between the fault occurrence period and thyristor turn-off period properly.his substantial estimation of Lprompts a respectablvoltage drop on the FCL and the power loss misfortunes including ac power loss influences to misfortunes on the shunt impedance as well as dc reactor loss component (that is non super-conductor) in the ordinary condition. By utilizing the semiconductor switch within the proposed structure and its quick operation, it is conceivable to pick a little esteem for Ldc to avert serious di/dt at the start of the fault event. Nowadays, high evaluating semiconductor switches are accessible in practice. Moreover, utilizing a self-turn-off power electronic switch rather than thyristors in the proposed structure prompts higher expense [13]-[17]. From a power loss perspective, in the typical condition, the proposed FCL has the somewhat loss on the rectifier topology, the semiconductor switch, and Rdc. Every diode of the rectifier topology is ON in half period of a cycle, while the semiconductor switch is constantly ON. In this manner, the loss component of this FCL in the ordinary operation could be ascertained.

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**TABLE I: SYSTEM PARAMETERS**

| | | |
|---|---|---|
| Source Side Data | Power Source | 20kV, 50Hz, X/R ratio: 5<br>Total impedance: 1.608 Ω |
| | Transformer | 20kV/6.6kV, 10MVA, 0.1pu |
| Distribution Feeders Data | Feeder F1 | j0.314 Ω |
| | Feeder F2 | j0.157 Ω |
| FCL Data | DC Side | $L_{dc}$ = 0.01H, $R_{dc}$ = 0.03 Ω<br>$V_{DF}$ = 3V, $V_{SWF}$ = 3V, $I_m$ = 0.6kA<br>Switch type: IGBT |
| | Shunt Branch | $L_{sh}$ = 0.08H, $R_{sh}$ = 5 Ω |
| Load Data | Sensitive Load | 10+j5.7 Ω |
| | Load of F2 | 15+j31.4 Ω |

## CONTROL STATERGY

Figure 5 shows the control circuit of the FCL. In the normal operating condition of the power system, IGBT is turned ON and the line current (iL) flows through “D1, Ldc, IGBT, D4” and “D3, Ldc, IGBT, D2” in positive and negative alternatives, respectively. So, Ldc is charged to the peak of the line current and behaves as a short circuit. Using semiconductor devices and a small dc reactor cause a negligible voltage drop on the FCL. During fault condition, Idc become greater than the maximum permissible current Im. The control circuit detects it and turns the semiconductor switch off. So the bridge retreats from the feeder, and the shunt impedance enters the faulted line and limits the fault current. At this moment, the freewheeling diode discharges Ldc. In fact, the freewheeling diode is used to provide a free route for the dc reactor current when the semiconductor switch is OFF After the fault is removed, while the semiconductor switch is OFF, shunt impedance will be connected in series with the load impedance. Therefore, line current will be reduced instantaneously. To detect this instantaneous reduction of line current, iLis compared fault current (If) with that can be calculated from

$$I_f = \frac{|V_{PCC}|}{|R_{sh} + j\omega L_{sh}|}$$

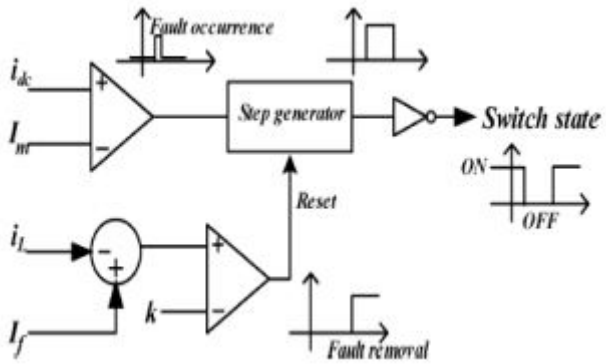


Fig 2: Control Circuit for FCL

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## III. SIMULATION AND RESULT

Three single phase sources are taken for simulation and the combined voltage wave form at PCC during the three phase fault created at t=0.1 sec to t=0.2 sec is plotted in Figure 3, Figure 4shows the instantaneous power in first phase of the system at PCC with fault condition.

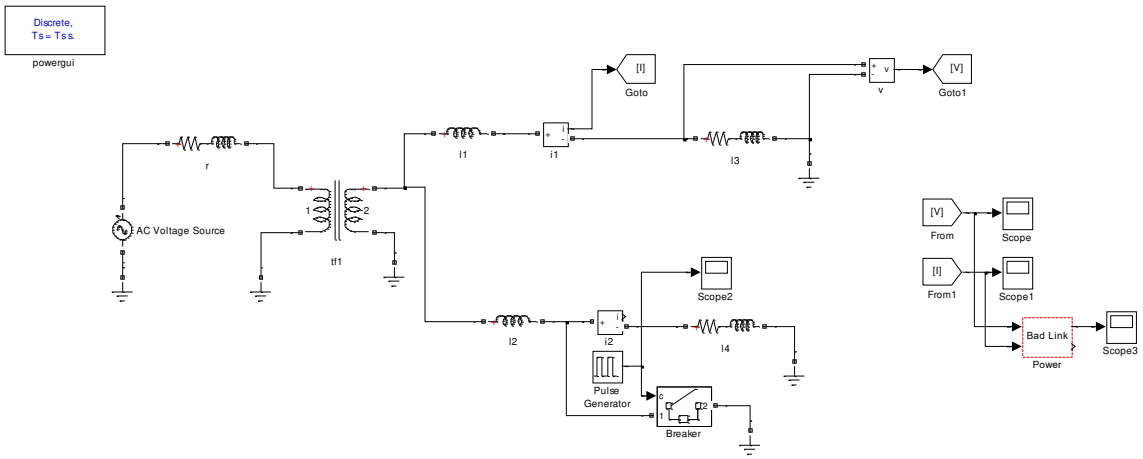


**Fig. 3 Simulink circuit of PCC without FCL**

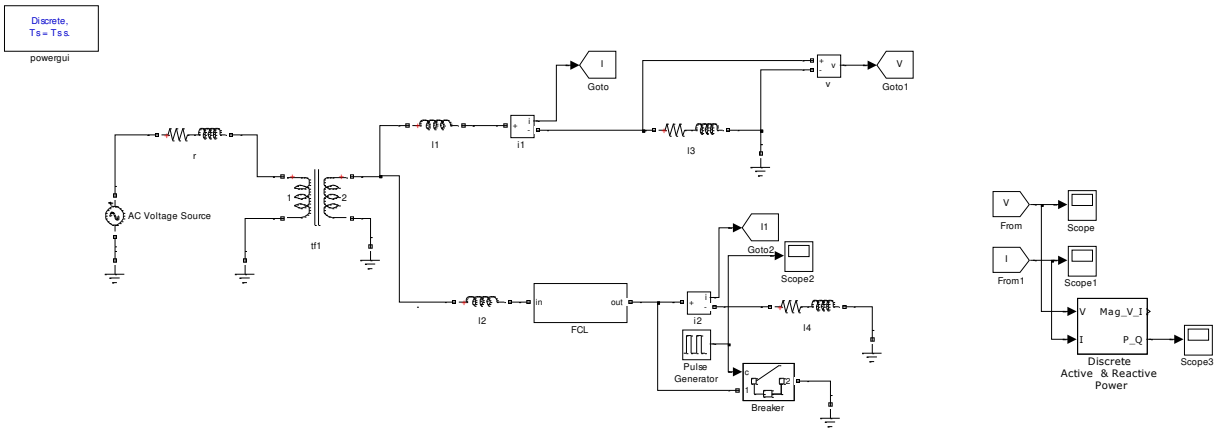


**Fig. 4MATLAB/Simulink of the proposed circuit**

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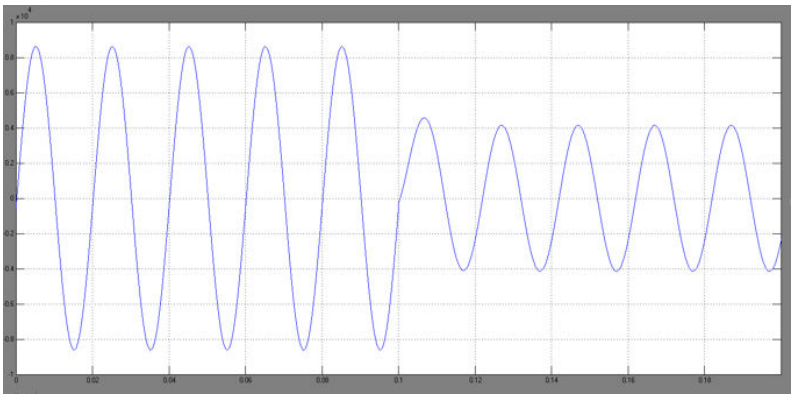

Fig. 5 PCC Voltage without FCL

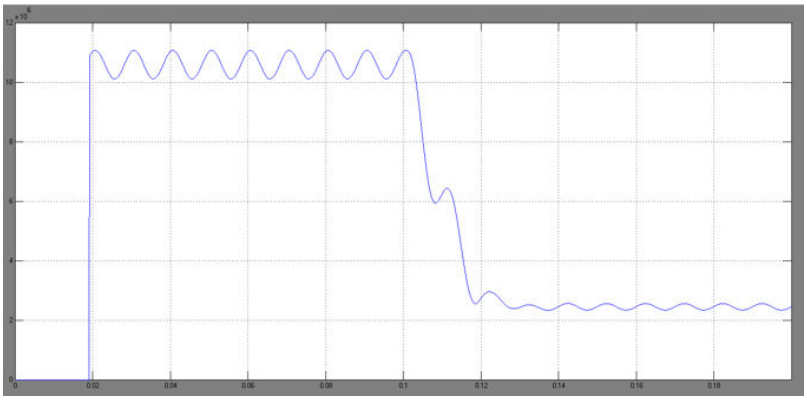

**Fig. 6**Single-phase instantaneous power of the sensitive load without FCL

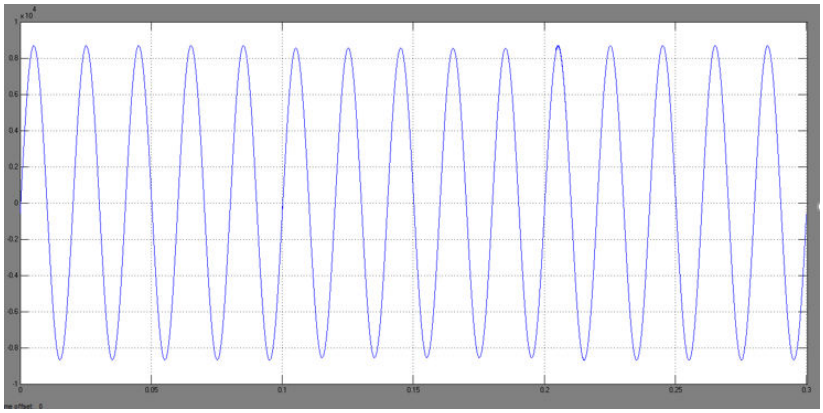

Fig. 7 PCC Voltage with the Proposed FCL.

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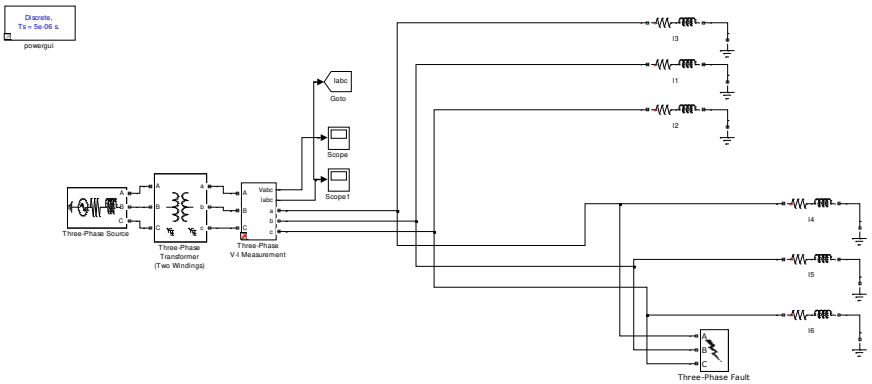


**Fig. 8 Simulink circuit of PCC without FCL**

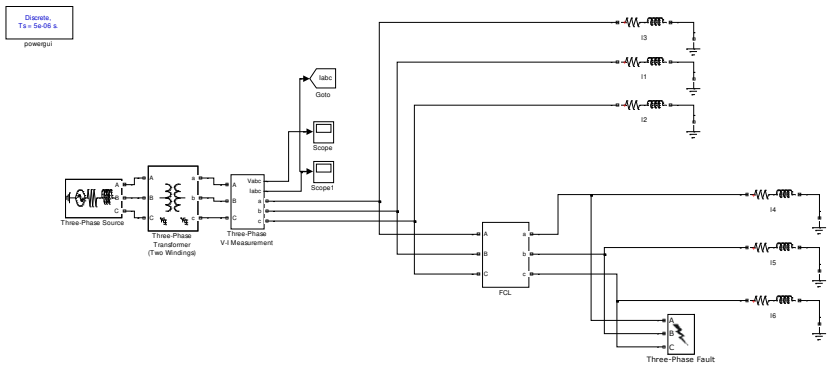


**Fig. 9 MATLAB/Simulink of the proposed circuit**

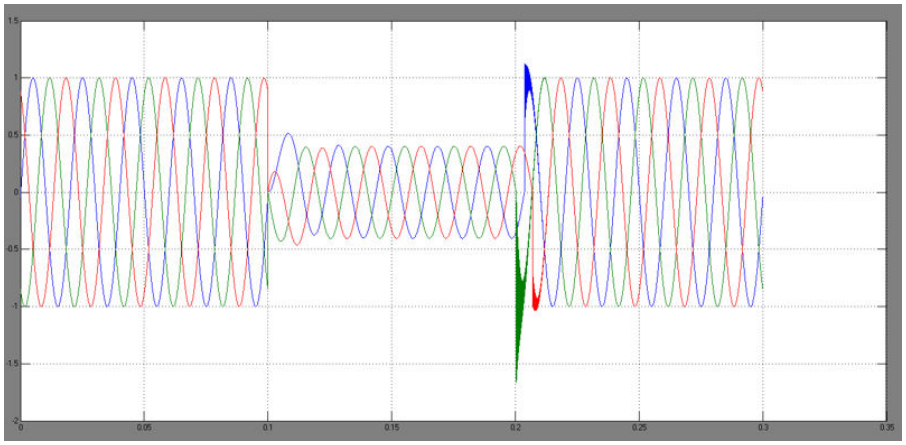

Fig. 10 PCC Voltage without FCL

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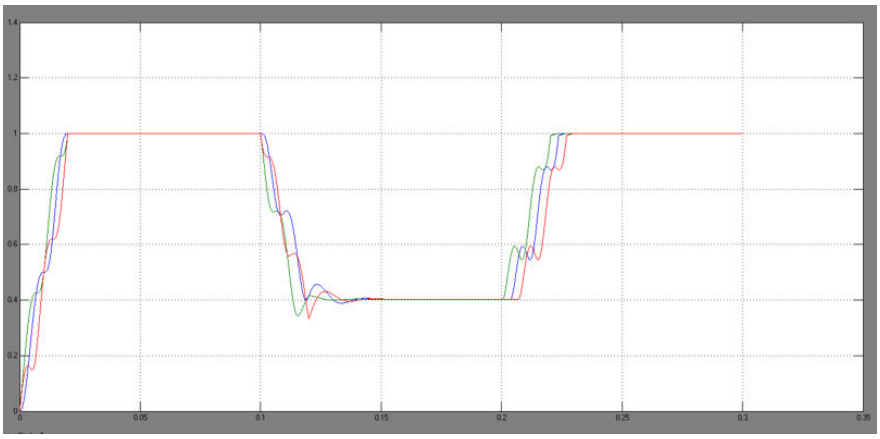

Fig. 11Three-phase instantaneous RMS voltage of the sensitive load without FCL

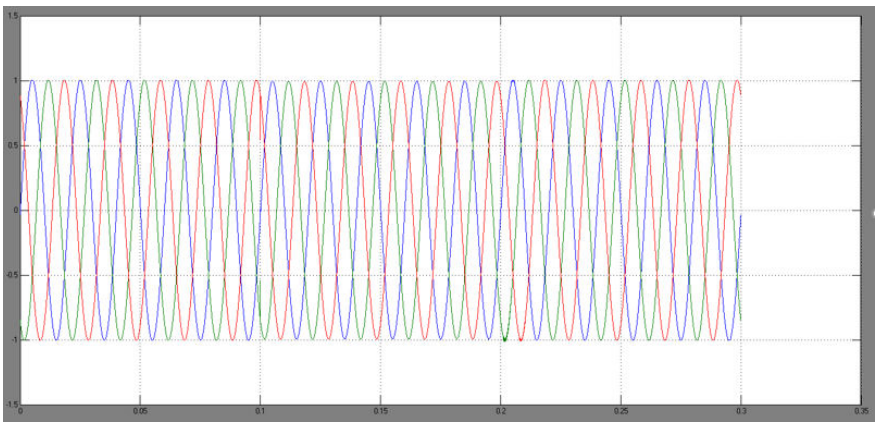

Fig. 12 Three phase PCC voltage with the proposed FCL.

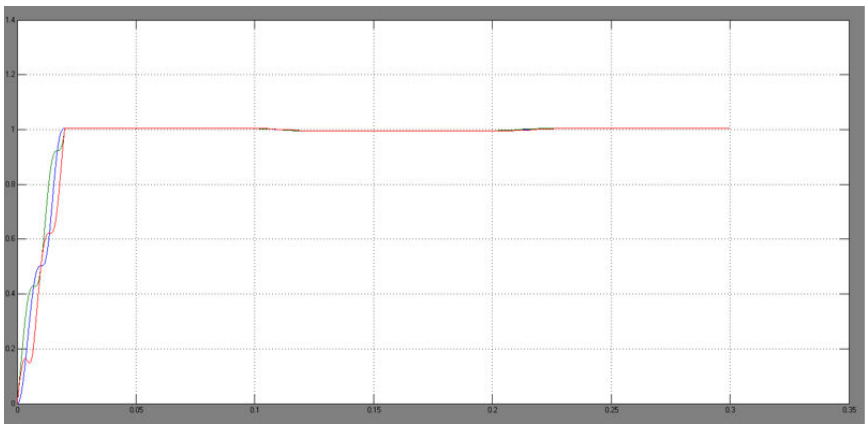

Fig. 13 Three-phase instantaneous RMS voltage of the sensitive load with the proposed FCL.

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## IV. CONCLUSION

In proposed system single phase and three phase fault will be create due which voltage deep accures in the system . this power quality problem will be mitigate using Fault cuurent limiter. In this paper, voltage sag compensation, phase-angle jump mitigation, and fault current limiting operation were analyzed. The designed FCL is capable of mitigating voltage sag and phase-angle jump to acceptable levels. By using the semiconductor switch in the dc current path instead of two numbers of Thyristors at the bridge branches, the FCL will have high speed and consequently, the dc reactor value is reduced to a lower value. In addition, the dc voltage source placed in the FCL structure reduces its THD and ac losses in normal operation. In general, this type of FCL, with the simple control circuit and low cost, is useful for the voltage-quality improvement because of voltage sag and phase-angle jump mitigating and low harmonic distortion in distribution systems. In addition to that three phase power systems are developed with and without the FCL as well as their behaviors are also observed

## REFERENCES

[1] Hye-Rim Kim, Seong-Eun Yang, Seung-Duck Yu, Heesun Kim, WooSeok Kim, Kijun Park, Ok-Bae Hyun,Byeong-Mo Yang, Jungwook Sim, and Young-Geun Kim, “Installation and Testing of SFCLs,” IEEE Trans. Appl. Supercond , vol. 22, no. 3, June 2012.

[2] M. Firouzi, G.B.Gharehpetian, and M. Pishvaie, “Proposed New Structure for Fault Current Limiting and Power Quality Improving Functions,” International Conference on Renewable Energies and Power Quality (ICREPQ’10) Granada(Spain), 23rd to 25th March, 2010.

[3] N. Ertugrul, A. M. Gargoom, and W. L. Soong, ‘‘Automatic classification and characterization of power quality events,’’ IEEE Trans. Power Del., vol. 23, no. 4, pp. 2417---2425, Oct. 2008.

[4] Steven M. Blair, Campbell D. Booth, Nand K. Singh, and Graeme M. Burt, “Analysis of Energy Dissipation in Resistive Superconducting Fault-Current Limiters for Optimal Power System Performance,” IEEE Trans. Appl. Supercond , vol. 21, no. 4, August 2011.

[5] M. Brenna, R. Faranda, and E. Tironi, ‘‘A new proposal for power quality and custom power improvement: Open UPQC,’’ IEEE Trans. Power Del., vol. 24, no. 4, pp. 2107---2116, Oct. 2009.

[6] W. M. Fei, Y. Zhang, and Z. Lü, ‘Novel bridge-type FCL based on self turnoff devices for three-phase power systems,’’ IEEE Trans. Power Del., vol. 23, no. 4, pp. 2068---2078, Oct. 2008

[7] E. Babaei, M. F. Kangarlu, and M. Sabahi, ‘‘Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters,’’IEEE Trans. Power Del., vol. 25, no. 4, pp. 2676---2683, Oct. 2010.

[8] M. Moradlou and H. R. Karshenas, ‘‘Design strategy for optimum ratingselection of interline DVR,’’ IEEE Trans. Power Del., vol. 26, no. 1, pp. 242---249, Jan. 2011.

[9] S. Quaia and F. Tosato, ‘‘Reducing voltage sags through fault current limitation,’’ IEEE Trans. Power Del., vol. 16, no. 1, pp. 12---17, Jan. 2001.

[10] L. Chen, Y. Tang, Z. Li, L. Ren, J. Shi, and S. Cheng, ‘‘Current limiting characteristics of a novel flux-coupling type superconducting fault current limiter,’’ IEEE Trans. Appl. Supercond., vol. 20, no. 3, pp. 1143---1146, Jun. 2010.

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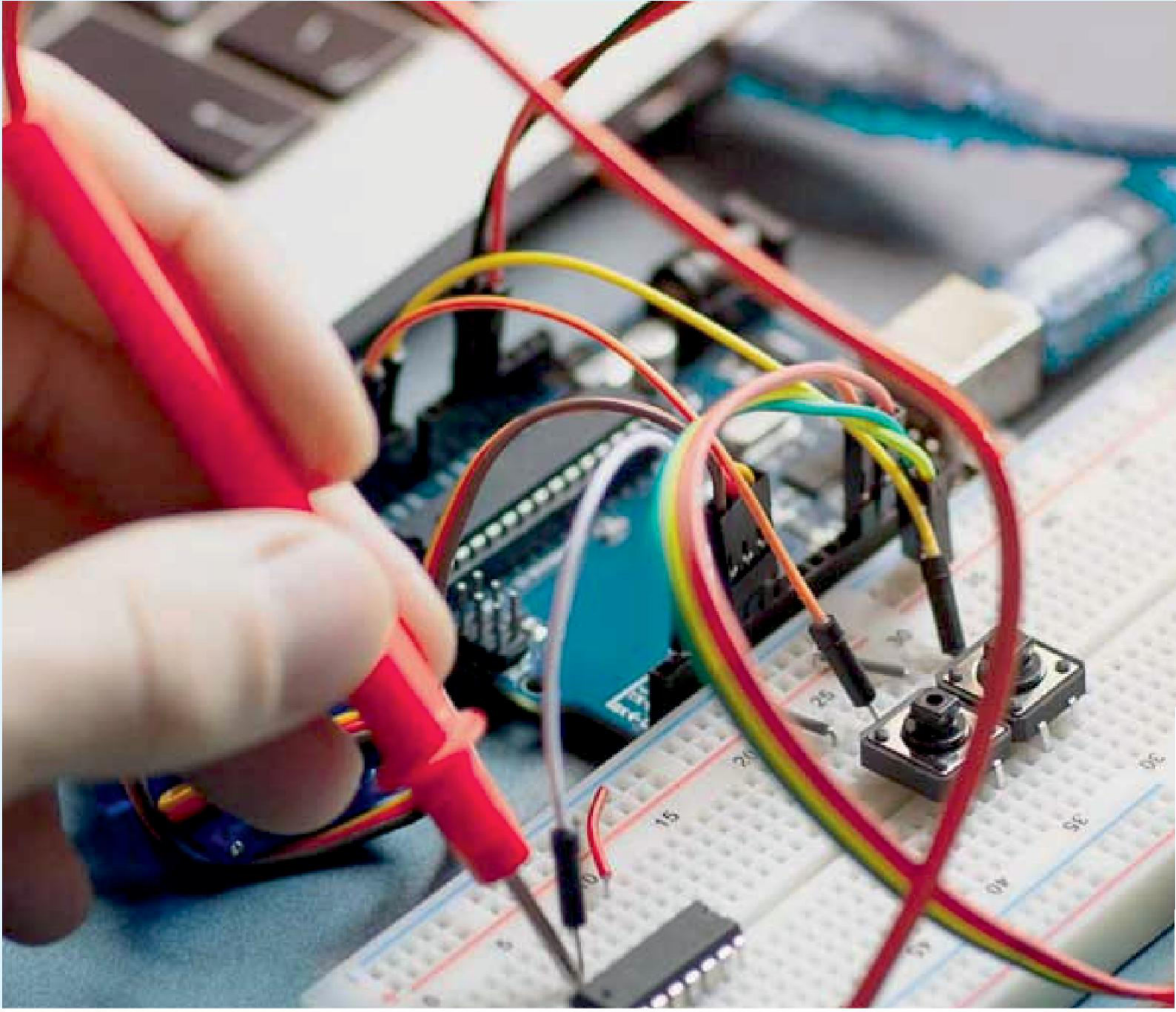

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