



e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 11, Issue 9, September 2022

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.18

☎ 9940 572 462

☑ 6381 907 438

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Pseudo Quadratic Dual Output Based Buck-Boost Converter

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ABSTRACT: The requirement of high frequency DC-DC converters is steadily increasing in many application areas such as portable electronic equipment, telecommunication systems, embedded systems, energy storage systems, and uninterruptable power supplies. A converter which follows pseudo quadratic voltage gain is designed. Compared with the quadratic buck boost topology, the pseudo quadratic topology can realize high voltage transformation ratio with lower peak voltage stress on switching devices. Additionally, the pseudo quadratic converter exhibits continuous input current and it results in lower peak to peak magnitude of ripple current in the source side. The voltage transformation ratio and the passive components design expression are formulated by using steady state time domain analysis. In order to increase the output voltage, the converter is employed with dual output concept. To illustrate the advantage of pseudo quadratic converter, a comparison with conventional and other buck boost converter is carried out. The performance study and analysis of pseudo quadratic dual output buck boost converter is carried out with MATLAB/SIMULINK 2017b. It is observed that the output of converter is 62V and 45V, 50Hz. Here the control circuit is realized using PIC16F877A.

KEYWORDS: DC-DC Converter, Buck-Boost Converter, Pseudo Quadratic, High Voltage Transformation Ratio.

I. INTRODUCTION

Nowadays, the requirement of high-frequency dc-dc converters is steadily increasing in many application areas such as portable electronic equipment, telecommunication systems, embedded systems, energy storage systems, and uninterruptable power supplies [1]-[2]. The traditional buck-boost converter (TBBC) is a well-known topology of realizing bucking/boosting the source voltage. However, achieving high voltage transformation ratio (VTR) at very high duty ratio is not a feasible solution due to the higher voltage stress on switching devices. Moreover, this topology has inverted load voltage polarity, and a higher magnitude of source current ripple is seen in the source side due to the power switch. To resolve these limitations, modified structures of buck-boost topologies have been reported in [3]-[5]. A non-inverted load voltage polarity based buck-boost converter with two power switches introduced in [3]. However, the nature of the input current is pulsating. Hence, this converter requires additional filtering circuit in the source terminal, leading to an increase in this topology order to six. Moreover, the maximum voltage stress associated with power switches and diodes is higher than the output voltage. Another buck-boost topology with four LC elements with a voltage transformation ratio square times than TBBC is presented in [4]. But this converter only operates in bucking mode due to the clamping action of intermediate diodes and its ripple contents in the source is more.

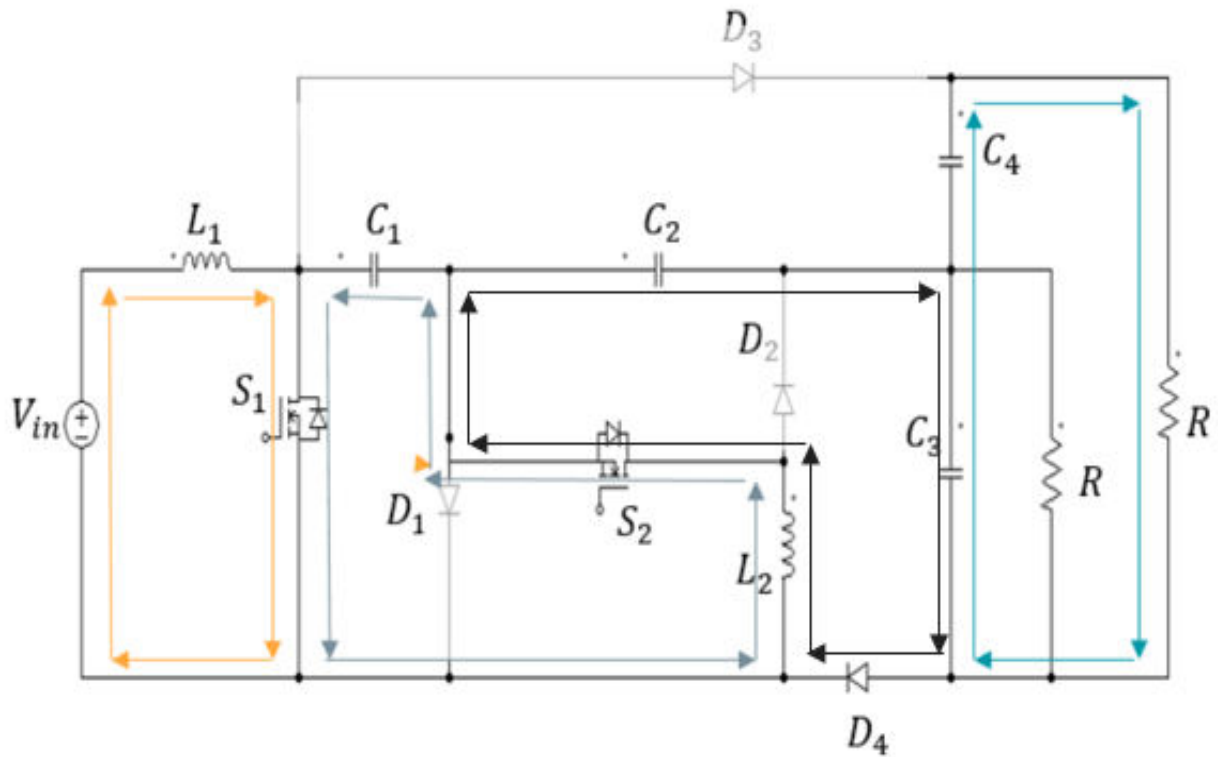
In [5], a quadratic buck-boost converter (QBBC) comprises six LC elements, five diodes, and one power switch with the advantage of lower magnitude of input current ripple is presented. But this converter has limitations, such as higher switching devices voltage stress, negative load voltage polarity and no common ground. All these topologies mentioned in [3]- [5], having quadratic voltage transformation ratio and these converters boosting the source voltage for duty ratio higher than 0.5 like TBBC. Therefore, the boosting region of these topologies is not very wide.

II. METHODOLOGY

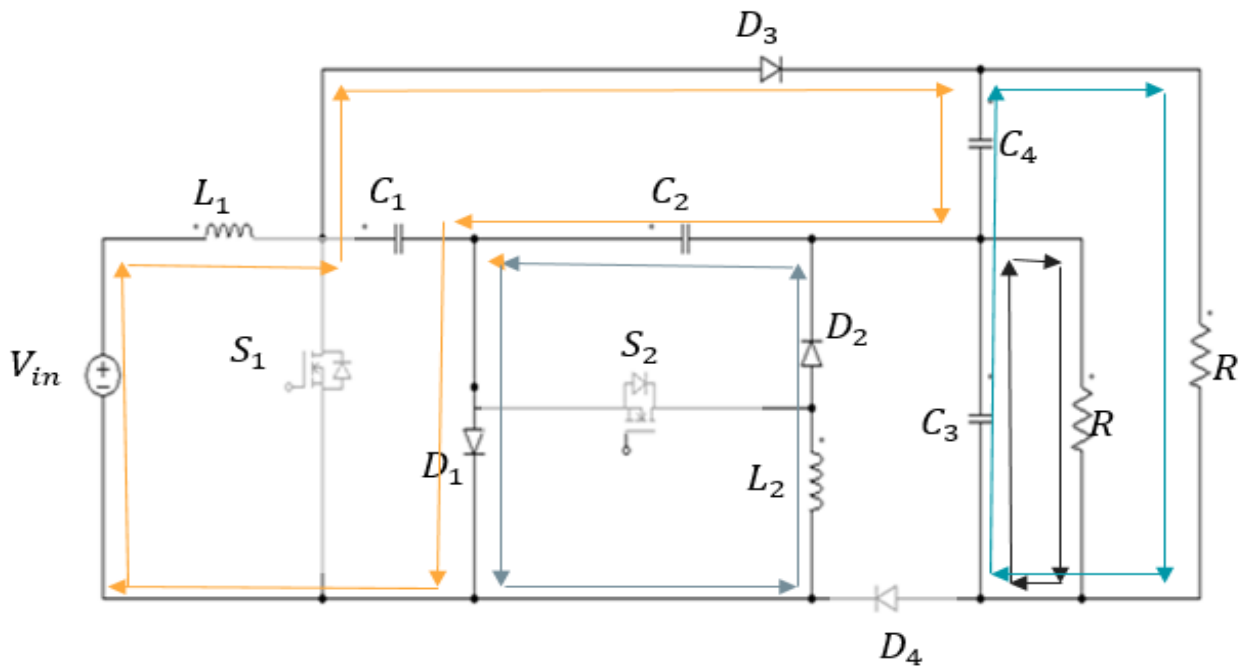
In Analysis and Control of Pseudo Quadratic Buck-Boost Converter, the capacitor C_3 is splitted into two for taking dual output, diode D_3 is rearranged to reduce distortions in output voltage, so it is tapped from the junction that meets L_1 , C_1 and S_1 . Diode D_4 is added in order to avoid reversel current flow in mode 2 operation. The modes of operation is similaras that of Pseudo quadratic buck-boost Converter.

There are two modes of operation.

State 1[t_0-t_1]: Switch S_1 and S_2 is turned on. All diodes except D_4 working off-state. The inductors L_1 and L_2 is charging through the input voltage and power switches. Capacitor C_1 , C_2 , and C_4 discharging and C_3 is charging.



State 2[t1–t2]: Switch S1 and S2 is turned off. The diodes D1, D2, D3 working conducting state. The diode D4 is reverse biased. The inductors L1 and L2 is discharging and capacitor C1, C2, and C4 charging and C3 is discharging.



III. DESIGN OF COMPONENTS

In order to operate converter, its components should be designed appropriately which consist of inductors and capacitors. The input voltage is taken as 50V with a switching frequency 50kHz. For designing pseudo quadratic buck



boost converter, For boost mode the input voltage is taken as 36V. The pulses are switched at the rate of 50kHz. The output voltage is taken as 48V. The rated power output of the converter is 42W.

Consider the input voltage is 36V and Gain is 1.247. Duty ratio can be calculated by,

$$\frac{V_{out}}{V_{in}} = G = \frac{48}{36} = 1.247$$

$$D = \frac{(2G+1) - \sqrt{(4G+1)}}{2G}$$

Assuming that the maximum allowed current ripple of the inductance is Δi_L , inductance L_1 and L_2 can be designed as

$$L_1 = \frac{DV_{in}}{F_s * \Delta i_1}$$

$$L_2 = \frac{DV_{in}}{F_s * \Delta i_2 * (1 - D)}$$

Taking the ΔV_c peak-to-peak capacitor voltage ripple into consideration, the capacitor value can be designed as,

$$C_1 = \frac{DI_o}{F_s * \Delta V_{c1} * (1 - D)}$$

$$C_2 = \frac{DI_o}{F_s * \Delta V_{c2} * (1 - D)}$$

$$C_3 = C_4 = \frac{DI_o}{F_s * 2 * \Delta V_{c3}}$$

IV. SIMULATION AND RESULT

Simulation parameters for the Pseudo quadratic dual output buck boost converter is given in Table, An input voltage V_{in} of 36V gives a output voltage V_o of 62V. The switch is MOSFET with constant switching frequency of 50 kHz. The duty cycle of switches is taken as $D= 0.43$.

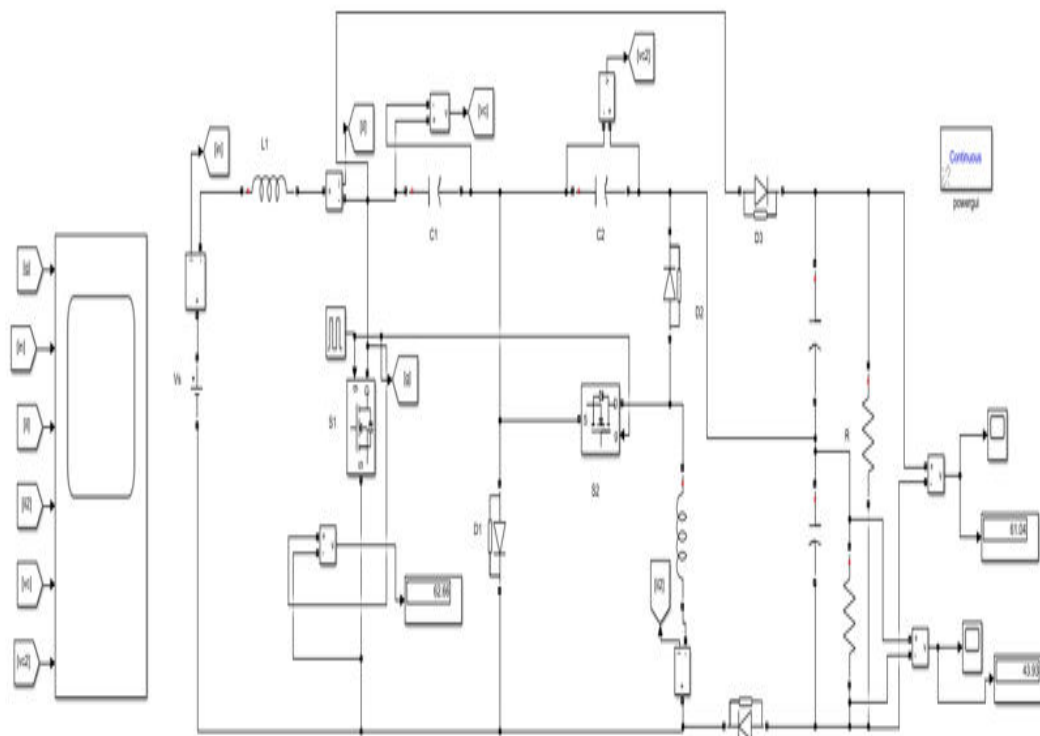
Table: 1

Parameters	Buck	Boost
Input Voltage(V_{in})	36V	36V
Duty ratio	0.31	0.43
Switching Frequency	50kHz	50kHz
Output Load resistance	24 Ω	48 Ω
Inductor L_1 Inductor L_2	1000 μ H 600 μ H	1000 μ H 600 μ H
Capacitor C_1 C_2 C_3 C_4	33 μ F, 33 μ f, 75 μ F, 75 μ F	33 μ F, 33 μ f, 75 μ F, 75 μ F

Pseudo quadratic dual output buck boost converter is simulated in MATLAB/SIMULINK by choosing the parameters listed in Table and the Simulink model is shown in figure.



Figure a: Simulink Model of Pseudo quadratic dual output buck boost converter



The simulation results of pseudo quadratic dual output buck boost converter are shown below. The switching frequency is chosen to be 50kHz.

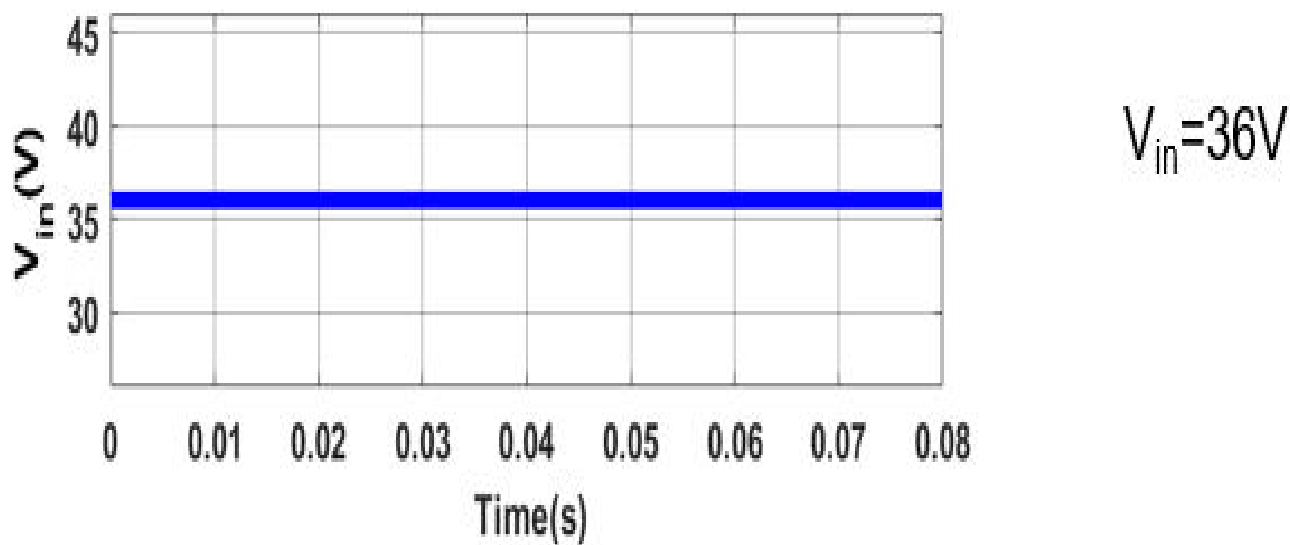


Figure b: Input voltage

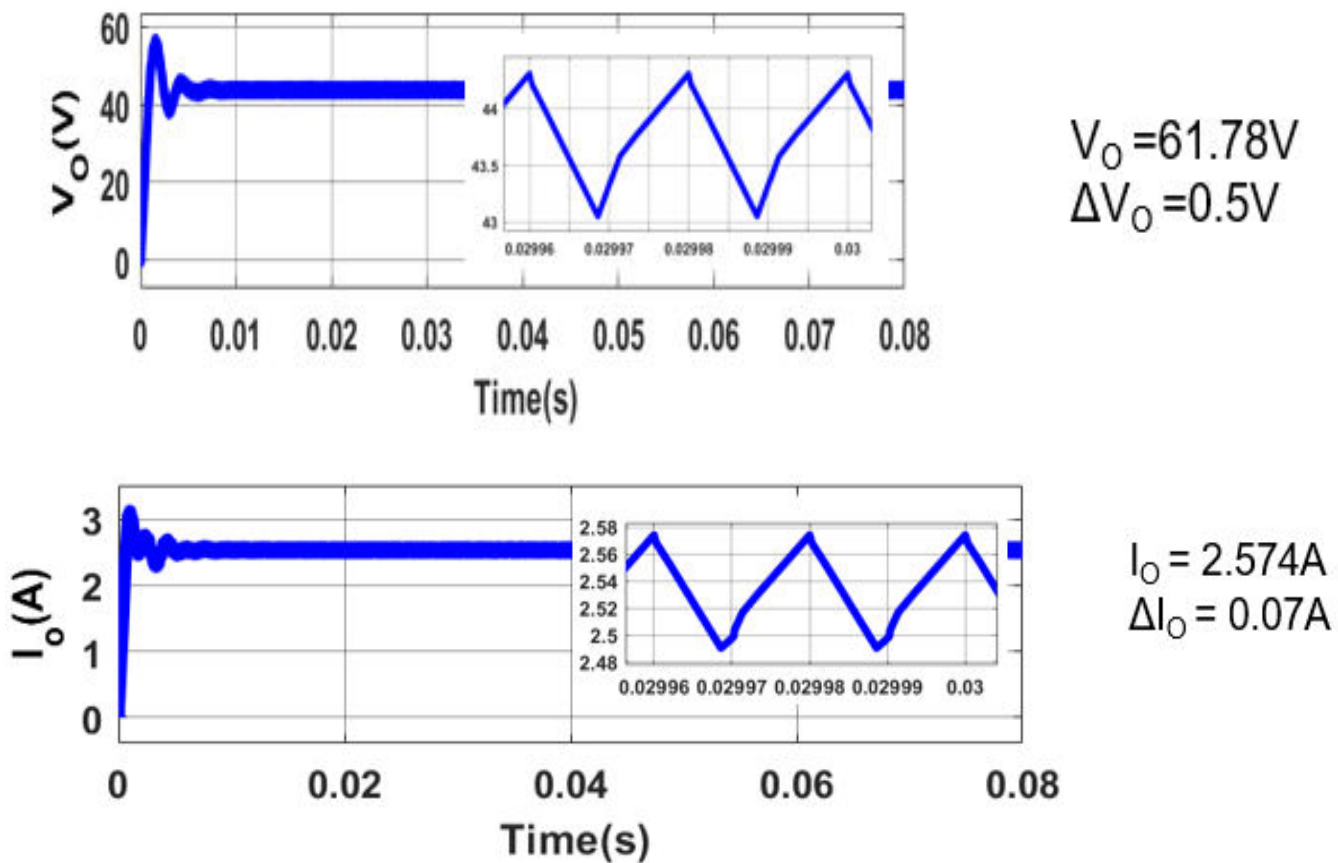


Figure c: (a) output voltage and (b) output current

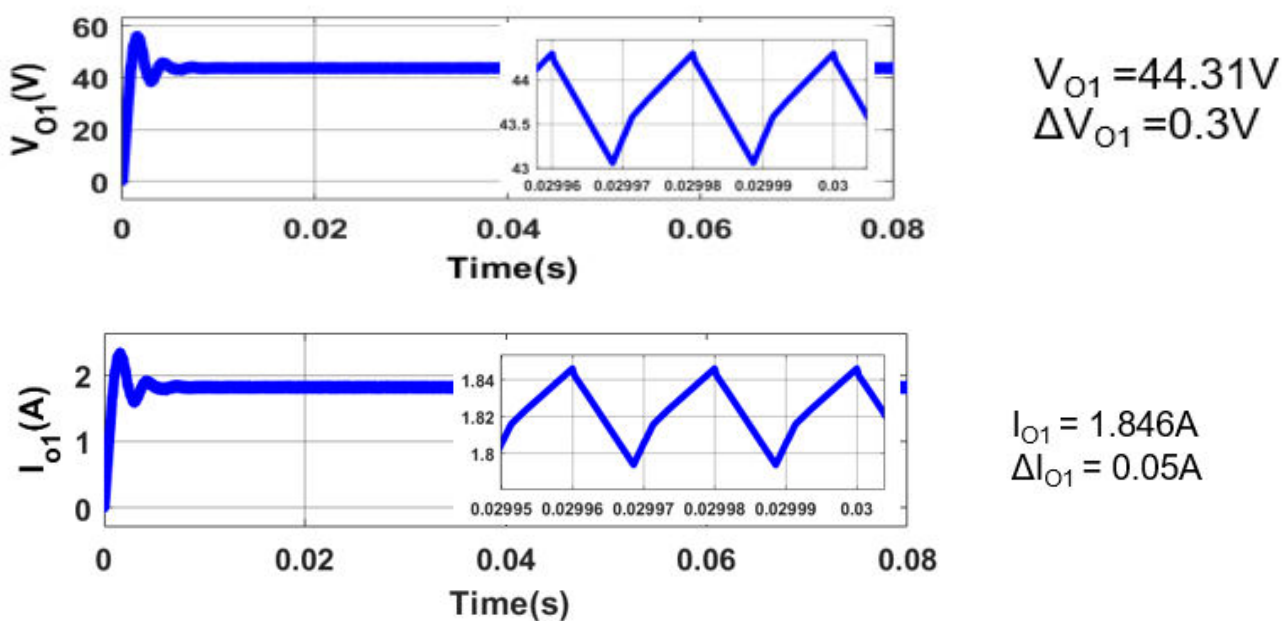
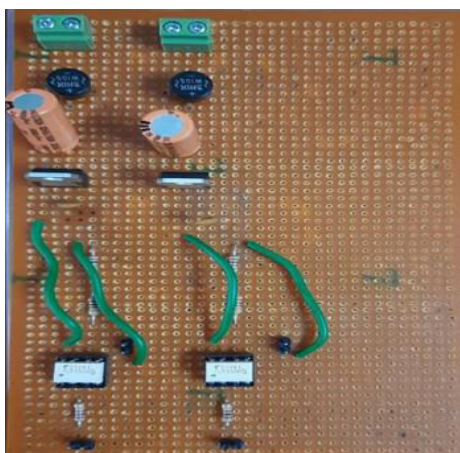
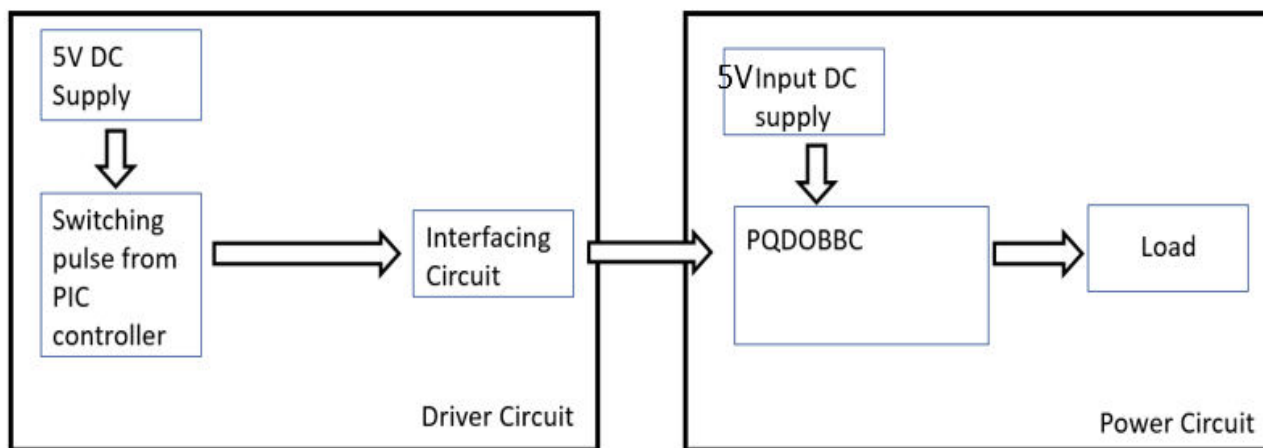


Figure d: (a) output voltage V_{O1} and (b) output current I_{O1}



V. HARDWARE IMPLEMENTATION

A prototype of Pseudo quadratic dual output buck boost converter with an input voltage of 5V is implemented. The experimental set up is shown in Figure. It consist of control circuit, driver circuit and power circuit. Control circuit is composed of PIC microcontroller and its power supply. The control pulses for MOSFET switches are generated using PIC microcontroller. The pulses from microcontroller is amplified by driver circuit which is composed of TLP250. It also provides isolation between control and power circuit. Figure 1 shows the schematic block diagram for hardware implementation. Figure 2 shows the interfacing circuit for converter. Figure 3 shows the experimental setup and output voltages.



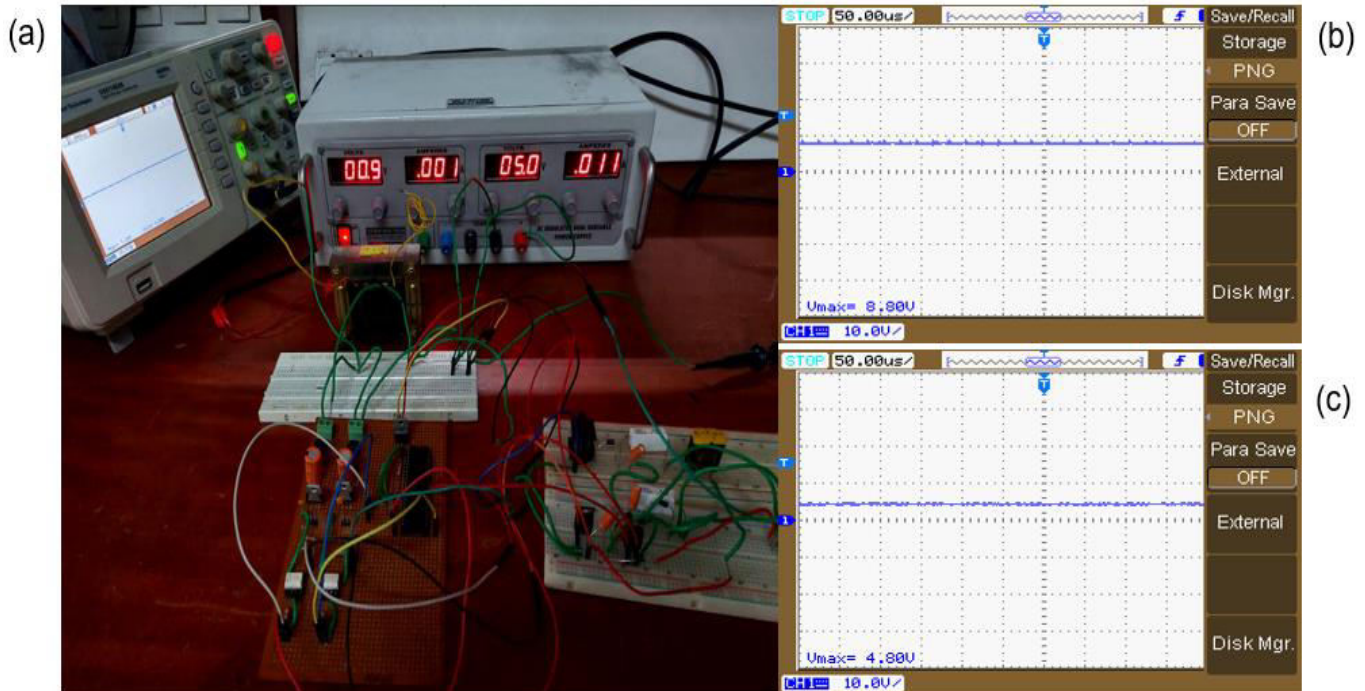


Fig. 1 Block Diagram Fig. 2 Interfacing Circuit

Fig .3 Experimental Setup and Output Voltages

VI.CONCLUSION

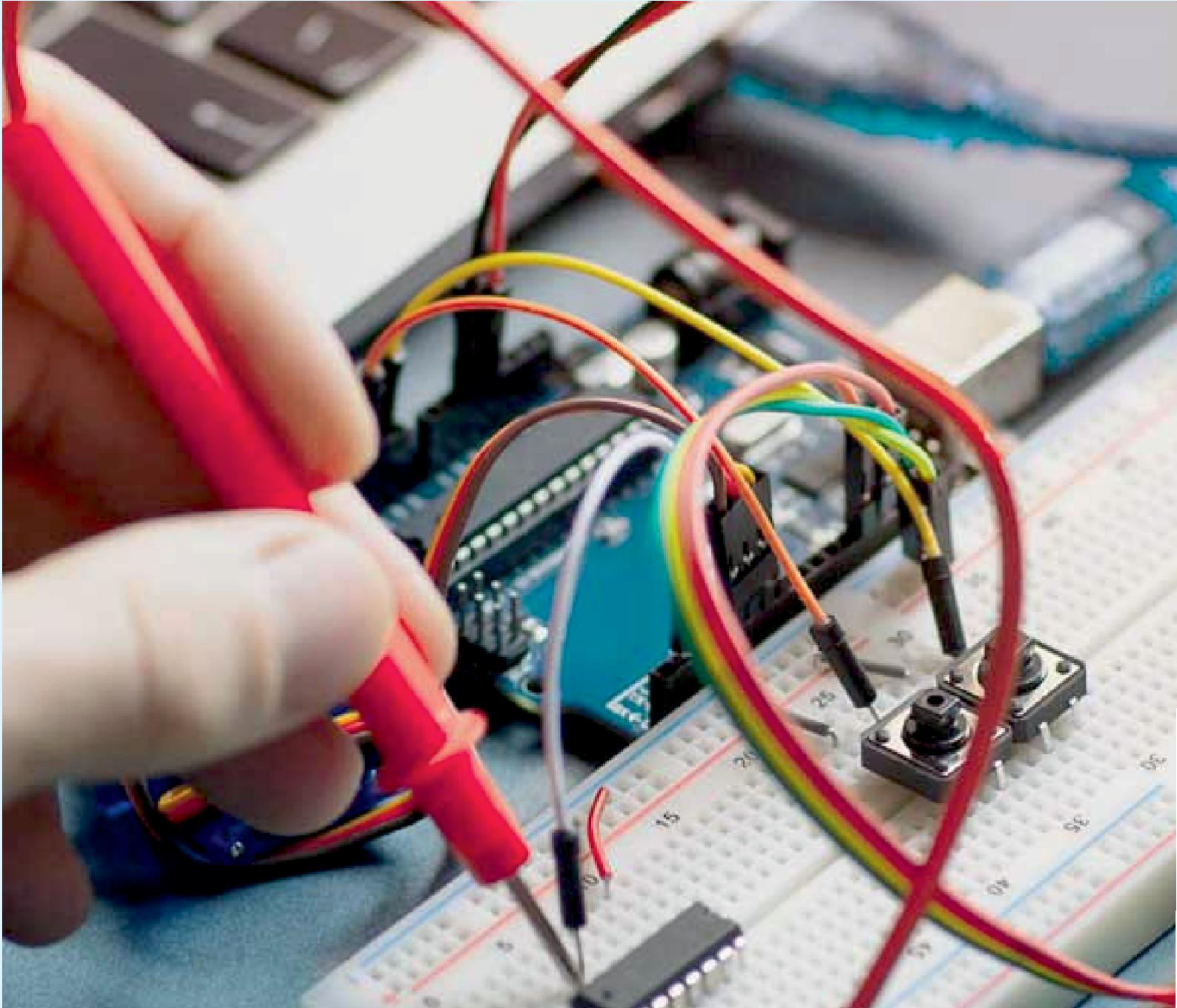
A pseudo quadratic dual output buck boost converter is explored for reducing voltage stress across switch and increasing output voltage. The advantage of the converter are high voltage gain, high output voltage and reduced voltage stress across the switch. A comparison considering the Pseudo quadratic converter and other converters was also carried out. Since this converter can achieve high voltage gain with reduced voltage stress and improved efficiency, it could be a promising choice for energy storage system, telecommunication system and portable electronic equipment. Converter performs both buck and boost operation with wide range of boosting operation.

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