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Universal Asynchronous Receiver and Transmitter (UART)

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ABSTRACT: All most every computer and microcontroller has several data ports with serial input/output devices like keyboards and serial printers which are used for communication. A modem connected to a serial port serial data can be transmitted and received from a remote location using a telephone line. The data communication protocol wherein a data communication interface which receives and transmits the serial data is known as a UART i.e. Universal Asynchronous Receiver Transmitter.RxD is the received signal and TxD is the transmited signal. The project (UART) has been implemented on Questa Sim due to its ASIC based functioning, high speed, accuracy, and user friendly interface.

KEYWORDS: UART; RxD; TxD; ASIC.

I.INTRODUCTION

UART isanintegratedcircuitwhichisprogrammedtocontrol a computer's interface to its attached serial devices, enabling it to talk to andexchange data with modems and some other serial devices.

- UART is a popular and most widely used device for data communication.
- Data is asynchronously transmitted and asynchronously received via the serial port on the computer.
- Contains parallel to serial converter for data transmission from the computer, and
- Serial to parallel converter is used for incoming data via the serial line.
- Two UARTs communicate with each other directly.

II. UART DESIGN

The UART design consists of three modules namely:-

1. UART Transmitter
2. UART Receiver
3. Baud Rate Generator

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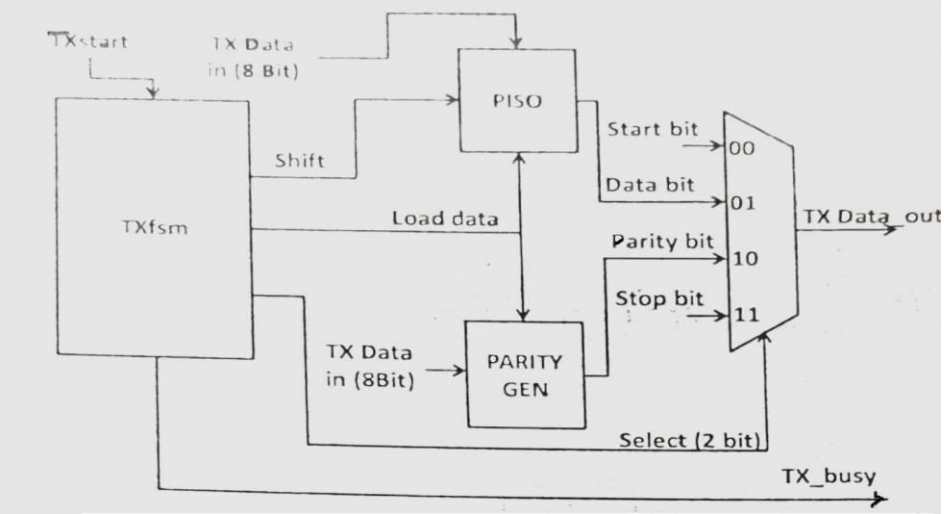
These modules further consist of several sub modules.

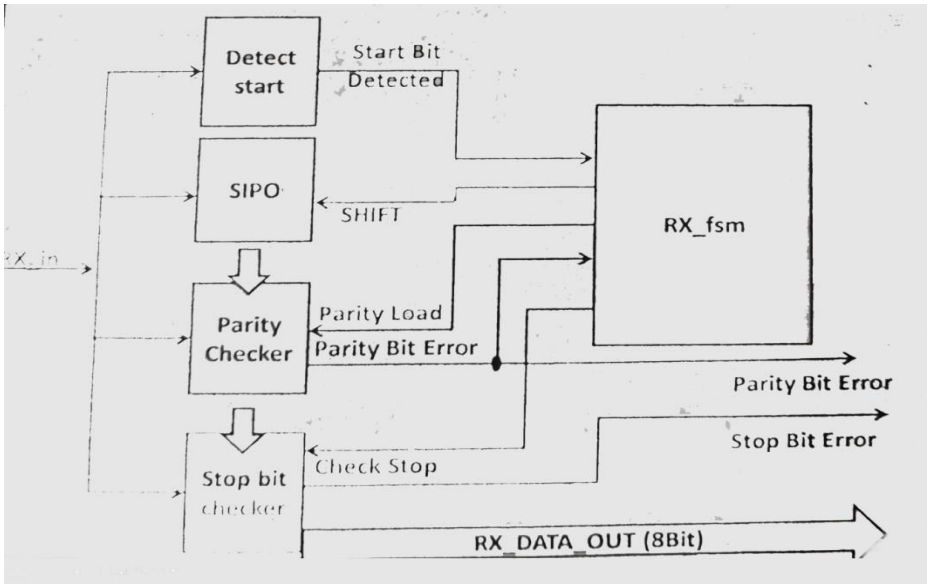
III.UART TRANSMITTER



This module comprises of four sub-modules:-
1.TX Controller fsm
Generates the necessary signals for data transmission at the correct time.
2.Parity Generator
For the 8-bit input data, generate parity.
3.PSIO (Parallel in Serial Out)
Takes the 8 bit input binary data and convert it into 1 bit serial data
4.Tx Mux
It is 4x1 Mux to transmit 4 different types of data viz. start-bit, data-bit, parity-bit and the stop-bit.

- The transmitter accepts the 8-bit data from the input and stores it in a register before adding additional special bits such as the start bit, stop bit, and parity bit (if enabled) to complete the data frame.
- The data frame then sent out serially by the transmitter at the predefined clock rate(baud rate).

IV.UART RECEIVER



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This module is divided further into five sub modules:-
1. Rx_fsm
Generates all the necessary signals required to receive data at right time for the UART Receiver.
2. Detect Start
The receiver ideally receives continuous 1 and as soon as the 0 is detected (which is done by this module), the reception of data starts.
3. SIPO (Serial to parallel out register)
Serial data is converted to 8-bit parallel data.
4.Parity checker
Check the correctness of data by Xoring the 10^{th} received bit with xor value of 8 bit received data.
5. Stop bit checker
After detecting of valid parity bit, the stop bit is detected and if the stop bit is not detected then reception of data is terminated/stopped by setting the stop bit error signal high.

- The receiver is by default at high logic state which indicates the idle state of receiver and keeps looking for the high to low transition i.e. start bit.
- When the start bit is detected, the receiver observes it for 50 percent of the receiving baud rate, then begins sampling other data bits in the middle of each bit if it is the receiver, otherwise the receiver sets the flag for framing.
- After detecting the 8 bit data, the receiver then looks for the parity bit which is generated by the transmitter for the single bit error detection.
- If the parity bit is detected properly, the receiver looks for the stop bit to stop the reception of data.
- After the successful detection of stop bit the receiver line goes from high logic state to indicate idle state and start looking for the next start bit.

V.BAUD RATE GENERATOR

- In asynchronous communication, the Baud Rate Generator determines the transmission pace.
- It is the number of symbols exchanged per second.
- Each bit is 1/(baud rate) wide.
- Baud rate =((clock freq. * 10^6)/(16*baud rate))/2.
- Some standard baud rates are:-

1. 2400
2. 9600
3. 19200
4. 384000
5. 115200

VI. RESULT AND DISCUSSION

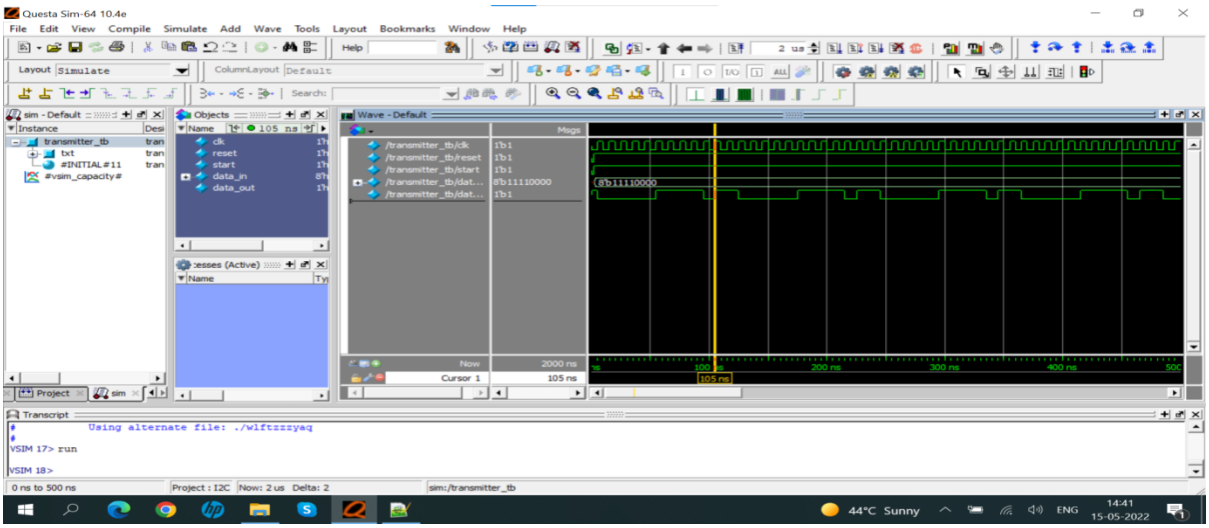

fig.1-TRANSMITTER

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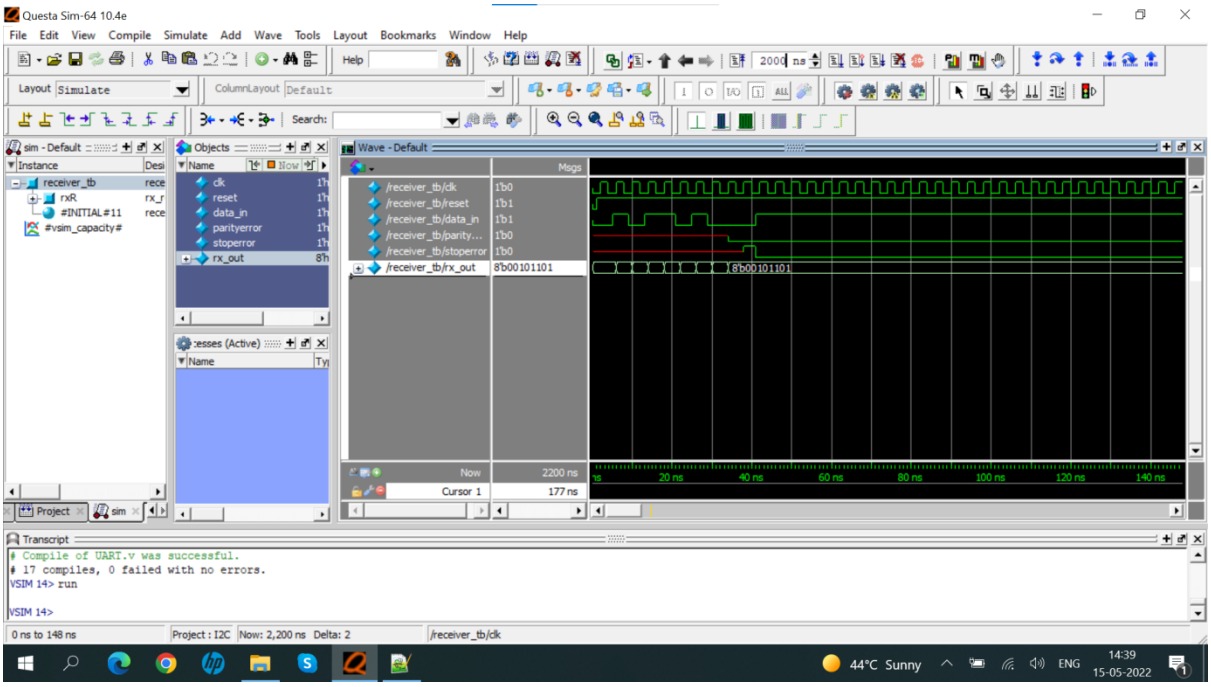

fig.2-RECEIVER

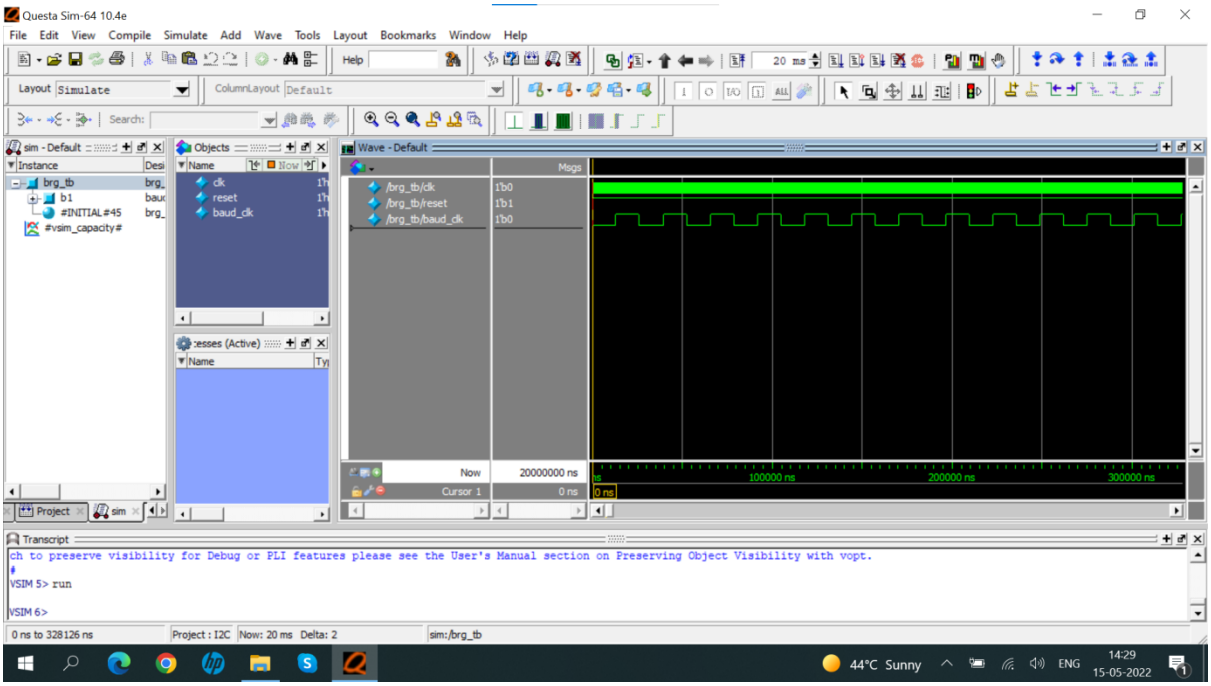

fig.3-BAUD RATE GENERATOR

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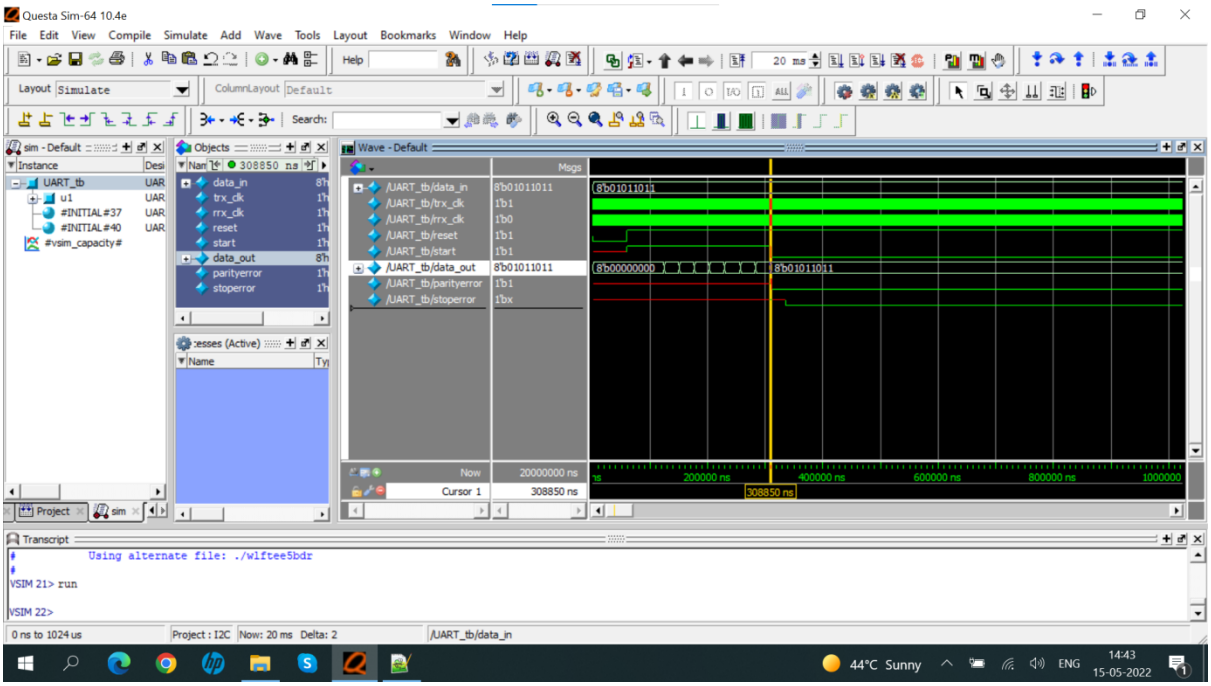


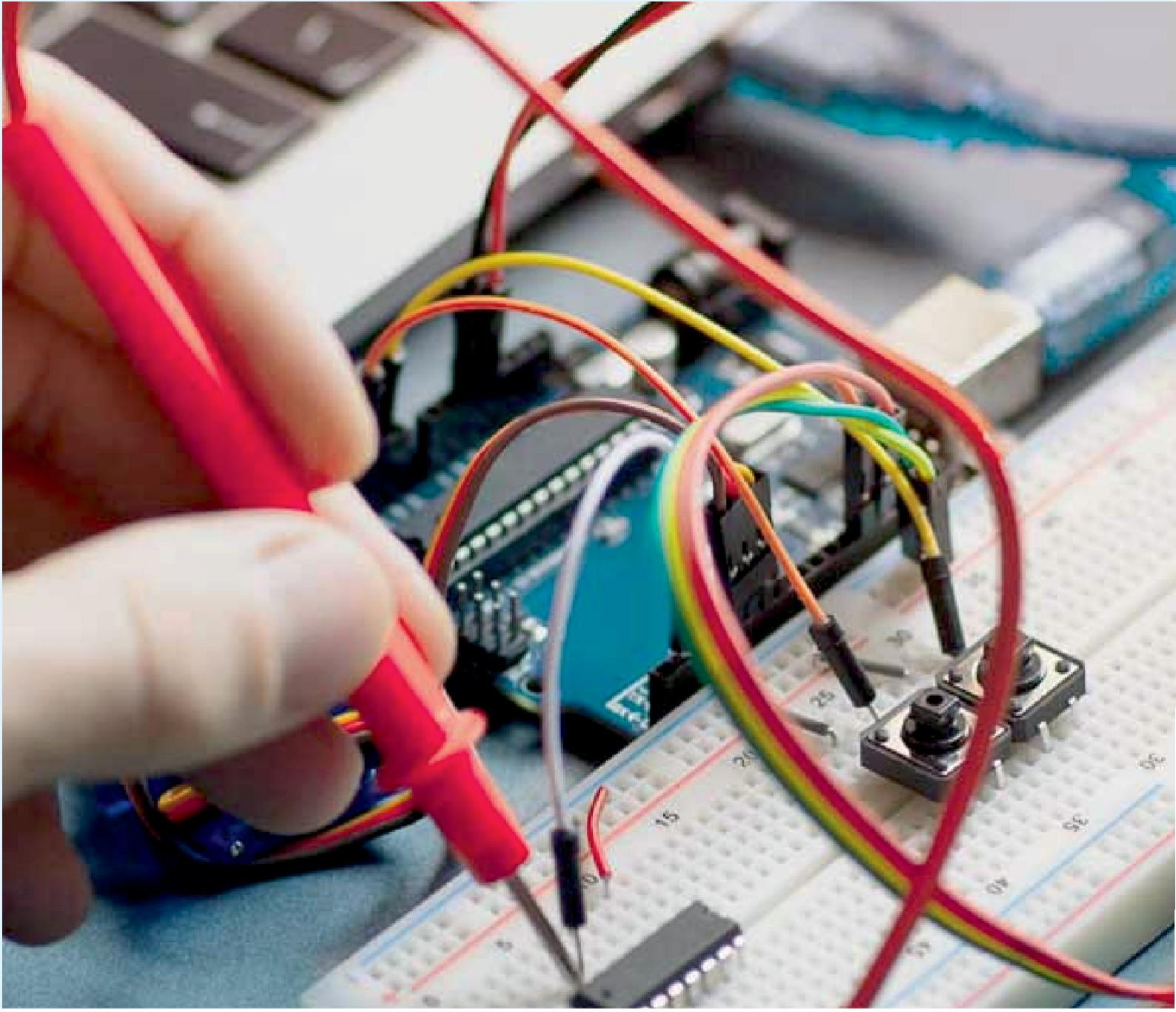
fig.4- Final output

VII.CONCLUSION

The UART architecture is successfully implemented.
Finally the simulation and synthesis of the UART design was obtained with the help of Questa Sim.

REFERENCES

[1] www.wikipedia.org
[2] IEEE Standard for Verilog Hardware Description Language (LRM)
[3] www.YouTube.com
[4] www.FPGA4.net



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