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An Evaluated Optimal Design of Full Adder and Full Subtractor in Quantum-Dot Cellular Automata

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ABSTRACT: Nowadays QCA technology seems to be very attractive for research purposes because of its various features like high speed, high packaging density, highly scalable, high switching frequency, and low power[2,3,7]. In this paper, we have design QCA circuits using majority voter gate .In this paper we have proposed design of a full subtractor and full adder which has least number of cell count. The output is shown with the QCA Designer tool and the result is obtained as full adder with 16 cell count and full subtractor with 17 cell count and both are having area as 0.012 μm^2.Bi-stable and coherence both simulation engines shows same output and this indicates the efficiency of our proposed design.

KEYWORDS: QCA, adder and subtractor, least cell design.

I.INTRODUCTION

These days CMOS technology lags, as it has faced various disadvantages like it absorbs high noise and consumes more power. So it is quite difficult to further create VLSI circuits with CMOS technology which will able to consumes less power and give high speed as well as density[2]. After CMOS, QCA is new upcoming technology. In QCA polarisation of electrons represents digital information. QCA allows very high operating frequencies that can be in tetra hertz range. Its integratable device density is also very high which is more than 900 times that of current CMOS scaling limits. It also have potential to reach upto very fast speed and ultra-low power consumption. The above mentioned characteristics develops research craze for it, in researchers mind. The heart of every processor's arithmetic unit is an adder. All other operations like subtraction, division, and multiplication can be implemented by using adders[11]. So for designing a good arithmetic circuit we have to put our focus on making an efficient adder circuit.

In this paper we tried to improvise the cell design of adder as well as subtractor that present in paper [28],by removing three cells in each design . This decreases cells count and area.

The structure of this paper is as follows: 2nd section present the detailed QCA technology background. In 3rd section the design is proposed with simulation result. The 4th section present the result. The discussion with limitations is given in section 5. Conclusion is presented in Section 6. Section 7 shows all helpful references.

II.BACKGROUND OF QCA TECHNOLOGY

In QCA the representation of digital information is in the form of electrons pair arrangement that forms quantum dot arrays. Every cell in QCA is generally made from four-electron sites that generally called quantum dots.There is a tunnel junction that couples these four electrons sites[3]. In the cell there exist two moving electrons[1]. By tunnelling, we mean that the moving electron can occupy freely any quantum sites inside cell. With coulomb interactions which are generally found between alternate cells, there information transfer is seen[22].

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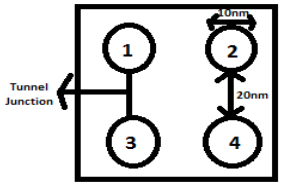

Fig 1:Basic QCA cell

Because of electrostatic or magnetic fields, there adjacent cells interacts with each other and then the state changes occurs. The below figure represents four quantum dots in QCA. The cell polarization are represent by two states of polarizations that is -1 for binary 0 and +1 for binary 1[1,2,3,4].

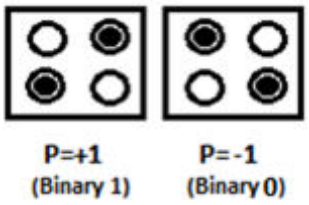

Fig 2: Four quantum dots in QCA with Polarization P as +1 and -1.

The above figure represents a square shaped space which contain two free electrons that form a quantum cell. In the square, there is quantum dots in all corner. Because of Coulomb interaction, electron pair move inside each cell and then the cell polarity can be determined by this position of electrons in the cell. As we know that the polarization has two values +1 and -1, that depends on the electron's position, which can also be termed as binary logic one and zero.

In QCA the application of wire is similar to that of the wire we used in the real world. Wire is nothing but a side by side connection of QCA cells that propagates a binary signal from one end of input to the other end that is till output[4]. Regular cells and rotated cells are two types of generally used cells from which wire is constructed. These two types of cells are shown in the figure below as follows[28].

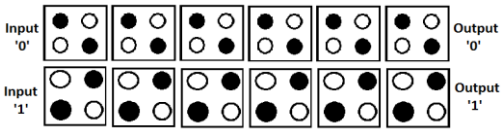

Fig 3: QCA wire(90 degrees)

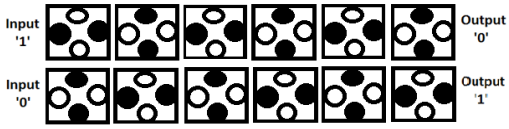

Fig 4: QCA wire (45 degrees)

Information that flows inside every circuit is generally controlled by the clock. This clock provides the power to run the circuit. It provides true power gain of the circuit. Cells are only powered by the clock and apart from it, there is not at all any other external source.

QCA inverter simply invert the given input signal and transfer it through output. The most widely used inverter is shown below as follow[2,21]:

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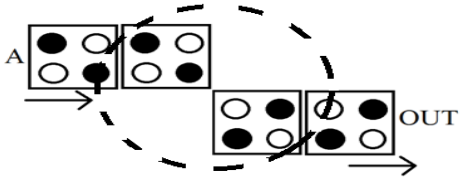

Fig 5: Inverter in QCA

The logical function representation of inverter gate is shown below:
F(A)=A'
Here we have A as input whereas F as output.
The truth table satisfying following logic function is shown below:

A	A'
1	0
0	1

Table 1:Truth table of inverter

In QCA, the majority voter gate plays a very important role in designing purpose. It has five cells in which three of them are input cells, the center cell makes decision and the fourth cell is used as an output cell [2,4].

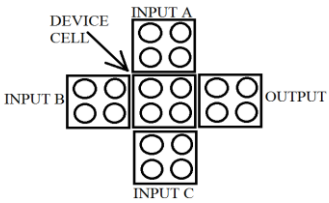

Fig 6:Majority vote gate in QCA

The logical function representation of majority voter gate is shown below as follows[14,18]:
F(A,B,C)= AB+AC+BC
Here we simply have three inputs as A,B and C and one output.

When we fix polarization of any one of the input of Majority gate to either "0" or "1", it can be used successively as AND or OR gate [9, 18].

Let us fix input C to 1 then we get output as A+B whereas fixing input C to 0 the output we get output as A.B. The logic function representation for majority voter gate as AND and OR gate is shown below as follows[19]:
M(A,B,1)=A+B
M(A,B,0)=A.B

A	B	C	OUT	
0	0	0	0	
0	0	1	0	
0	1	0	0	AND Logic When one input is set to "0"
0	1	1	1	
1	0	0	0	
1	0	1	1	
1	1	0	1	OR Logic When one input is set to "1"
1	1	1	1	

Table 2: Truth table of majority voter gate.

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The three input XOR gate is simply passes '1' if it get odd number of '1' at input side and because of this it is called as a odd detector.The present most efficient least cell QCA XOR gate design is made by adding three more cells in majority voter gate design and is presented in below as follows[28]:

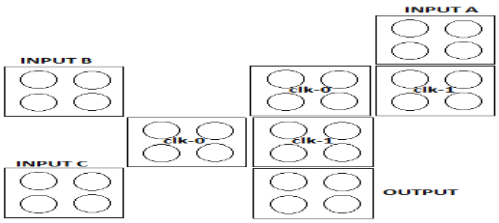

Fig 7:XOR gate in QCA

The logic function representation of XOR is shown below as follows[26]:
F(A,B,C)= A⊕B⊕C=ABC+A'B'C+AB'C'+A'BC'
Here we simply have three inputs as A,B and C and one output.

The truth table satisfying the above mentioned logical function of XOR gate is shown below:

Input			Output
A	B	C	F=A⊕B⊕C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 3: Truth table of XOR gate.

III.PROPOSED DESIGN WITH ITS SIMULATION RESULT

The QCA design of full adder as well as full subtractor are presented in the QCA Designer simulation tool.This tool is used to stimulate computational logic circuit constructed using QCA. It can be very simple to construct complex Quantum Dot cellular Circuits using this very simple tool. The engines are used in this tool for simulation are Bistable and Coherence Simulation Engine.

3.1 Full Adder

The 1-bit full-adder performs the addition of three inputs A,B,C which is one bit input each.We get two outputs at the end, one of the output termed as Sum and another one as Carry. The full adder block diagram with its truth table are shown below.

Fig 8:Block diagram of full adder.

The logical function for Sum and Carry is shown below[15]:
SUM=A⊕B⊕C
CARRY=AB+BC+AC

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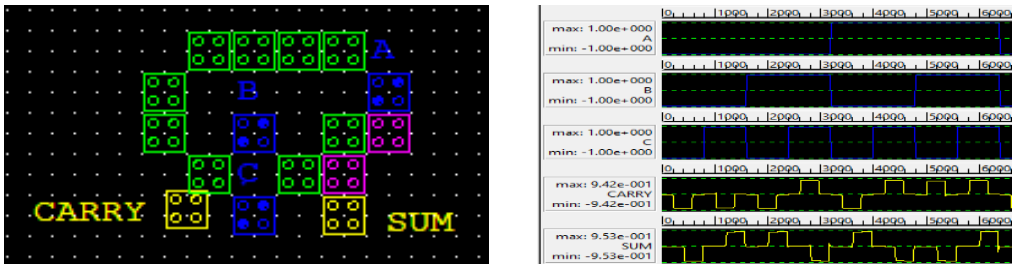
The truth table satisfying the above mentioned logical function of Sum and Carry is shown below:

Input			Output	
A	B	C	Sum = S	Carry = C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4: Truth table for full adder.

On analyzing the truth table of majority voter gate presented in table 2 we found that the output of majority voter gate is similar to the carry bit of full adder, so we can use QCA design of majority voter gate presented in figure 6 in designing carry bit of our full adder. And On analyzing the truth table of XOR gate presented in table 3 we found that the output of XOR gate is similar to the SUM bit of full adder, so we can use QCA design of XOR gate presented in figure 7 in designing SUM bit of our full adder. So by merging these two previously mentioned design the new proposed design of QCA Full-Adder circuit is shown below in figure 9(a) and the correctness of result this proposed design is successfully check using QCA Designer 2.0.3 tool and the output is shown in figure 9(b). Here the graph showing A,B and C as three input and the SUM output we get as (0,1,1,0,1,0,0,1)and CARRY output we get as (1,1,1,0,0,1,1,1) which are same as the desired output shown in truth table of full adder presented in table 4.



(a) (b)

Fig 9: (a) full adder circuit in QCA, (b) its simulation result

On counting the cells of full adder proposed here we can clearly see that our full adder design includes total 16 cells.
For calculating area we have to follow following steps which is shown below:
Step1: Here we can see total 6 cells are presented horizontally and each cell is having 18nm lenth and 18nm breadth so 18*18nm^2 area is being occupied by each cell. So for 6 cells with the particular gap between cells 2nm and the gap between one cell from its last boundary are 1nm.
So the entire horizontal area of 6 cells = (1+18+2+18+2+18+2+18+2+18+2+18+1) = 120nm
Step2: Next we have on total 5 cells are presented vertically so by following previous similar calculation we have.
the entire vertical area of 5 cells = (1+18+2+18+2+18+2+18+2+18+1) = 100nm
step 3: Total area occupied = 120nm * 100nm = 12000nm^2
So the area occupied by proposed design of full adder is about 0.012 μm^2.

3.2 Full subtractor
The one-bit full-subtractor performs the substraction of three inputs A,B,C which is one bit input each.We get two outputs at the end, one of the output termed as Difference and another one as Borrow. The full subtactor block diagram with its truth table are shown below.

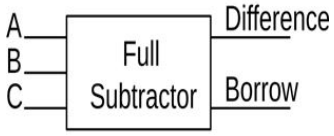


Fig 10:Block diagram of full subtractor

The logical equations for difference and borrow is shown below as follows[15]:

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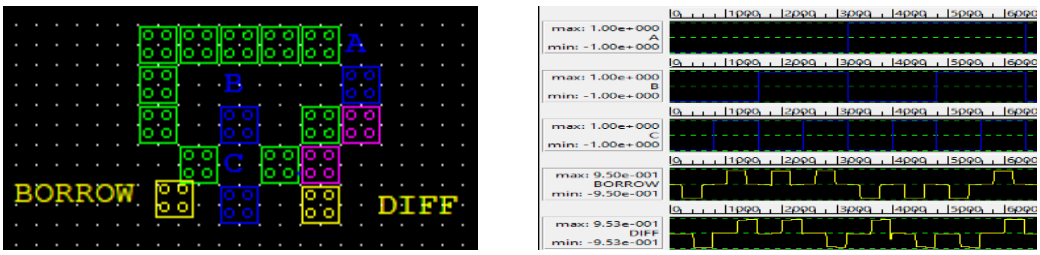
Difference=A⊕B⊕C
Borrow=A'B+A'C+BC

The truth table satisfying the above mentioned logical function of difference and borrow is shown below:

Input			Output	
A	B	C	Difference = D	Borrow = B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 5: Truth-table for full subtractor

On analyzing the truth table of majority gate voter presented in table 2 we found that the if we invert one of input of majority voter gate then we get the borrow bit of full subtractor, so we can use QCA design of inverter gate presented in figure 5 merging with design of majority voter gate presented in figure 6 to get borrow bit of our full subtrator. And On analyzing the truth table of XOR gate presented in table 3 we found that the output of XOR is similar to the difference bit of full subtractor, so we can use QCA design of XOR gate presented in figure 7 in designing difference bit of our subtractor. So by merging these previously mentioned designs the new proposed design of QCA Full-subtractor circuit is shown below in figure 11(a) and the correctness of result this proposed design is successfully check using the QCA designer tool and the output is shown in figure 11(b). Here the graph showing A,B and C as three input and the diff output we get as (0,1,1,0,1,0,0,1)and borrow output we get as (0,1,1,1,0,0,0,1) which are same as the desired output shown in truth table of full subtractor presented in table 5.



(a) (b)

Fig 11: (a)full subtractor QCA circuit,(b) its simulation result.

On counting the cells of full subtractor proposed here we can clearly see that our full subtractor design includes total 17 cells.
For calculating area we have to follow following steps which is shown below:
Step1: Here we can see total 6 cells are presented horizontally and each cell is having 18nm lenth and 18nm breadth so 18*18nm^2 area is being occupied by each cell. So for 6 cells with the particular gap between cells 2nm and the gap between one cell from its last boundary are 1nm.
So the entire horizontal area of 6 cells = (1+18+2+18+2+18+2+18+2+18+2+18+1) = 120nm
Step2: Next we have on total 5 cells are presented vertically so by following previous similar calculation we have.
the entire vertical area of 5 cells = (1+18+2+18+2+18+2+18+2+18+1) = 100nm
step 3: Total area occupied = 120nm * 100nm = 12000nm^2
So the area occupied by proposed design of full subtractor is about 0.012 μm^2.

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IV.RESULT ANALYSIS

Various papers are compared and the comparison table is shown below as follows.
Comparison table of QCA Full adder circuit

S.NO	REFERENCE	CELL COUNT	AREA
1	[1]	198	0.206
2	[2]	168	0.228
3	[3]	154	0.180
4	[4]	135	0.144
5	[5]	124	0.097
6	[6]	107	0.920
7	[7]	105	0.146
8	[8]	96	0.120
9	[9]	95	0.087
10	[10]	93	0.086
11	[11]	79	0.050
12	[12]	73	0.044
13	[13]	71	0.060
14	[14]	69	0.070
15	[15]	63	0.050
16	[16]	61	0.030
17	[17]	59	0.043
18	[18]	52	0.038
19	[19]	51	0.034
20	[20]	44	0.060
21	[21]	41	0.030
22	[22]	38	0.020
23	[23]	33	0.020
24	[24]	31	0.019
25	[25]	30	0.011
26	[26]	29	0.020
27	[27]	23	0.010
28	[28]	19	0.014
29	**PROPOSED DESIGN**	16	0.012

Table 6: Comparision table of QCA Full adder circuit

Comparison table of QCA Full Subtractor circuit

S.NO	REFERENCE	CELL COUNT	AREA
1	[29]	186	0.206
2	[3]	154	0.180
3	[30]	136	0.168
4	[31]	108	0.120
5	[32]	104	0.028
6	[33]	84	0.027
7	[34]	63	0.050
8	[35]	53	0.047
9	[36]	46	0.015
10	[37]	37	0.040

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11	[38]	32	0.028
12	[39]	27	0.030
13	[28]	20	0.014
14	**PROPOSED DESIGN**	17	0.012

Table 7: Comparision table of QCA Full subtractor circuit

From the above mentioned comparison tables we can see that our both proposed design of adder and subtractor have least cell count and area compared to all previously presented designs.

V.DISCUSSION AND LIMITATION

In this study, we apply the concepts and QCA designs of inverter, majority voter gate and XOR gate to design the QCA full subtractor and adder circuits.In future these designs will be very useful for designing large ALU. The simulation results is successfully demonstrated with comparision table between proposed design and all previous designs. But there can be one limitation in our designs,the proposed design of QCA full adder presented in this paper requires 16 cells and subtractor requires 17 cells. So in total if we want to make a circuit that can perform both adding and subtracting operations so from merging these separate designs, we required 16 cells summing with 17 cells so require 33 cells for it. But we see here that the sum bit in full adder and difference bit in full subtractor are same. So there is no need to make two different circuits for it. And on inverting one of the input in design giving output as carry bit we can easily get borrow bit output. So in future we will work in presenting an adder-subtractor circuit that can able to perform both adding as well as subtracting operations, design should possibly have the least no of cells that can decrease area.

VI.CONCLUSION

At the nanoscale circuit design level, QCA is the new emerging technology. QCA seems to be very realiable for the design of complex logic circuits and low-power-consuming logic circuits. The theoretical basis of Quantum Cellular Automata is discussed in this relevant QCA background for the research purpose. The basic elements of this technology like wire and clock are explained here. The above explained design shows adder and subtractor QCA circuits with least QCA cells that minimizes size. This paper presents improved design of adder and subtractor that shows expected result in least cell. The output is succsessfully shown using QCA designer 2.0.3 tool.

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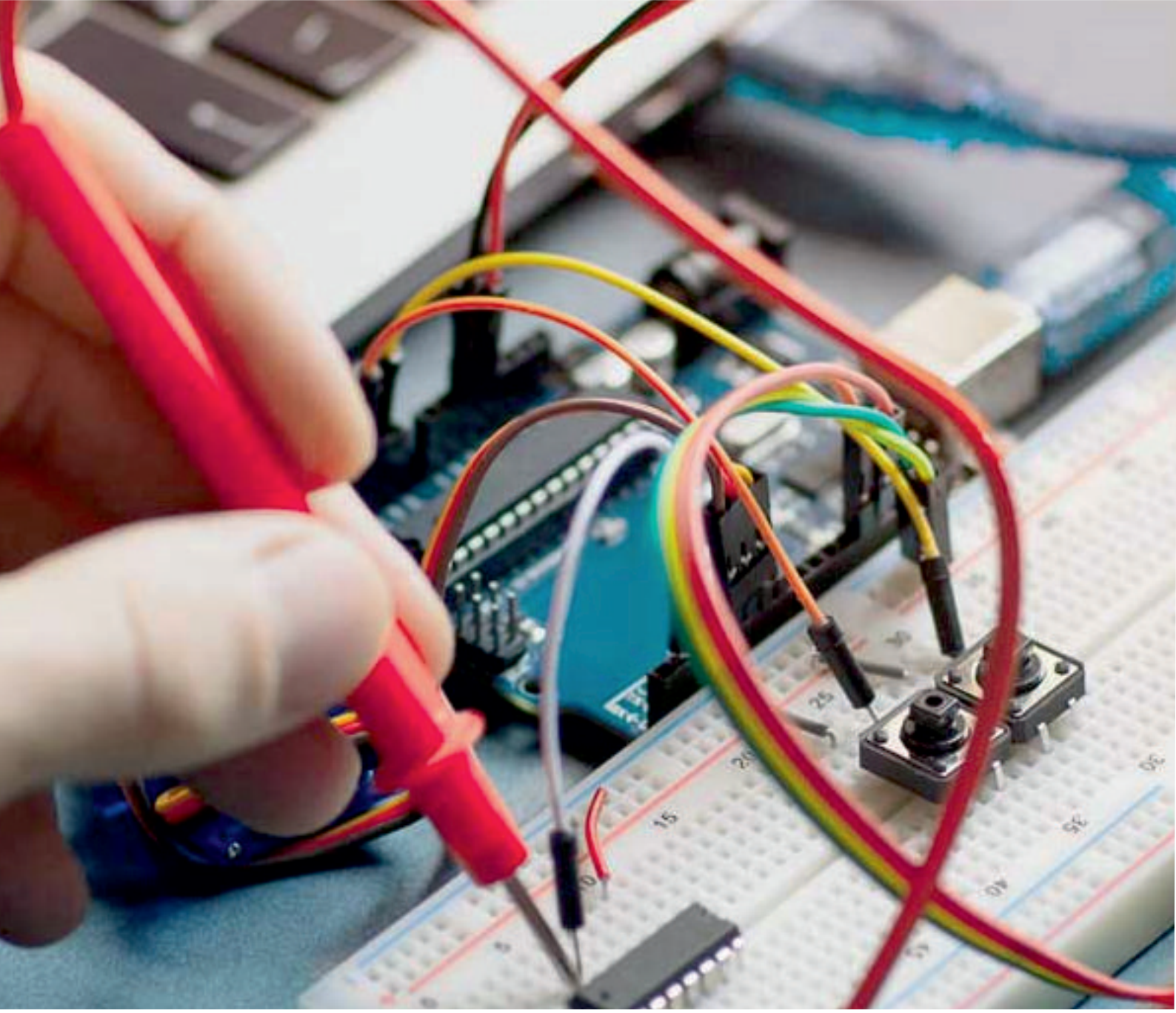

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