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Performance Analysis of T-Type Inverters Using SVPWM Control Technique

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ABSTRACT: A power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. Some advantages that multilevel inverters have compared to two level inverters are minimum harmonic distortion, reduced EMI/RFI generation, and operation on several voltage levels. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and a machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages and they are more expensive. The proposed paper focuses on reduction of conduction losses at the output of T-type multi-level inverter topology. The neutral point voltage balancing of the circuit is performed using redundant vectors of three level space vector diagram. Since the number of switches are reduced and single switching takes place per transition in SVPWM technique, the switching losses will get reduced to a considerable range. The above work is simulated using MATLAB / Simulink software. The experimental verification is carried out and the output waveforms are obtained.

KEYWORDS: SVPWM, Multilevel Inverters, T-Type Inverters, Conduction Losses, Reduced Device Count.

I.INTRODUCTION

The trend on providing electricity for cleaner environment has influenced the need for electric power in different forms. Power electronics in electrical engineering is a subject as a whole which has seen more technical enhancement and has impacted almost every sphere of human life. Power electronics has evolved as a key domain of electric power engineering and has got close bonding with different other disciplines like semiconductor engineering, network theory, analog electronics and digital electronics. Along with these, control systems, electrical machines, electrical power systems, electromagnetic theory etc are also connected with power electronics. The basic definition of power electronics is "control, regulation, conversion and conditioning of power". In recent times the most compelling advances in power electronics are **inverters**.

There are numerous applications where we will be having AC power load which needs to be powered from a DC power source. Generally renewable energy resource like solar PV cells are used to synthesis DC power where inverters are put in action to obtain AC power.

The paper proposed in [1] uses modified sinusoidal PWM technique to reduce the switching losses in T-type inverters, however neutral point balancing is difficult for the circuits like T-type inverters using this control technique. The paper proposed in [2] uses the concept of reduced device count for T-type inverters by modifying the switches placed between clamped neutral and load into a single switch, also reduced device count concept makes T-Type inverter more compatible with economical cost structure and there is no effect of reduced device count on output of T-Type converter. This paper focuses on reduction of overall conduction losses by reducing the number of switching devices used and by using modified SVPWM control technique.

II. COMPARISON OF CONVENTIONAL AND PROPOSED MODIFIED T-TYPE INVERTER

The T-Type inverters are originated by the modification of neutral point clamped (NPC) multilevel inverters. The working principle of T-type inverters remains same as NPC inverters. The conventional T-type inverter topology is as given in figure 1. Here 12 number of power devices are used, 12 number of diodes are used, 2 number of DC link capacitors are used and single DC supply is used. The switching table for this circuit is given in table 1. The possible three levels of outputs of this circuit are [$+V_{DC}/2$, 0, $-V_{DC}/2$]. Consider any one phase of the inverter. To obtain the positive state of output [$+V_{DC}/2$], the switch connected to the positive rail must be turned ON as given in figure 2a. Hence this switching state is called positive switching state and is represented as '**P**'. Likewise to obtain zero state of

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the output [0], the switches connected to the neutral point must be turned ON. Hence this switching state is called zero switching state and is represented as '**O**'. Similarly to obtain negative state of the output [-V_{DC}/2], the switch connected to the negative rail must be turned ON. Hence this switching state is called negative switching state and is represented as '**N**'. Working of the circuit considering the flow of the current in one of the three phases is explained in figure 2.

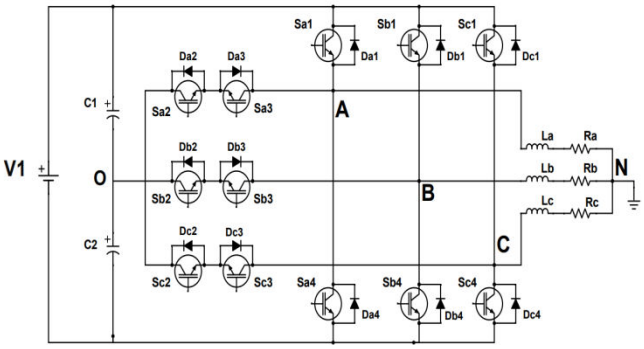

Figure. 1 : Conventional T-type inverter

Switching State	Device Switching Status (x=a,b,c)				Output Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P	ON	OFF	OFF	OFF	$V_{dc}/2$
O	OFF	ON	ON	OFF	0
N	OFF	OFF	OFF	ON	$-V_{dc}/2$

Table. 1: Switching table of conventional T-type inverter

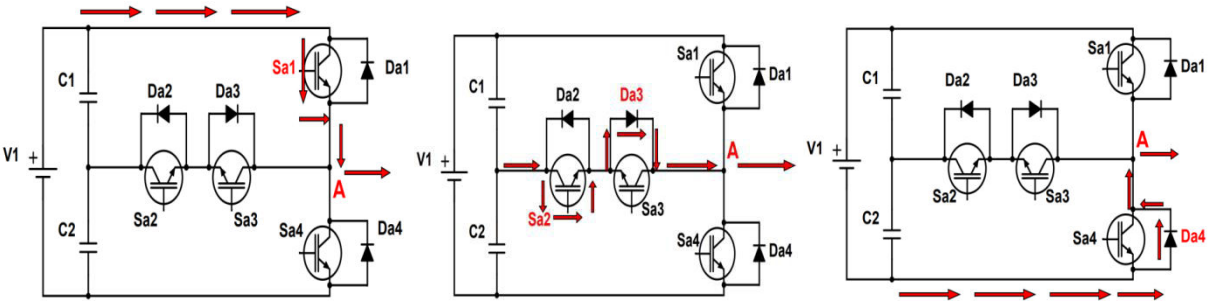

Figure. 2a,2b & 2c: Switching of conventional T-type inverter.

The modified T-type inverter topology is as given in figure 3. Here 9 number of power devices are used, 18 number of power diodes are used, 12 number of DC link capacitors are used and single DC supply is used. The switching table for this circuit is given in table 2. The possible three levels of outputs of this circuit are [+V_{DC}/2, 0, -V_{DC}/2]. Hence this switching state is called positive switching state and is represented as '**P**'. Likewise to obtain zero state of the output [0], the switches connected to the neutral point must be turned ON. Hence this switching state is called zero switching state and is represented as '**O**'. Similarly to obtain negative state of the output [-V_{DC}/2], the switch connected to the negative rail must be turned ON. Hence this switching state is called negative switching state and is represented as '**N**'. Working of the circuit considering the flow of the current in one of the three phases is explained in figure 4.

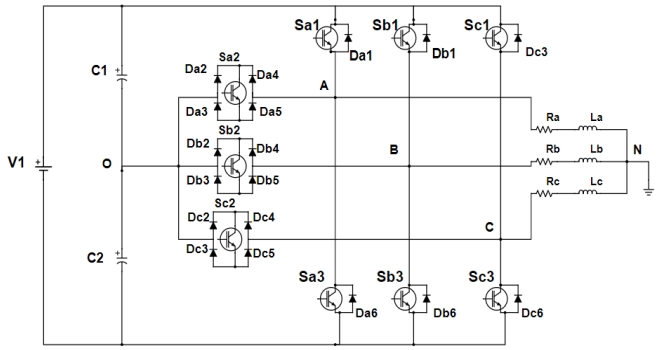

Figure. 3: Modified T-Type inverter circuit.

Switching State	Device Switching Status (x=a,b,c)			Output Voltage
	S_{x1}	S_{x2}	S_{x3}	
P	ON	OFF	OFF	$V_{dc}/2$
O	OFF	ON	OFF	0
N	OFF	OFF	ON	$-V_{dc}/2$

Table. 2: Switching table Modified T-type inverter

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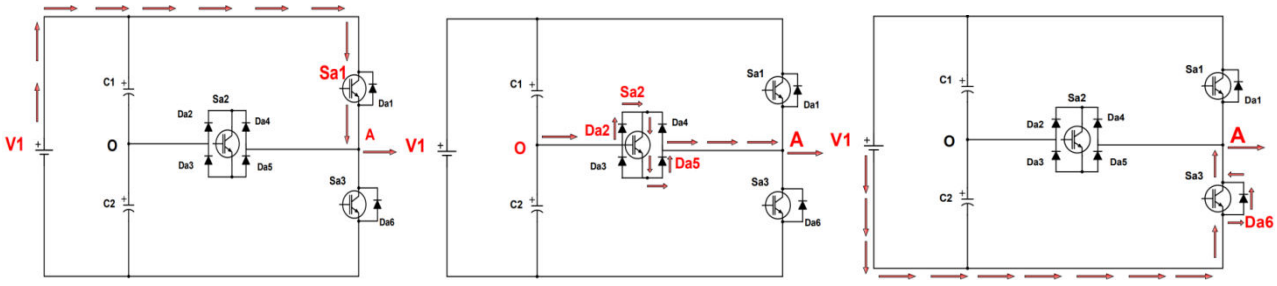

Figure. 4a, 4b & 4c : Switching of modified T-type inverter.

III.SVPWM CONTROL TECHNIQUE

The three level space vector diagram is as shown in figure 5(a). There are total 27 number of switching states in a three level space vector diagram which is explained with the help of table 3. Based on magnitude of space vectors, four categories of vectors are found in a three level space vector diagram. The four categories of Space Vectors are Zero vectors, Small vectors, Medium vectors and Large vectors.

The grand hexagon is divided into six small hexagons as shown in figure 5(b). These small hexagons are called **sub-hexagons.** In order to synthesize the resultant vector, each sub-hexagon can be split into 6 parts which are called **sub-sectors**. The resultant vector is synthesized by using these sub-hexagons and sub-sectors. To simplify into the space vector diagram of a two-level inverter, the following two steps have to be taken. First, from the location of a given reference voltage, one sub-hexagon has to be selected among the six sub-hexagons. Secondly the original reference voltage vector has to be subtracted by the amount of the centre voltage vector of the selected sub-hexagon. By these two steps, the three-level space vector plane is transformed into the two-level space vector plane.

Then the determination of switching sequence and the calculation of the voltage vector duration time are done as conventional two-level SVPWM method. As the proposed SVPWM method is same in principle as conventional two-level SVPWM, various techniques used in two-level SVPWM can be applied to this proposed method too.

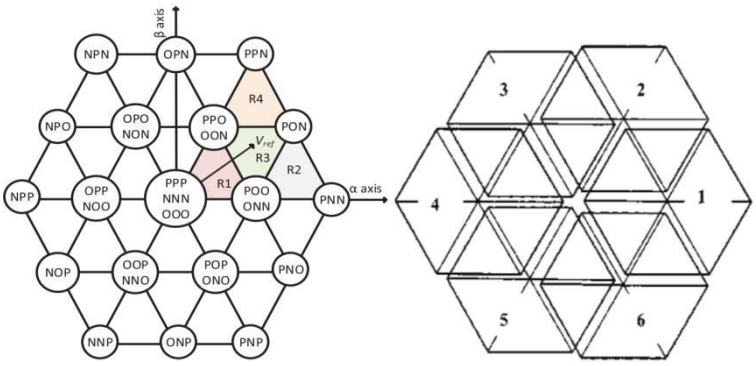

Figure 5a: Space vector diagram **Figure 5b: Six sub-hexagons**

Figure. 5: Representation of three level space vector diagram.

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VECTOR TYPE	MAGNITUDE	SWITCHING STATE		NEUTRAL POINT CURRENT	
ZERO VECTOR	0	[PPP]		----------	
		[OOO]			
		[NNN]			
SMALL VECTOR	$\frac{1}{3}V_D$	P-TYPE	N-TYPE	P-TYPE	N-TYPE
		[POO]	[ONN]	$I_b + I_c$	I_a
		[PPO]	[OON]	I_c	$I_a + I_b$
		[OPO]	[NON]	$I_a + I_c$	I_b
		[OPP]	[NOO]	I_a	$I_b + I_c$
		[POP]	[ONO]	I_b	$I_a + I_c$
		[OOP]	[NNO]	$I_a + I_b$	I_c
MEDIUM VECTOR	$\frac{\sqrt{3}}{3}V_D$	[PON]		I_b	
		[OPN]		I_a	
		[NPO]		I_c	
		[NOP]		I_b	
		[ONP]		I_a	
		[PNO]		I_c	
LARGE VECTOR	$\frac{2}{3}V_D$	[PNN]		----------	
		[PPN]			
		[NPN]			
		[NPP]			
		[NNP]			
		[PNP]			

Table. 3 : Different types of space vectors of three level space vector diagram.

IV.NEUTRAL POINT VOLTAGE BALANCING

The neutral point voltage balancing is mainly due to the uneven charging and discharging of DC link upper and lower capacitors. Firstly let us understand why does neutral point voltage fluctuates? The answer for this question is when we access the mid-point (neutral point) for our switching, the voltage at the midpoint fluctuates. This voltage fluctuation depends on the direction of current at the mid-point (which in turn depends on whether the capacitors are getting charged or discharged). The direction of current depends on the switching states we choose. This can be explained with the help of an example as given below.

Consider a switching state **[POO]** as shown in figure 6. When the current is flowing from source to load ($i_a > 0$)

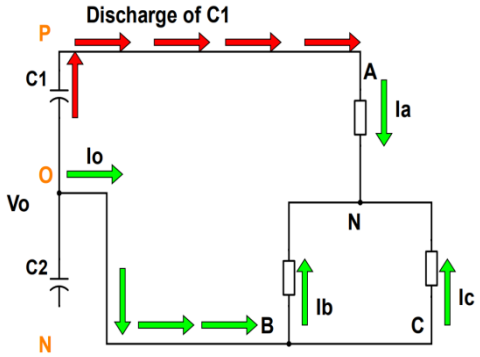

Figure. 6: Circuit of POO switching state.

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For a balanced load ($i_a + i_b + i_c = 0$) and ($i_b + i_c = - i_a$) from figure ($i_a = - i_0$). Hence the upper capacitor C_1 starts discharging and V_0 (mid-point voltage) goes up assuming total DC bus voltage is constant. More fluctuations leads to more harmonic distortion in the output and further uneven charging and discharging will put the capacitors and power switches at great risk and deteriorate the inverter performance. Possible solutions are additional balancing circuit which add cost and complicates therefore it is not widely used. The solution for this problem is by using the concept of multiplicity or degree of freedom since it is observed that these redundant switching states (alternative switching states) affect the mid-point voltage oppositely. For example consider a switching state **[ONN].** This is the redundant vector of **[POO]** which we had explained previously. Now let us see how oppositely does [ONN] affect the mid-point voltage. When the current is flowing from source to load ($i_a > 0$) as shown in figure 7.

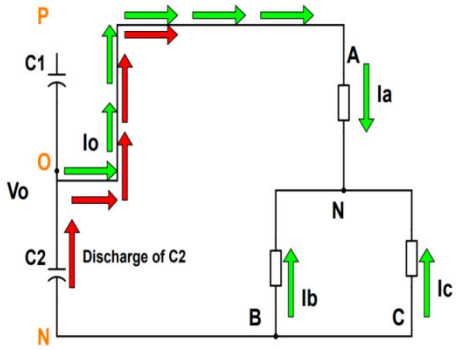

Figure. 7: Circuit of ONN switching state.

For a balanced load ($i_a + i_b + i_c = 0$) and $i_a = - (i_b + i_c)$ from figure ($i_0 = i_a$). Hence the lower capacitor C_2 starts discharging and V_0 (midpoint voltage) goes down assuming total DC bus voltage is constant. From these two examples we can say that the redundant vectors affect the neutral point voltage in opposite fashion. Therefore we can say that with redundant vectors we can balance the neutral point voltage that is by using one of the redundant vector for one switching time period TPWM and other redundant vector for the next switching time period so that the mid-point voltage remains constant.

V. RESULT AND DISCUSSION

The results of MATLAB simulation implementing space vector pulse width modulation to both conventional T-type inverter and modified T-type inverter (proposed circuit topology) are as given below.

Results for Modified T-Type Circuit Topology with RL load.

The results of simulations considering resistive inductive load with theoretically calculated values which is, output power of P_{out} = 30KW, output phase voltage of 240V, power factor of 0.9, resistance of R = 5.42 Ω and inductance value taken as L = 4.32 mH for a modified T-Type inverter is explained here. The conduction losses for the proposed circuit considering internal resistance of the switch to be R_{int} = 1mΩ is given in table 4. The waveforms of phase current, phase voltage, line voltage and neutral point voltage balancing are given in figure 8a, 8b, 8c & 8d.

PARAMETERS	S_{A1}	S_{A2}	S_{A3}	S_{B1}	S_{B2}	S_{B3}	S_{C1}	S_{C2}	S_{C3}
i_{rms}	29.38	19.28	29.5	29.47	19.17	29.58	29.54	18.84	29.68
$i^2_{rms}R_{int}$	0.863	0.372	0.87	0.868	0.367	0.875	0.873	0.355	0.88
OVERALL CONDUCTION LOSSES = 6.323 W									

Table. 4: Conduction losses calculated for modified T-type inverter with RL load.

The efficiency is calculated using the values of I_{in} = 53.64A, V_{in} = 700V, I_{out} = 45.74A, V_{out} = 467.6V and cos ϕ = 0.9.

Efficiency (η) % = $\frac{Pout}{Pin}$ x 100 = $\frac{35933.8}{37548}$ x 100 = **95.7%**.

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Total harmonic distortion THD obtained is as follows. For Line Currents = **6.28%**, Line Voltages = **35.81%** and Phase Voltages = **36.53%**.

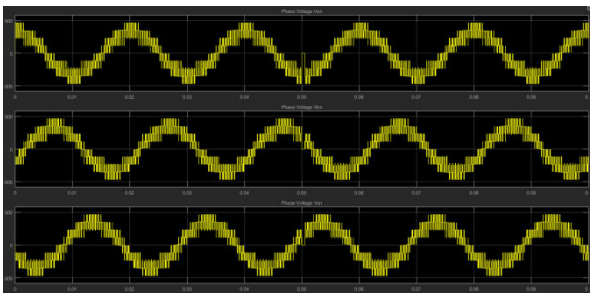

Figure. 8a: Obtained phase voltages of modified topology considering RL load.

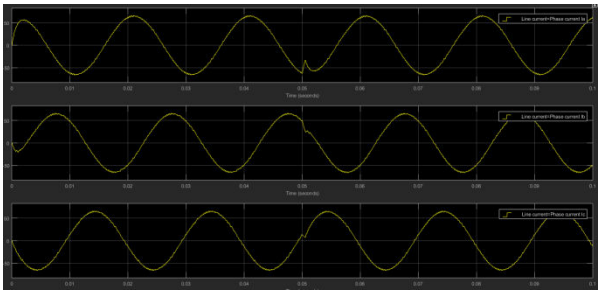

Figure. 8b: Obtained phase currents of modified topology considering RL load.

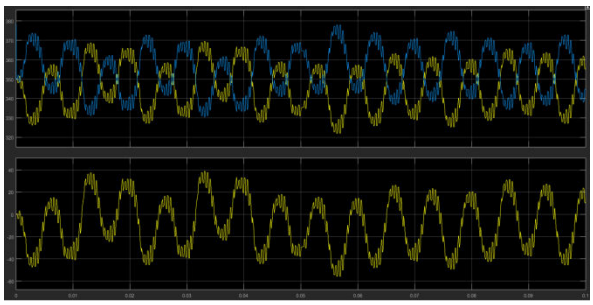

Figure. 8c: Obtained neutral point voltage balancing of modified topology considering RL load.

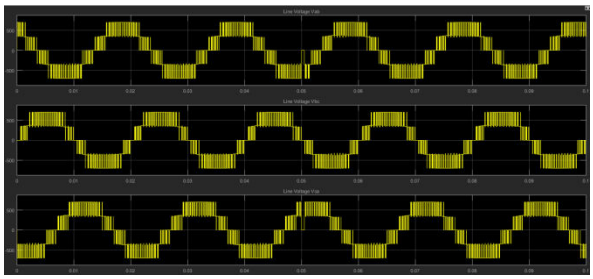

Figure. 8d: Obtained line voltages of modified topology RL load.

Results for Conventional T-Type Circuit Topology with RL load.

The results of simulations considering resistive inductive load with theoretically calculated values which is, output power of P_{out} = 30KW, output phase voltage of 240V, power factor of 0.97, resistance of R = 5.42 Ω and inductance value taken as L = 4.32 mH for a conventional T-Type inverter is explained here. The conduction losses for the proposed circuit considering internal resistance of the switch to be R_{int} = 1mΩ is given in table 5. The waveforms of phase current, phase voltage, line voltage and neutral point voltage balancing are given in figure10a, 10b, 10c & 10d.

PARAMETERS	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{B1}	S_{B2}	S_{B3}	S_{B4}	S_{C1}	S_{C2}	S_{C3}	S_{C4}
i_{rms}	29.12	19.13	19.13	29.55	29.2	19.03	19.03	29.62	29.27	18.7	18.7	29.73
$i^2_{rms}R_{int}$	0.848	0.366	0.366	0.873	0.853	0.362	0.362	0.877	0.857	0.35	0.35	0.884
OVERALL CONDUCTION LOSSES = 7.348 W												

Table 5: Conduction losses calculated for conventional T-type inverter with RL load.

The efficiency is calculated using the values of I_{in} = 53.17A, V_{in} = 700V, I_{out} = 45.68A, V_{out} = 467.7V and cos ϕ = 0.9.

Efficiency (η) % = $\frac{Pout}{Pin}$ x 100 = $\frac{35894.33}{37219}$ x 100 = **96.4%**.

Total harmonic distortion THD obtained is as follows. For Line Currents = **6.27%**, Line Voltages = **36.23%** and Phase Voltages = **37%**.

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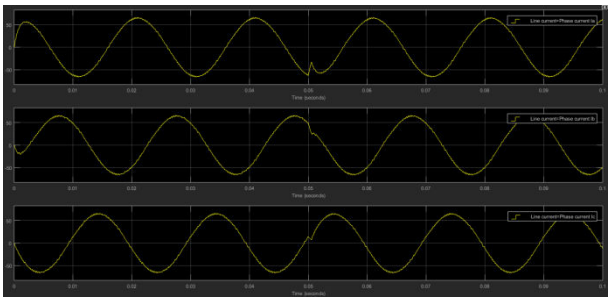

Figure 10a: Obtained phase currents of conventional topology considering RL load

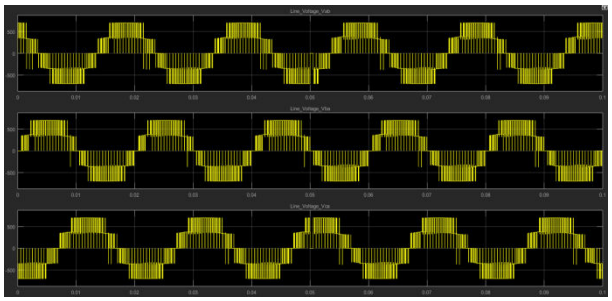

Figure 10c: Obtained line voltages of conventional topology considering RL load.

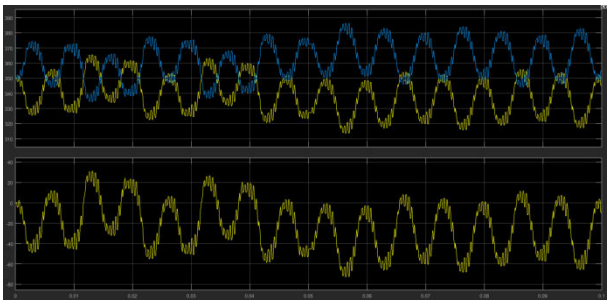

Figure10b : Obtained neutral point voltage balance of conventional topology considering RL load.

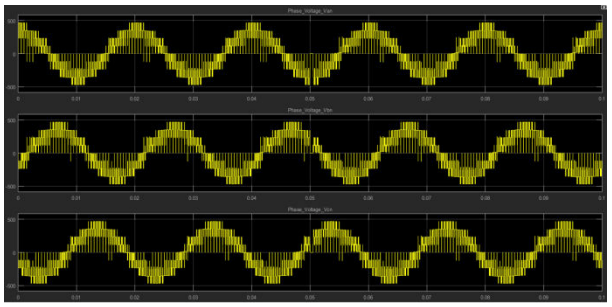

Figure10d: Obtained phase voltages of conventional topology considering RL load.

VI.CONCLUSION

From the comparison of conduction losses of conventional T-type inverter with modified T-type inverter (proposed) using space vector pulse width modulation, it is observed that we achieve lower conduction losses in modified T-type inverter, with the same ratings and same output parameters for medium switching frequencies.

The neutral point voltage balancing of the circuit is performed using redundant vectors of three level space vector diagram and the simulation results are attached to the report. Since the number of switches can be reduced and single switching takes place per transition in SVPWM technique, the switching losses will also get reduced to a considerable range.

Theoretical calculations of efficiency, THD and conduction losses were compared with simulation results. The simulated waveforms of phase currents, line voltages, phase voltages and neutral point voltage balancing for RL load for each of the topology (conventional T-Type and modified T-Type topology) are verified.

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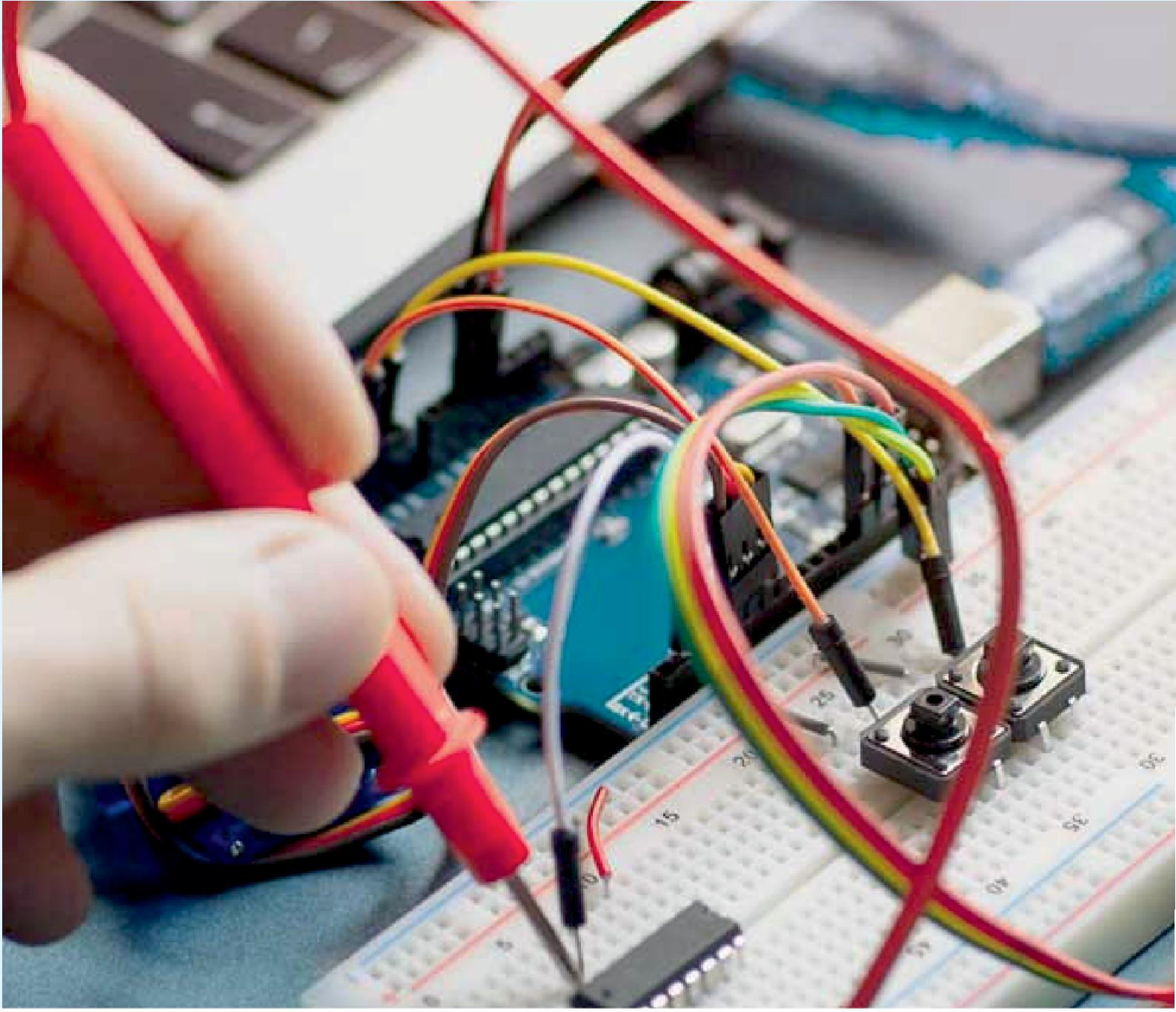

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