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The Four Newly Proposed Reflexive Definitive Flip Flops based upon Deterministic Restoration Behaviour for Digital Systems and it's Applications in Digital Circuit Designing.

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ABSTRACT: Computing Hardware plays an Evolutionary role in the near futuristic age of computing-informatics trends for accomplish any multiplex and rational computational tasks. For any Computing Hardware taxonomy the fabrication of superior and reliable digital circuits on any system board play's a significant role to perform any composite computational mechanisms or methodology. Because all fundamentals and Intermediate computational tasks are fully depend on the working patterns and computational behaviour mechanisms of these elementary digital circuits. The main and a composite part of the microprocessor name says ALU (Arithmetic Logic Unit) working mechanisms are fully based upon the working pattern, nature and the underlying architecture of digital circuits. Digital Circuits contains various varieties correspondent to their working behaviour and some primary components such as Logic Gates (AND, OR, NOR, XOR, XNOR, NOT etc.), Flip-Flops (S-R, J-K, T, D), Counters, Multiplexers, De-Multiplexers, Encoder Decoder and Registers etc. These primary components are responsible to makeup the architecture of any Digital Circuits. In this paper we generally proposed four new flip-flops, their mechanisms, characteristic table and their logic expressions as well. The working mechanisms and the computational behaviour of these all four flip-flops about their working methodology or mechanisms and their bit storing patterns are detailed describing in the upcoming sections of this paper. The first two newly flip-flops have capability that they behave or works as a buffer to store same bit pattern in the remaining states which occurred previously, but next remaining two works different relative to these first two. The next remaining two flip-flops are also storing same data bit patterns in the remaining states which occurred previously, but these tendency will occur for only some input data bit patterns, but for some other remaining data bit patterns it's stored '1s' for some input data items and complements of some previously occurred data as well.

KEYWORDS: Flip-Flops, Digital Systems, Digital Circuit Component, Primary Digital Circuit Components.

I.INTRODUCTION

Digital Electronics [1] play's a major role in the age of computing. All Computing taxonomy and mechanisms are strictly dependent on the fundamental functionality of digital circuits and their working patterns. Digital circuits [2] contains various electronic components such as Logic Gates, Flip-Flops, counters, multiplexers, de-multiplexers, encoder, decoder etc. Generally In a broad spectrum all digital circuits are classified into two major categories such as combinational circuits [3] and sequential circuits [4] based on their functionality. In a combinational circuits [3, 11] outputs are generally depend on any of the current inputs, but In the sequential circuits [4] outputs are depend on all of the inputs and some previously occurring inputs. In this paper we generally designed four universal restoring flip-flops [5, 6, 18]. In this four new flip-flops [5, 6, 13], first two flip flops [5, 6, 18] are working as a buffer, its stores all previously occurred bits as same as in the remaining patterns, It's doesn't contains any invalid patterns. Because we also known that flip-flop [5, 6, 18] works as a memory element and it's generally stores one bit number, but various previously designed flip-flops such as S-R flip-flop [7, 12, 17] and J-K flip-flop [8, 12] gives some invalid or unsatisfactory patterns corresponding to some inputs, but In this newly designed flip-flops [5, 6, 18] the same pattern or

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generally same bits occurred in the remaining state, which stores previously in this flip-flops. Because S-R [7] and J-K flip-flops [8] gives many heterogeneous results such as complement of previously stored bits, or sometimes '0' or '1', but In these newly designed flip-flops [5, 6] all results which will occur in the remaining state are as same as the previously occurred results, and we can say generally that it's works as a buffer and a memory element. Because flip-flops [5, 6, 14] play's a varieties of role in the taxonomy of digital circuits architecture and its functionalities. Because all Arithmetic Logic Unit (ALU) are generally based upon the Registers [9, 10, 16] and all registers are make up with the well-defined collection of flip-flops. Because generally at the time of computations and the processing of arithmetic or logical data, all intermediate results are stored in Accumulator Register (AC) and this registers a contains of size 8 bits, based on the microprocessor version or generally depend on the word length of your computer. Generally 8085 microprocessor contains a 8 bit Accumulator Register (AC). So flip-flops play's a versatile role in the architecture of microprocessor or digital circuits, because all microprocessor are designed with the fundamental architecture of digital circuits and flip-flops play's a significant role in the architecture of digital circuits. In the T and D flip-flops also restoring bit, but to store all previously occurred bits or those bits, which previously stored in the flip-flop are occurring as same as in the remaining states, this tasks accomplished this only newly designed first two flip-flops [5, 6, 14]. The detailed working mechanism and bits pattern of these flip-flops are described in the upcoming sections of this paper. The next two flip-flops also provides satisfactory results, but these flip-flops doesn't stored all previously occurred bit values, these flip-flops generally occurred some previously bits in the remaining patterns and also occurred '1' for some input bit patterns and complements of previously input data bits as well. In the first flip-flop we generally used XOR (Exclusive-OR) gate, AND gate and OR gate to achieve this versatile flip-flops [5, 6] which occurred same bit patterns in the remaining states which occurred previously. But In the next flip-flop we generally used XNOR or (Exclusive NOR) gate, NOR gate, AND gate to achieve the same bit patterns in the remaining states which would occurred in the previous states and these first two buffers works as a buffer because all bits which will stored in the flip-flop in the previous states, the same bits are stored in the remaining states of the flip-flops [5, 6]. That's why its works as a buffer or memory element for any digital circuit [19], because all those bit patterns which occurred previously in the flip-flop [20], the same are stored in the remaining states of the flip-flops. The next flip-flop excluded first two contains XNOR or (Exclusive-NOR) gate, AND gate to store some previously occurred data bits in the remaining state of this flip-flops, but all bits are never stored in the remaining state which occurred previously in the flip-flop, here some '1s' are also occurred some data inputs and the next flip-flop [5, 6, 15] contains XNOR (Exclusive-NOR), OR, AND gate for storing some previously occurred data bits in the remaining state, but all previously occurred data bits are never stored in the current state of the flip-flops, here some complement of the previously occurred data its correspondent to some data inputs as well. So In this paper the detailed of these 4 flip-flops are have to be discussed in the upcoming section of this paper.

II.SOME PREVIOUSLY DEVELOPED CONVENTIONAL FLIP-FLOPS

S-R Flip-Flops [5, 6, 17]: Here In the S-R flip-flop [5, 6, 17], here S stands for Set and R Stands for Reset. In this flip flop for many input data items some invalid outputs have to be occurred or In other words we can say that many time for some given data input the S-R flip-flop doesn't restore some previously occurred bits or some same bit patterns, it's fluctuated each instance for those data items. The truth table of S-R flip-flops [5, 6, 17] are as follows:

S	R	Q_n	Q_{n+1}	Y
0	0	0	0	Q_n
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	1
1	0	1	1	
1	1	0	-	invalid
1	1	1	-	

Table 1: S-R flip-flop truth table

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the truth table of S-R flip-flop are represent in this above table, according to this table the S-R flip-flop [5, 6, 17] works as a buffer for only first two data inputs excluded first two input data items, it's never works as a buffer and last two input data items it's gives some invalid outputs. So it's a main drawback of S-R flip-flop [5, 6, 17].

J-K Flip-Flops [4, 8, 11]: The truth table of J-K flip-flop [4, 8, 11] are as follows:

J	K	Q_n	Q_{n+1}	Y
0	0	0	0	Q_n
0	0	1	1	
0	1	0	0	0
0	1	1	0	
1	0	0	1	1
1	0	1	1	
1	1	0	1	$Q_n'\ (toogle)$
1	1	1	0	

Table 2: J-K flip-flop truth table

In this above truth table of J-K flip-flops [4, 8, 11] it's doesn't give a satisfactory results for some data input cases such as for first two data inputs it's works as a buffer, stored same output values which previously occurred but for next two data input items , it's store 0 and for next two it's stores 1 and at the last it's behaviour shows as a complement or toggle, but the main mechanisms of flip-flops is that it's behaves as a buffer and stored same output in the remaining cases which previously occurred, but these outputs occurred first two cases only.

T Flip-Flop [3, 7, 9]: T flip flop works with only one data inputs, for one data inputs we check the behaviour of this T Flip-Flops on 0 and 1. The truth table of T flip-flop [3, 7, 9] are as follows:

T	Q_n	Q_{n+1}	Y
0	0	0	Q_n
0	1	1	
1	0	1	$Q_n'\ (toogle)$
1	1	0	

Table 3: T flip-flop truth table

In this flip-flop for each data item of 0 and 1 we check the behaviour of this flip-flop by given the 0 and 1 in the previously occurred state and check the upcoming or remaining values that it's restored previously value or not in the next upcoming states.
For inputs 0s it's restore the same value which previously occurred, but for 1s it's behave as a complement or toggle, but the main anatomy of flip-flop is that it's acts as a buffers and restore all inputs values which occurred in the previously state.

D Flip-Flop [6, 9, 10]: The truth table of D flip flop [6, 9, 10] are as follows:

D	Q_n	Q_{n+1}	Y
0	0	0	0
0	1	0	
1	0	1	1
1	1	1	

Table 4: D flip-flop truth table

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In this D flip flop [6, 9, 10] it's never works as a buffer, or it's doesn't restore some previously occurred output in the remaining states as the D flip-flop [6, 9, 10] table represents for the data input 0 when we give 0 and 1 as an input for previously occurred output then it's doesn't restore exact same value which previously occurred it's stored only 0 and when for the data input 1 when we give 0 and 1 as the previously occurred output, then it's not restore exact the same output in the remaining state it's restore 1, so this flip-flop never works as a buffer.
So these are some drawbacks of these most significant previously flip-flops, but In the next upcoming section of this paper we would designed a new four flip flops which working mechanisms are similar but their behaviour are different correspondent to the conditions of data inputs. The upcoming section of this paper describe these four novel flip-flops.

III.A NEW PROPOSED FOUR FLIP FLOPS

In this newly designed flip flops, we proposed four flip flops which are as follows:
The first newly proposed flip flop: The diagrammatic representation of this flip flop are as follows:

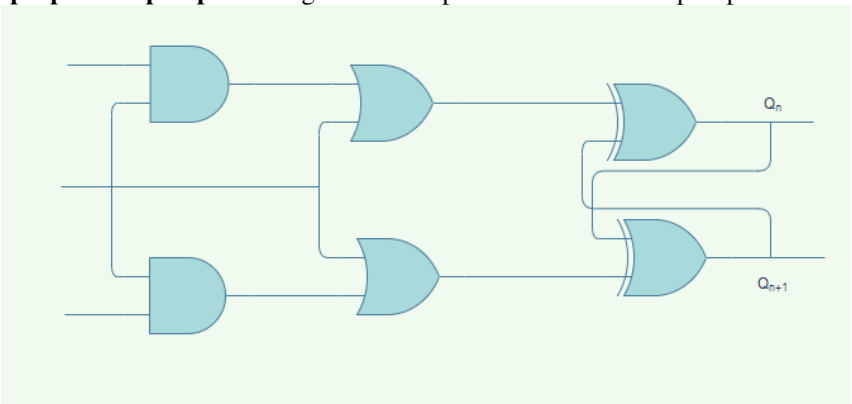

Fig A: first newly proposed flip flop.

In this flip flop we generally used 6 logic gates to accomplish the tasks. Generally these flip flops works as a buffer. The truth table of these flip flop are as follows:

A	*B*	Q_n	Q_{n+1}
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*1*
1	*0*	*0*	*0*
1	*0*	*1*	*1*
1	*1*	*0*	*0*
1	*1*	*1*	*1*

Table 1: Truth table of first newly proposed flip flop.

According to this truth table the Q_n represents the previous state and Q_{n+1} represents the remaining state. For each data input the values which placed on the previous state Q_n the same values would occur in the upcoming state or remaining state which is Q_{n+1}. Here this flip flop work as a buffer because values which occurred in the previous state the same values will occurred in the remaining state and flip flop works as a memory element. The diagrammatic representation of this flip flops are demonstrated in Fig A. Here In this figure when the system clock value are 0 then this flip flop cut off from the system, but when we will set system clock (SYS CLK) value as 1, then this flip flop works smoothly and reliably. For each data input but pattern when we put the value of 0 or 1 in the previous state the same values would occur in the remaining state. So here these flip flops works as a buffer or In other words we can say that it's acts as a memory element. The function table of this flip flop are as follows:

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A	*B*	*Y* (Q_{n+1})
0	*0*	Q_n
0	*1*	Q_n
1	*0*	Q_n
1	*1*	Q_n

Table 2: function table of first newly proposed flip flop.

According to this function table for the input S=0 and R=0, S=0 and R=1, S=1 and R=0, S=1 and R=1 it will give the same values in the remaining states which occurred previously and flip flop works as a buffer and a memory element. So this is the mechanisms of first newly proposed flip flop. The characteristic equation of this flip flop are as follows:

$Q_{n+1} = Q_n$

Here $Q_n$represents the previous state, and Q_{n+1} represents the upcoming state. So they both are equal and working as similar to buffer, so this newly proposed flip flop purely worked as a memory element. So this is the main mechanisms of this newly proposed flip flop.

The Second newly proposed flip flop: The diagrammatic representation of this newly proposed flip flop are as follows:

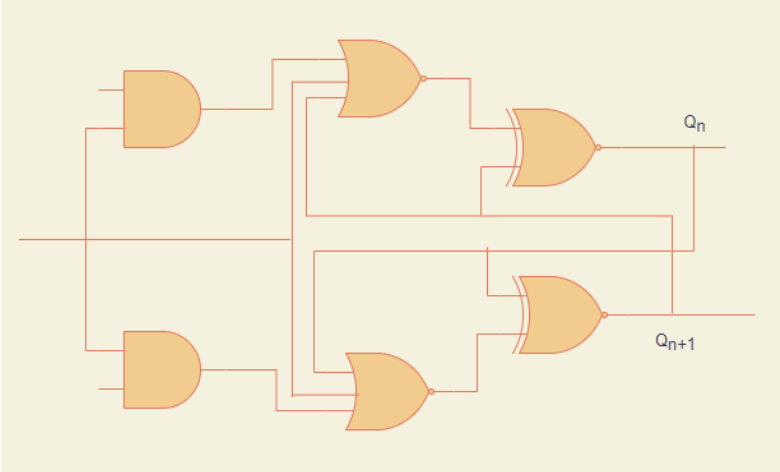

Fig B: second newly proposed flip flop.

In this flip flop 6 logic gates are used to accomplish the tasks, here two AND gate and two NOR gate and two XNOR (Exclusive NOR) gates are used to accomplish the desired task. In this diagram we set clock pulse or system clock as 1, because for value 0 it's cut off to the outside environment. The truth table or characteristic table of this flops are as follows:

A	*B*	Q_n	Q_{n+1}
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*1*
1	*0*	*0*	*0*
1	*0*	*1*	*1*
1	*1*	*0*	*0*
1	*1*	*1*	*1*

Table 3: Truth table of second newly proposed flip flop.

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According to this flip flop truth table and diagrammatic representation, we would easily seen that data input values which occurred in the previous states , the same values will occurred in the remaining state and this flip flop works as an independently and behave as a buffer and memory element . Here In this paper we generally proposed the four novel flip flops correspondent to their working environment and task oriented mechanisms. Here we would make all possible combinations of 0 and 1 and also switch 0 and 1 in the previous state Q_n and examine the behaviour of the flip flops, that it's work properly or not?
The function table of this flip flop are as follows:

A	*B*	*Y* (Q_{n+1})
0	***0***	Q_n
0	***1***	Q_n
1	***0***	Q_n
1	***1***	Q_n

Table 4: function table of second newly proposed flip flop.

The function table of this second newly proposed flip flop are represented in the table 4, according to this function table we take two generalized input lines which are A and B and we provide all data input possible combinations and a values which occurred or which stored flip flop in the previous state the same value will occurred in the remaining state which represents in the table 4 by Y here Y represents Q_{n+1}. As the table 4 represents that flip flops works as a buffer and memory element which is the main mechanisms of the flip flop.
The Characteristic Equation of this flip flop are as follows:

$$Q_{n+1} = Q_n$$

Here the characteristic equation of these newly proposed flip flop the same values which occurred in the previous states will occurred exactly in the remaining state and flip flops works as a buffer or memory element. So this is all about the mechanisms of second newly proposed flip flop.
The Third newly proposed flip flop: The diagrammatic representation of this flip flop are represent in the Fig C.
Here we used two AND and two XNOR (Exclusive NOR) gate are used to accomplished the tasks.

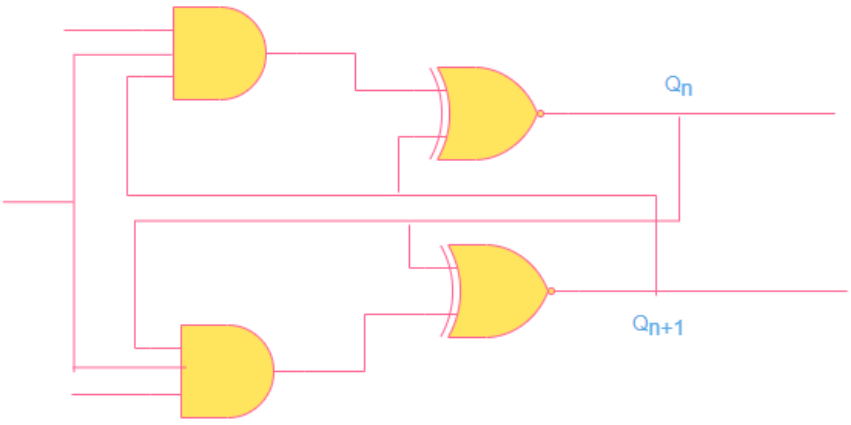

Fig C: Third newly proposed flip flop.

In this flip flop it never works as a buffer or memory element, but In this flip flop we doesn't get any invalid state, It's also gives the same values in the remaining state which occurred in the previous state for some data inputs and for some data inputs it gives value o and for some other data inputs it will give value 1.

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The Characteristic table or truth table of this flip flop are represented in the table 5:

A	*B*	Q_n	Q_{n+1}
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*1*
1	*0*	*0*	*1*
1	*0*	*1*	*1*
1	*1*	*0*	*1*
1	*1*	*1*	*1*

Table 5: Truth table of third newly proposed flip flop.

According to this truth table we would make all combinations of o and 1 with including the previous state values and find out the values patterns in the remaining state. So it's clearly visible that for first four data inputs it's works as a buffer and strong the same values in the remaining state which occurred previously, but for next two states after this it will give value 1 for all data inputs. But the main key point of this flip flop is that it's never give the invalid state as S-R flip flop which also gives invalid state.
The function table of this flip flop are as follows:

A	*B*	$Y(Q_{n+1})$
0	*0*	Q_n
0	*1*	Q_n
1	*0*	*1*
1	*1*	*1*

Table 6: function table of third newly proposed flip flop.

So these are the function table of this flip flop, According to this generalized function table for A=0,B=0 and A=0,B=1 it will give the same value which occurred previously and for A=1, B=0 and A=1, B=1 it will give value 1.
The characteristic equation of this flip flop are as follows:

$$Q_{n+1} = Q_n + AQ_n'$$

This is the characteristic equation of this flip flop,, here

Q_n *represents the previous state value and* Q_{n+1} *represents the remaining state value.*

The Fourth newly proposed flip flop: The diagrammatic representation of this fourth newly proposed flip flop are as follows:

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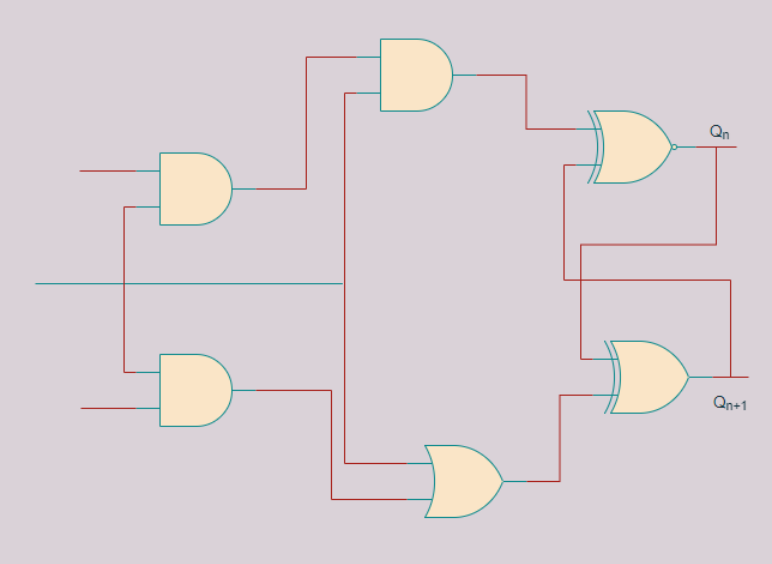

Fig D: Fourth newly proposed flip flop.

In this flip flop we used 6 logic gates for accomplish the desired task. Here we used three AND gate, one OR gate, one XNOR (Exclusive NOR) gate and one XOR gate. This flip flop also works as a buffer for some data inputs but not for all inputs but for the remaining inputs it's also gives 0 and 1 and also gives complement or toggling for some data inputs. The characteristic or truth table of this flip flop are as follows:

A	*B*	Q_n	Q_{n+1}
0	*0*	*0*	*0*
0	*0*	*1*	*1*
0	*1*	*0*	*0*
0	*1*	*1*	*1*
1	*0*	*0*	*1*
1	*0*	*1*	*0*
1	*1*	*0*	*1*
1	*1*	*1*	*0*

Table 7: Truth table of fourth newly proposed flip flop.

According to this truth table for first four data inputs it's behave as a buffer and gives the similar values in the remaining state which occurred previously. But excluded these first four data inputs remaining four data inputs it's shown the complement behaviour or generally toggling. So the main key point of this flip flop is that it's never give any invalid state like S-R flip flop which gives some invalid results for last two data inputs. It's also shown the complementary behaviour and generally do the toggling for some data inputs. The generalized function table of this flip flop are as follows:

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A	*B*	*Y* (Q_{n+1})
0	***0***	Q_n
0	***1***	Q_n
1	***0***	Q'_n
1	***1***	Q'_n

Table 7: function table of fourth newly proposed flip flop.

According to this function table for value A=0, B=0 it will gives the same values in the remaining state which occurred previously and behave as a buffer and a memory element, but next remaining two data inputs such as A=1, B=0 and A=1, B=1 it will shown or gives the complementary behaviour or generally do the toggling. So these are the main concepts of this fourth newly proposed flip flops.
The characteristic equation of these newly proposed flip flop are as follows:
Characteristic equation
$Q_{n+1} = AQ'_n + A'Q_n$
Or
$Q_{n+1} = A\ XOR\ Q_n$
This is the characteristic equation of this flip flop,, here

Q_n *represents the previous state value and* Q_{n+1} *represents the remaining state value.*

So this is all about this fourth newly proposed flip flop.

IV. COMPARISON CHARTS

Comparison charts among truth tables of various flip flops:

Inputs			*S-R Flip Flop*	*J-K Flip Flop*	*First new flip flop*	*Second new flip flop*	*Third new flip flop*	*Fourth new flip flop*
A	***B***	Q_n	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}	Q_{n+1}
0	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*1*
0	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*
0	*1*	*1*	*0*	*0*	*1*	*1*	*1*	*1*
1	*0*	*0*	*1*	*1*	*0*	*0*	*1*	*1*
1	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*0*
1	*1*	*0*	*Invalid*	*1*	*0*	*0*	*1*	*1*
1	*1*	*1*	*Invalid*	*0*	*1*	*1*	*1*	*0*

Table 8: Comparison charts of truth tables of various flip flops and newly proposed flip flops.

Comparison charts among function tables of various flip flops:

Input		**S-R Flip Flop**	**J-K Flip Flop**	**T Flip Flop**	**D Flip Flop**	**First New flip flop**	**Second New Flip Flop**	**Third New Flip Flop**	**Fourth New Flip Flop**
A	**B**	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})	**Y** (Q_{n+1})
0	0	Q_n	Q_n	Q_n	*0*	Q_n	Q_n	Q_n	Q_n
0	1	*0*	0			Q_n	Q_n	Q_n	Q_n
1	0	*1*	1	Q'_n	*1*	Q_n	Q_n	*1*	Q'_n
1	1	*invalid*	Q'_n (*toogle*)			Q_n	Q_n	*1*	Q'_n

Table 9: Comparison charts of function table of various flip flops and newly proposed flip flops.

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This is the comparison charts of all about flip flops and newly proposed flip flops.

V. FUTURISTIC SCOPE AND IT'S APPLICATIONS

In the Concepts of Digital Systems some basic and fundamental components play's a very major and significant role to accomplish any computational tasks in reliable and adequate manner with fastest response time. But there are many overheads about the fundamental and primary components of Digital Systems. In this paper we proposed four flip flops which contains same mechanisms but adopt different behaviour correspondent to the input data items. But In the previously developed flip flops none of behave or worked as a buffer, because but here In this paper the first two flip flops works as a buffer and stored the same output in the upcoming states which occurred previously, but the main theme and key point of this flip flop is that these flip flop stored all data bits in the upcoming states which occurred previously. These newly first two flip flops out of the four worked as a buffer which is the main mechanisms of the flip flops. In the near future there are many advancements have to be done in all these four flip flops, such as we also known that if the number of primary components which make up the flip flops drastically increases then the component resistance and delay's also would be occurred, In this paper we would generally use approximately 5 or 6 logic gates to designed four novel flip flops, but In the near future we also accomplish these tasks using the minimum number of logic gates such that no resistant and delay have to be occurred.

Flip Flops are the very basic and significant components of any Digital Systems and Digital Circuits because flip flops works as a memory element to store a one bit of information but it's also plays a significant role to design and develop registers because registers contains the integration of various flip flops and it's also worked as an memory element for digital systems. But In the context of some previously developed flip flops it's gives satisfactory results or restore some previously occurred data bits for only some set of input data but for some remaining set of input data it's behave abnormally and never gives a satisfactory results because the main mechanisms of the flip flops are that it's acts as a buffer for any digital systems and stored the same values which occurred previously. But the one main challenging concern is that we developed the same mechanisms using the minimum number of logic gates such that no larger resistance and delay have to be occurred.

There are many advancements have to be done in the near future such as if we developed any flip flop which works as a buffer and also contains minimum number of logic gates then it's response time and value fetching time much faster as relatively to compare with other flip flops because minimum delay have to be possible due to minimum number of logic gates because this is the main disadvantage of logic gates such as delay's occur in a very huge quantity because values fetching and values holding in a flip flop are a very time consuming tasks due to the large amount of logic gates are used, so In the near future if we optimize the number of logic gates in the flip flops, so the effect of resistance harm some number of bits and never occurred any delay and all Digital systems works properly and reliably.

VI. CONCLUSION

In the analogy of flip flops there are various flip flops are also available for designing the Digital Systems, but it's a most challenging tasks to design a flip flop which gives the same output in the remaining states which occurred previously and worked as a buffer or memory element, but In this paper we would designed for new flip flops which gives the same output in the remaining states which occurred previously and also worked as a buffer or memory element, but a one main challenging tasks is that these task accomplish using the minimum number of 6 logic gates approximately which direct to the concerns of the major delay's and a huge resistance occurs which effects some number of bits, but there are various advancements done in the near future about the minimum number of gates will use to accomplish these tasks. Flip Flops play's a versatile and a significant role in the designing of digital systems because flip flops are generally used to storing one bit of information and Registers contains a well-defined collection of flip flops for storing significant information. All Digital Systems mechanisms are dependent on the primary components such as Logic gates and Flip Flops, Counters, Multiplexers, De-Multiplexers etc. So the reliability and accuracy of the Digital Systems are totally dependent on the primary and fundamental components. In this paper these four flip flops also reliably worked with positive edge triggered flip flop or negative edge triggered flip flops, the accuracy and the adequateness of these four flip flops are outstanding, because In the first two flip flops works as a buffer or memory elements and storing same data bits which occurred previously but the next two flip flops are not purely worked as a buffer, for some input data values it's generate 0s and 1s and sometimes complement and toggling. It's a very challenging tasks that e designed or to develop any digital systems using the minimum number of logic gates and direct to optimality because if we designed and developed any digital systems using the maximum or large number of logic

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gates then the resistance and delay's also would be occur because resistance effects some data bits and the meaning of the information have been changed and for fetching there are some delay's occur about the processing and starting of logic gates. So it's mandatory to design any digital systems using the minimum number of logic gates. All previously developed flip flops such as S-R flip flop and J-K flip flop, T and D flip flop also gives satisfactory results but these flip flops also gives some invalid outputs correspondent to some data inputs, so these are the main drawback of these flip flops. All previously developed flip flops never worked as a buffer or memory element, but In this newly developed flip flops first two flip flops out of four also worked as a buffer or memory element this is the main key point and significant factor of these flip flops. In the near future various research advancements have to be done in this flip flops such as we accomplish these tasks that flip flops works as a buffer using the minimum number of logic gates such that no resistance and delays have to be occur during computations and direct to optimality. Because all the working mechanisms and computational tasks of Digital Systems are totally depend upon the primary and fundamentals elements of digital design such as the Logic Gates, Flip Flops, Counters, Multiplexers and De-Multiplexers etc. so it's mandatory to optimize the computational cost of these primary elements such that the digital systems works properly and reliably.

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IX. CONFLICT OF INTEREST

The authors declare that they have no conflict of interest.

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BIOGRAPHY

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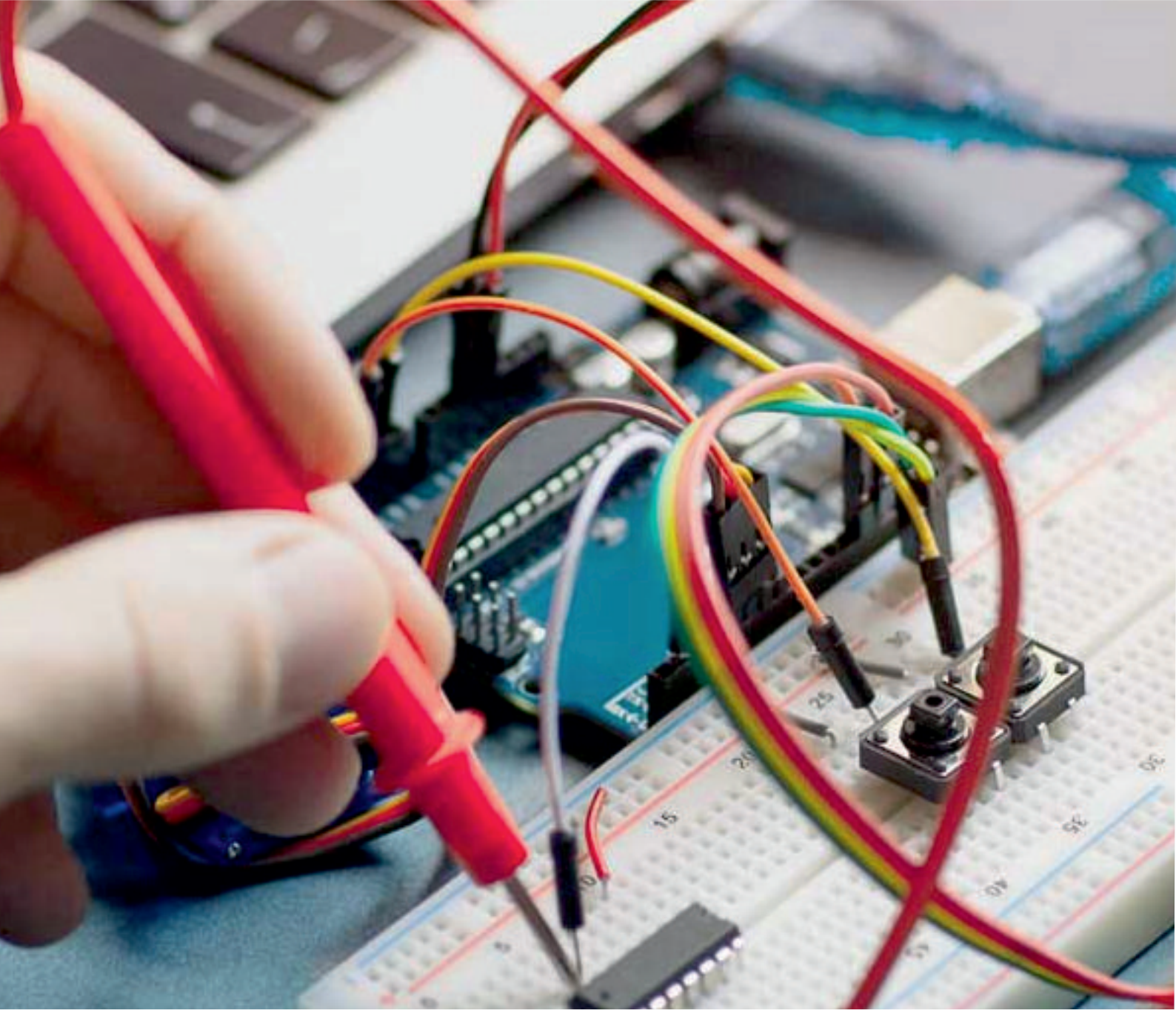

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