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Comparative Analysis of 33 level Asymmetrical Cascaded H Bridge Inverter Using Different LS-PWM Techniques

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ABSTRACT:The multilevel inverters have become popular due to various advantages like better harmonic quality, staircase waveform, reduced electromagnetic interference etc.. Many industrial applications use MLIs. Various level shifted PWM techniques are popular for control of multilevel inverters. This paper presents the comparative analysis of various level shifted multicarrier PWM techniques like Phase Disposition Pulse Width Modulation (PDPWM), Alternate Phase Opposition Disposition Pulse Width Modulation (APODPWM), Variable Switching Frequency Pulse Width Modulation (VFCPWM) control techniques for operation of 33 level Cascaded H Bridge Multilevel inverter is done. The decimal to binary conversion technique to generate pulses for different switches is employed. The Total Harmonic Distortion, are compared and results are presented. The topology is suitable for medium to high power applications.

KEYWORDS: Asymmetrical Cascaded H Bridge Multilevel Inverter (ACHBMLI), Multilevel Inverter (MLI), Level Shifted Pulse Width Modulation (LSPWM), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD).

I.INTRODUCTION

Inverters are type of power electronic devices which converts an DC signal to AC signal, for uses in various commercial and home applications like UPS, FATCS, grid integration of PV,WECS and adjustable speed drives etc.. Multilevel inverters produce multiple output levels in staircase form in the shape of sinusoidal waveform. It has added advantages of lower THD, lower electromagnetic interference (EMI), lower switching losses etc.. As the world moves towards renewable sources of energy, there is an increasing demand of inverters with higher power rating, better power quality with lower harmonic distortions and lesser EMIs. multilevel inverters have the ability to satisfy these demands. Thus, there is an increased focus on development of MLIs with better harmonic performances, power capacity, modularity, lower losses etc.. to cater to the increasingly diverse applications of MLIs.

The Multilevel Inverter are broadly classified into three types based on switches configuration. They are:

1. Diode Clamped Multilevel Inverters
2. Flying Capacitor Multilevel Inverters
3. Cascaded H Bridge Inverters

The diode clamped multilevel inverters are also known as neutral point clamp inverter use diodes, capacitors and switches to achieve desired output. The advantages of this inverter is that is uses relatively simple control technique, and distortion decreases with increased number of levels. However, the output voltage is half of dc input voltage and the large number of clamping diodes are required to obtain higher levels.

The Flying Capacitor multilevel inverter uses combination of capacitors and switches to get desired output. It does not use diodes, and filters can be avoided. Flying capacitor multilevel inverter can control both active reactive power flow, with added advantage of large amount of packing capacity. However, switching losses are high and inverter control is complicated.

The Cascaded H bridge multilevel (CHB) inverter is made up of single H bridge combined with a series of power conversion cell. CHB MLIs have various advantages over NPC and FC MLIs, it uses less number of components for each level of output. It doesn't require filter to produce outputs with lesser THD values. The only disadvantage is that it requires isolated DC voltage sources.

The Cascaded H bridge multilevel inverters can be classified into two groups based on the value of dc sources. They are: (1) Symmetrical Cascaded H Bridge Multilevel inverter: This inverter consists of H bridge connected to series level generating circuit with DC sources of equal magnitude (1:1:1:1) therefore it requires higher number of dc sources

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to generate higher number of levels. (2) Asymmetrical H Bridge Multilevel inverter uses dc sources of unequal magnitude (1:2:4:8) in level generating circuit. It allows generation of higher levels with equal number of dc sources as Symmetrical cascaded H Bridge Multilevel inverter with lower THD value. Thus, Asymmetrical CHBs give superior performance and will be used as an inverter of choice for this paper.
There are different PWM techniques to generate gate pulses in order to control the switches of the inverter. Figure 1.1 shows different PWM techniques available. High switching Frequency for high switch frequency PWM is considered above 1 KHz.

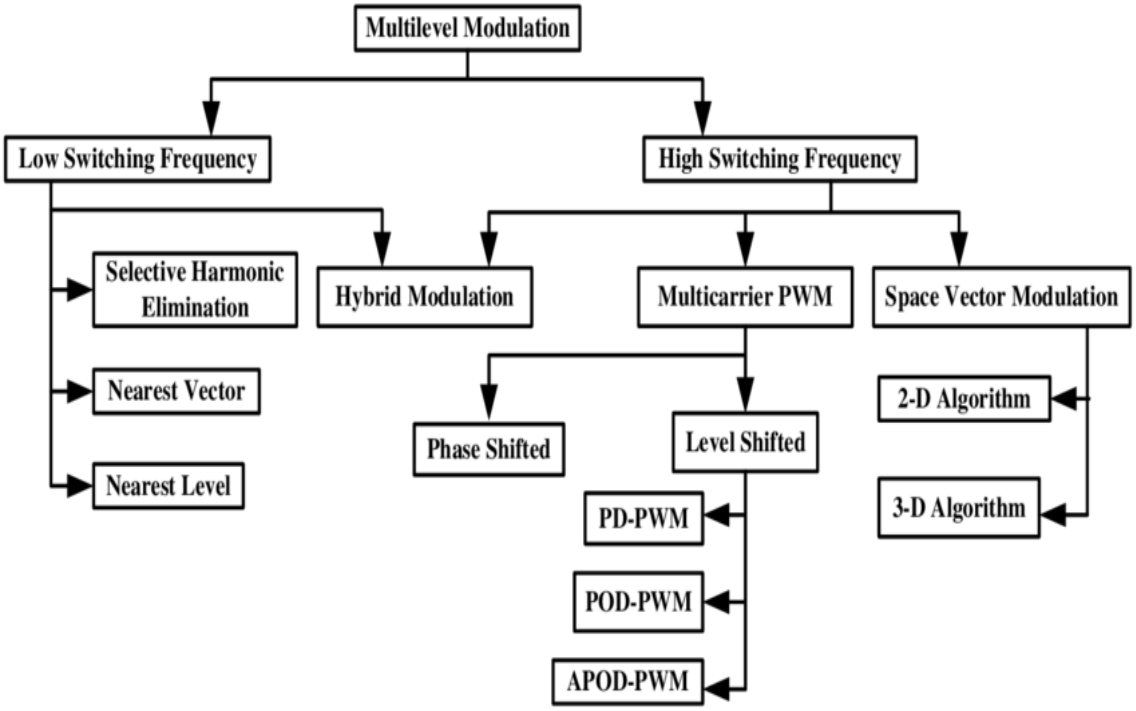

Figure 1.1: Classification of Modulation techniques for Multilevel Inverter

Multicarrier PWM (MC-PWM)
Multiple Carrier Pulse Width Modulation switching technique is utilized to generate output of more than three levels. The working principle of carrier PWM techniques is that it compares a reference waveform, usually a sine waveform with carrier waveform. MC PWM utilizes more the one carrier signals to produce gate signals. The switching frequency of the inverter is determined by the carrier frequency. All carrier signals are continuously compared with reference signal, and if the reference signal is more than the carrier signal, the controller gives an turn on signal to the switches. The MCPWM are techniques further classified to two types: Level Shift Pulse Width Modulation (LS-PWM) and Phase Shift Pulse Width Modulation (PS-PWM).

Level Shifted PWM (LS-PWM):
In this technique, N-1 carrier signals are vertically shifted to each other. There are different types level shifted PWM techniques given below:

Phase Disposition (PD-PWM): Phase Disposition PWM technique uses (n-1) carrier signals to generate pulses to produce n level output and all the carrier signals are in phase with each other.

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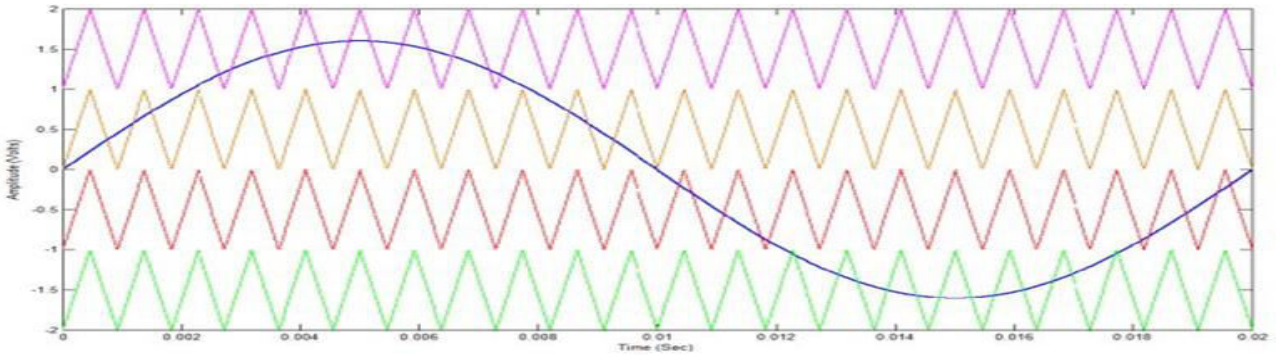

Figure 1.2 (a): Phase Disposition PWM

Phase Opposition Disposition (POD-PWM): Phase Disposition PWM technique uses (n-1) carrier signals to generate pulses to produce n level output and the carrier signals are having 180º phase shift below the x-axis.

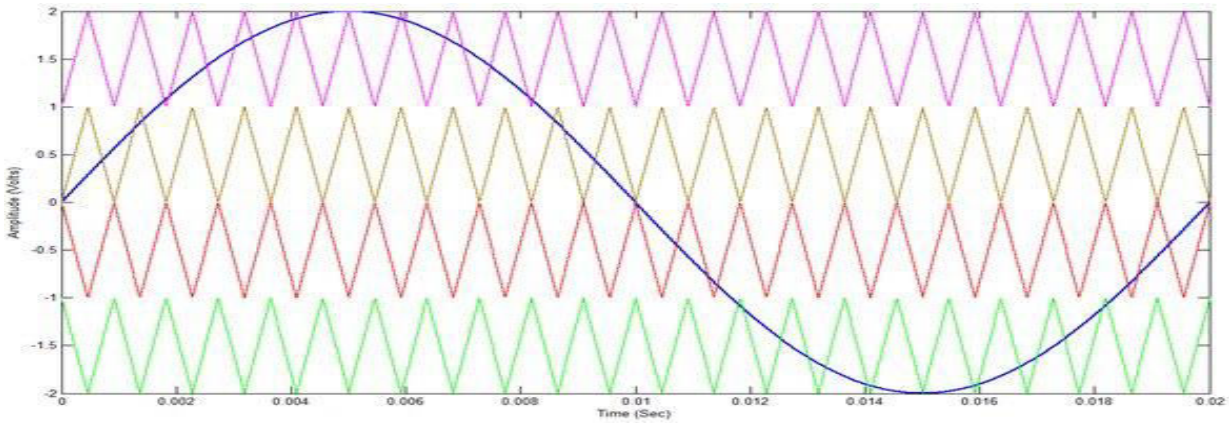

Figure 1.2 (b): Phase Opposition Disposition PWM

Alternative Phase opposition Disposition (APOD-PWM): Phase Disposition PWM technique uses (n-1) carrier signals to generate pulses to produce n level output and all the carrier signals are having 180º phase shift with respect to each other.

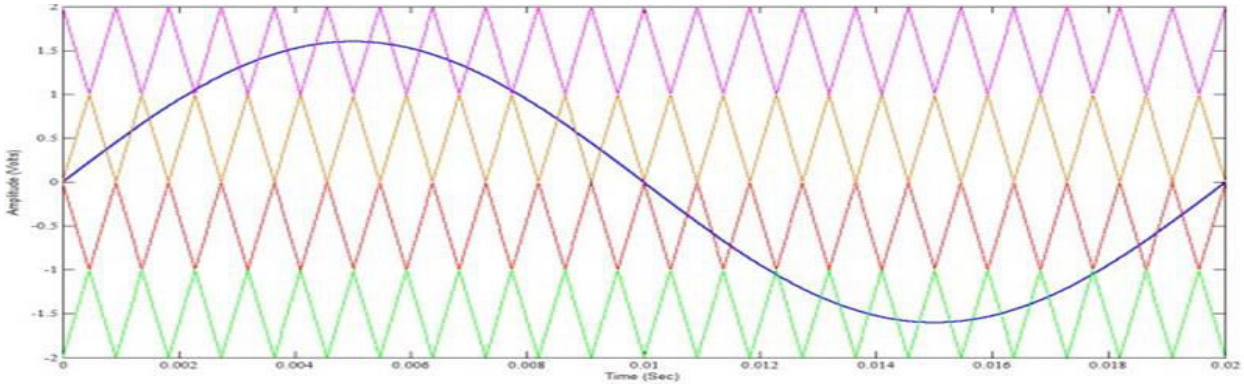

Figure 1.2(c): Alternate Phase Opposition Disposition PWM

Variable Frequency Carrier (VFC-PWM): In Variable Frequency Carrier, the carrier signals above and below x axis have decreasing order of frequency with respect to adjacent carrier signal.

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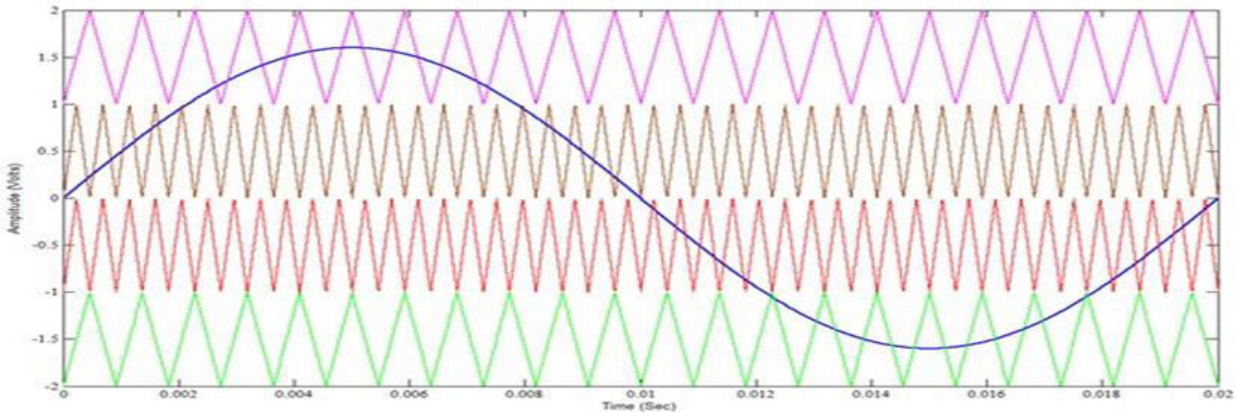

Figure 1.2(d): Variable Frequency Carrier PWM

The 33-level multilevel topology studied in this paper, uses absolute sine wave as a reference. Hence, only PDPWM,APODPWM andVFCPWM techniques are chosen for comparative analysis of their performance.

II.33 LEVEL MLI TOPOLOGY

The Asymmetrical CHBMLI used in this paper can generate 33 level output using bidirectional switches and diode. The topology has a polarity changing H Bridge connected to series connected level generating half bridges. Topology utilizes five DC voltage sources with ratio of (1:1:2:4:8). The switches used are IGBT. This configuration allows generation of higher levels with same number of dc sources as symmetrical CHBs. Figure 2 shows the circuit diagram of the 33 level ASCHBMLI with R Load.

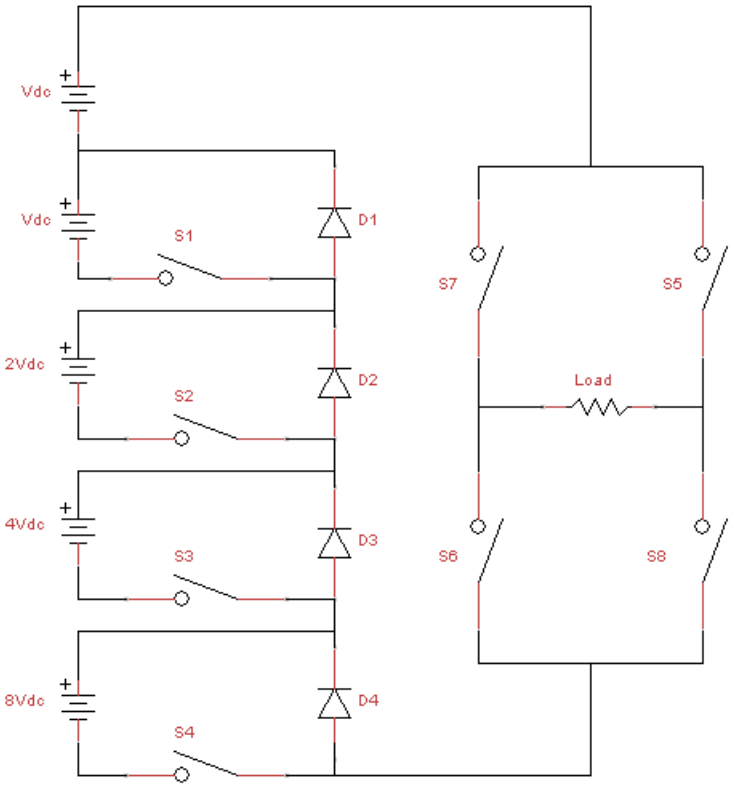

Figure 2: Schematic Diagram of the 33 level Multilevel Inverter

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The topology consists of eight switches, where four switches S5,S6,S7,S8 make up polarity reversing H bridge and S1,S2,S3,S4 make up level generating circuit. The H bridge changes its polarity every half cycle where, S5,S6 are turned on (and S7,S8 are off) to get positive polarity and S7,S8 are turned on (and S5,S6 are off) to get negative polarity. Switches S1,S2,S3,S4 are turned on by gate circuit to obtain various voltage levels in staircase form.

2.1 Control Strategy:

In the LSPWM technique, there are two types of signals, a reference sine wave and multiple carrier waves of high frequency. The voltage of each carrier signal is vertically shifted with respect to each other (level shifted).

Multiple carrier waves are compared with absolute sine wave having maximum amplitude of 16V. A total of sixteen carrier signals with amplitude of 1V are generated for modulation. Each are level shifted and other parameters like phase shift, frequency is decided based on the switching techniques used. The two signals are compared using a comparator block, and the output of the comparator is applied to decimal to binary conversion block,which is configured based on the switching table to generate switching pulses for each voltage levels. The gate pulses control the switching of IGBT switches. Switching table for the inverter is given in table 1.

The switching frequency of the carrier waves are chosen to be 10KHz and reference sine wave is generated at frequency of 50Hz.

Output Voltage	Conducting Switches								Conducting Diodes			
	S1	S2	S3	S4	S5	S6	S7	S8	D1	D2	D3	D4
16Vdc	1	1	1	1	1	1	0	0	0	0	0	0
15Vdc	0	1	1	1	1	1	0	0	1	0	0	0
14Vdc	1	0	1	1	1	1	0	0	0	1	0	0
13Vdc	0	0	1	1	1	1	0	0	1	1	0	0
12Vdc	1	1	0	1	1	1	0	0	0	0	1	0
11Vdc	0	1	0	1	1	1	0	0	1	0	1	0
10Vdc	1	0	0	1	1	1	0	0	0	1	1	0
9Vdc	0	0	0	1	1	1	0	0	1	1	1	0
8Vdc	1	1	1	0	1	1	0	0	0	0	0	1
7Vdc	0	1	1	0	1	1	0	0	1	0	0	1
6Vdc	1	0	1	0	1	1	0	0	0	1	0	1
5Vdc	0	0	1	0	1	1	0	0	1	1	0	1
4Vdc	1	1	0	0	1	1	0	0	0	0	1	1
3Vdc	0	1	0	0	1	1	0	0	1	0	1	1
2Vdc	1	0	0	0	1	1	0	0	0	1	1	1
1Vdc	0	0	0	0	1	1	0	0	1	1	1	1
0Vdc	0	0	0	0	0	0	0	0	0	0	0	0
-1Vdc	0	0	0	0	0	0	1	1	1	1	1	1
-2Vdc	1	0	0	0	0	0	1	1	0	1	1	1
-3Vdc	0	1	0	0	0	0	1	1	1	0	1	1
-4Vdc	1	1	0	0	0	0	1	1	0	0	1	1
-5Vdc	0	0	1	0	0	0	1	1	1	1	0	1
-6Vdc	1	0	1	0	0	0	1	1	0	1	0	1
-7Vdc	0	1	1	0	0	0	1	1	1	0	0	1
-8Vdc	1	1	1	0	0	0	1	1	0	0	0	1

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-9Vdc	0	0	0	1	0	0	1	1	1	1	1	0
-10Vdc	1	0	0	1	0	0	1	1	0	1	1	0
-11Vdc	0	1	0	1	0	0	1	1	1	0	1	0
-12Vdc	1	1	0	1	0	0	1	1	0	0	1	0
-13Vdc	0	0	1	1	0	0	1	1	1	1	0	0
-14Vdc	1	0	1	1	0	0	1	1	0	1	0	0
-15Vdc	0	1	1	1	0	0	1	1	1	0	0	0
-16Vdc	1	1	1	1	0	0	1	1	0	0	0	0

Table 1: Switching Sequence for the 33 level Multilevel Inverter

The Modulation Index gives us information about how much the modulated variable of carrier signal changes around its unmodulated level. The modulation index (Ma) is the ratio of Amplitude of reference wave to the carrier wave.

$$\text{Ma} = \frac{\text{Vref}}{\text{mVc}}$$

Where, Vref – Amplitude of the Reference sine wave.
Vc – Amplitude of the Carrier Wave
m – number of carrier signals

III.SIMULINK MODELING

Simulation Model and parameters which are used is presented in this section. The Figure 3.1 shows the Simulink model.

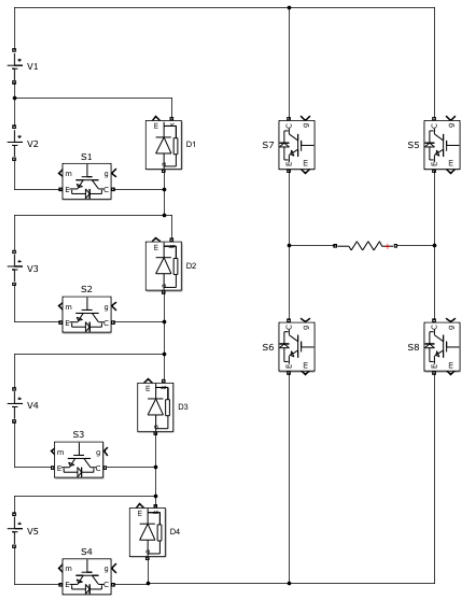

Figure 3.1: Simulink circuit of 33 level multilevel inverter

The value of input DC sources are 21.5V, 43V, 86V, and 172V.The switches are chosen to be IGBT for its high-power handling capacity and is used at switching frequency of 50Hz. The output voltage has a step size of 21.5V. The value of R Load is 100 Ohms and the reference Sine wave is taken with 50Hz as frequency and carrier signals having 10Khz is taken for simulation purpose. The simulated waveforms generate a rms value of 240V with 340V as a maximum positive voltage and -340 maximum negative amplitude.

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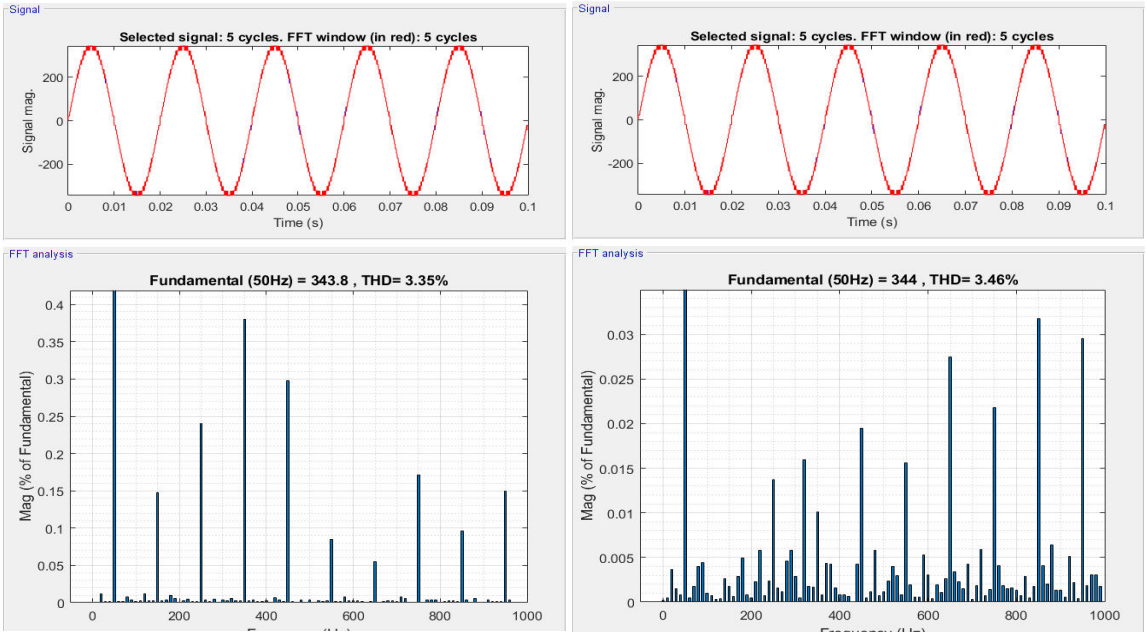
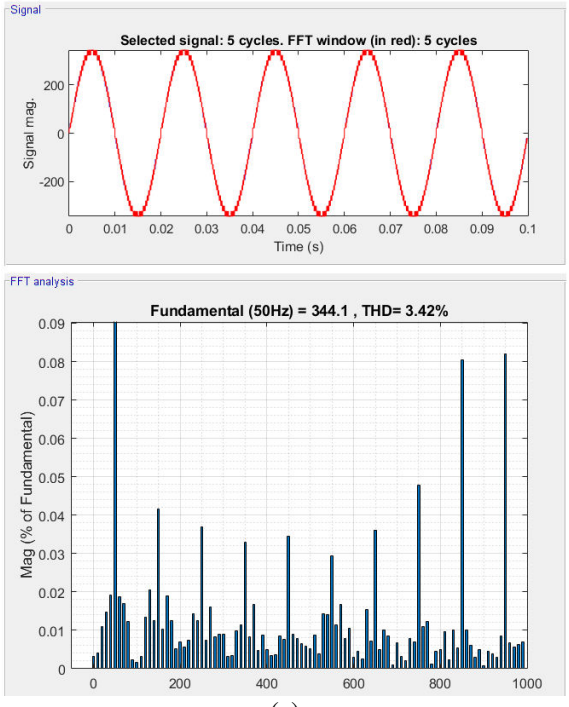
IV.RESULTS AND DISCUSSION

The circuit is simulated with different LS-PWM switching techniques and FFT analysis is done and harmonicspectrum is shown in the figure 3.2. For VFCPWM operation, the carrier signal frequencies are chosen in the order of 10Khz 20Khz,40Khz,80Khz and so on up to the 16th level.



(a) (b)



(c)

Figure 3.2: THD analysis of output voltage waveform using (a) PDPWM (b) APODPWM (c) VFCPWM switching techniques for ma=1.0

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The harmonic spectra is obtained and FFT analysis is done for different LSPWM techniques for different modulation indexes (Ma). The comparison of the THD and rms output voltage for different modulation index values are shown in the table 2.

Modulation Index (Ma)	Performance Parameters	PDPWM	APODPWM	VFCPWM
0.44 (Under-Modulation)	% THD	8.35	8.24	7.44
	Vo (rms)	106.9	106.9	107
0.9	% THD	4.07	4.09	3.87
	Vo (rms)	213.1	213	213
1.0	% THD	3.35	3.46	3.42
	Vo (rms)	243.2	243.4	243.4
1.1 (Over-Modulation)	% THD	5.66	5.58	5.47
	Vo (rms)	262.5	262.1	262.1

Table 2: Performance analysis of different switching techniques

VI.CONCLUSION

In this paper, the 33 level CHB Multilevel Inverter is simulated with Phase Disposition Pulse Width Modulation, Alternate Phase Opposition Disposition Pulse Width Modulation, and Variable Frequency Carrier Pulse Width Modulation and performance of the three techniques are compared with respect to THD values for different modulation indexes. From simulation results, we can conclude that PDPWM technique gives lower THD compared to other methods for ma=1.0 and the Variable Frequency Carrier (VFCPWM) technique gives lesser THD for under-modulation (ma=0.44). Hence, VFCPWM is better technique for operation of inverter in under-modulation conditions and PDPWM is superior for modulation index of 1.0.

REFERENCES

[1] Y. Yu, G.Konstantinou, B.Hredzak, and V. G. Agelidis, "Power Balance of Cascaded H-Bridge Multilevel Converters for Large-Scale Photovoltaic Integration," IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 292-303, 2016.

[2] Malinowski M.. "Recent advances and industrial applications of multilevel converters, IEEE Transactions on industrial electronics", Vol.57, No.8, pp- 2553-2580. 2010

[3] P.Y.Keskar, "Specification of variable frequency drive systems to meet the new IEEE 519 standard ‖ , IEEE Transactions on Industry Applications, vol.32, no.2 pp.393 – 402, March/April 1996.

[4] T.L.Grant and T.H.Barton, "Control strategies for PWM drives", IEEE Transactions on Industry Applications, vol.16, no.2, pp.211-215, March/April 1980.

[5] Y. G. Jung, S. H. Na, Y. C. Lim, and S. H. Yang, "Reduction of audible switching noise in induction motor drives using random position PWM", ‖ IEEE Proc. Inst. Electr. Eng. Electr.Power Appl., vol. 149, no. 3, pp.195 – 202, 2002.

[6] V. Roberge, M. Tarbouchi, and F. Okou, "Strategies to Accelerate Harmonic Minimization in Multilevel Inverters Using a Parallel Genetic Algorithm on Graphical Processing Unit," IEEE Transactions on Power Electronics, vol. 29, no. 10, pp. 5087-5090, 2014.

[7] Young cheol Lin, Young-gook Jung, Jong-namkim and Seog-oh Wi, "A pseudorandom carrier modulation Scheme", IEEE Trans, vol 25, no.4, April 2010.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

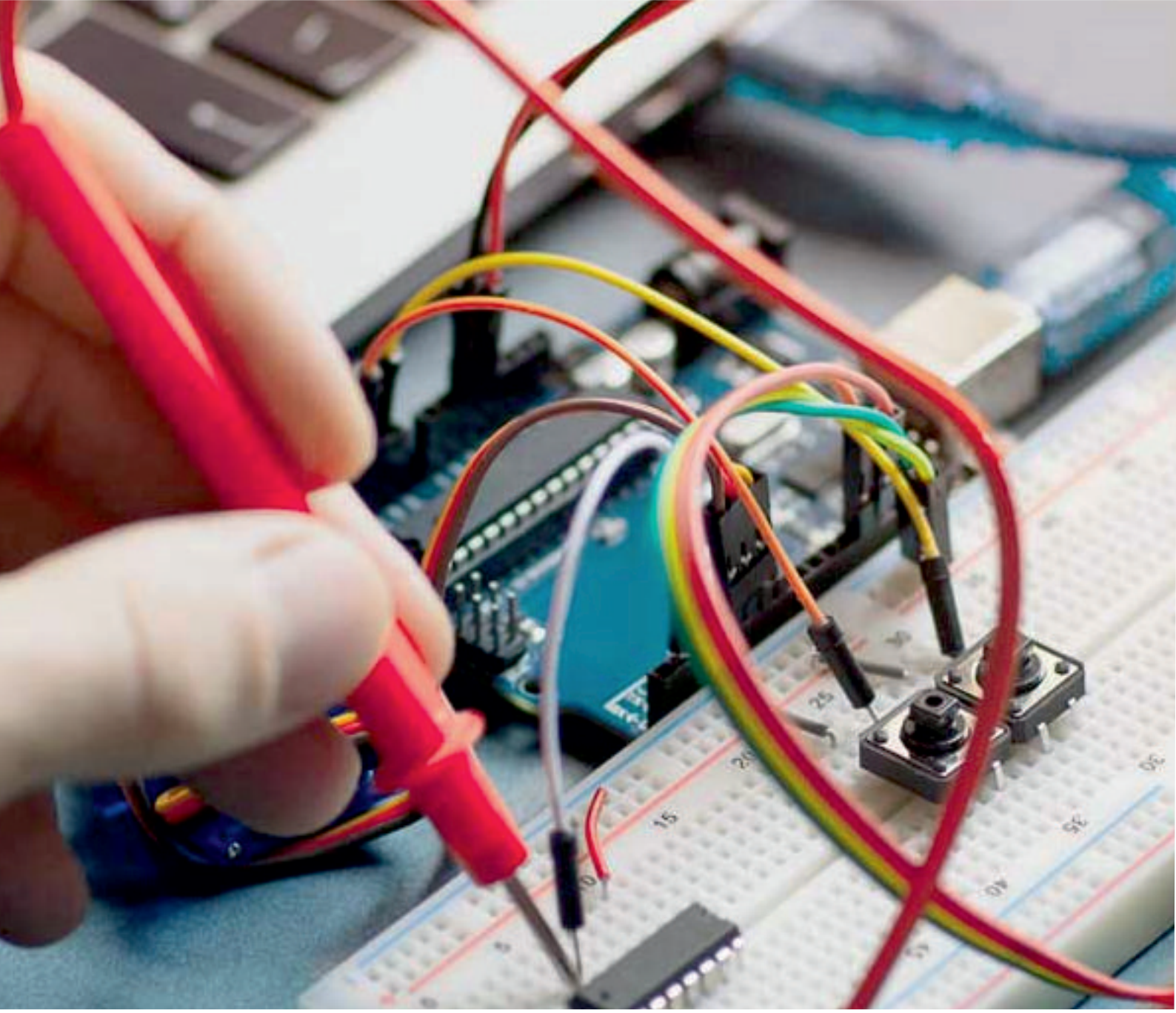
|| Volume 10, Issue 10, October 2021 ||

DOI:10.15662/IJAREEIE.2021.1010006 |

[8] Manoj,T N Raghavendra."A 129-level Asymmetrical Cascaded H-Bridge Multilevel Inverter with Reduced Switches and Low THD". International Journal for Research in Applied Science and Engineering Technology. 9. 1982-1989. 10.22214/ijraset.2021.37697, 2021.

[9] S. Amamra, K.Meghriche, A.Cherifi, and B. Francois, "Multilevel Inverter Topology for Renewable Energy Grid Integration," IEEE Transactions on Industrial Electronics, vol. 64, no. 11, pp. 8855-8866, 2017.

[10] Kyu Min Cho, Won SeokOh,Young Tae Kim, and Hee Jun Kim, "A new switching strategy for pulse width modulation (PWM) power converters", IEEE Transactionson Industrial Electronics, vol.54, no.1, pp.330-337, February 2007.



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