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Survey Paper of High Speed and Low Area Compressor based Adder using XOR-XNOR Gate

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ABSTRACT: The ever growing demand for portable applications like mobile phones and laptops under explosive proportions has made the designers to strive for smaller silicon area, high speed, longer battery life and more reliability. XOR/XNOR gates are the basic building blocks of various digital system applications like adders, multipliers, comparators, ALUs, MAC units, parity generators/checkers and error detection and correction coders etc. In this paper, the studied of different XOR/XNOR logic circuits for two input, three input, multi input, differential outputs, self-checking operation, low voltage working and ternary logic is present.
The studied of two input, three input and multi input circuits are simple and symmetric which used the topology of pass transistor logic and transmission gate logic. All the designs will simulate Xilinx software.

KEYWORDS: - Compressor, Compressor Based Adder, XOR-XNOR Gate, Different Input

I. INTRODUCTION

In the previous not many years, the greater part of the individuals is enchanted by the advanced or parallel rationale. The very idea that a two-esteemed number framework, can be the establishment for the most intense and modern PCs appears to be shocking, without a doubt. Notwithstanding, it is in this way, and the how and the why of these take some clarification. Everything in the computerized world is based along the double number plan. Numerically, this requires only two images: 0 and 1. Legitimately, we can apply these images or we can level them with different images as per the requests of the minute. In this way, when taking care of with computerized rationale, we can characterize that image '0' = Low = False =No and image '1' = High = True =Yes.
Applying this two-esteemed rationale framework, each announcement or status must be either 'genuine' or on the other hand 'bogus': it can't be mostly valid and in part untrue. While this methodology may seem restricted, it has truly come about in pleasantly, and can be spread out to make complex connections and collaborations among any number of person conditions. Information uprightness right now is obviously superior to that of simple structure portrayal on the grounds that here information misfortune includes a subjective change of the state of a gadget, not a float in esteem. That is parcels more uncertain, and there are approaches to make up for it.
A couple of decades prior, people just used to play out some unpredictable things which now PCs do without lifting a finger. Things that require human idea are finished by associating chips made of silicon. This can best be seen with the assistance of Boolean rationale, a rationale, initially made by George Boole in the mid-1800s that permits all in all a hardly any startling things to be mapped into bits and bytes. The ground-breaking thing about
Boolean rationale is that, when you get the progression of things, it is ridiculously basic. It helps in transforming 1's and 0's into important data. A rationale entryway is only a course of action of electrically controlled switches, regularly called as transistors. Every rationale entryway is utilized to speak to a component of a Boolean rationale. An advanced circuit of easy to complex is acknowledged utilizing these rationale entryways.

II. LOGIC GATE

A logic gate is a position of controlled changes used to ascertain tasks utilizing Boolean rationale in advanced circuits. They are fundamentally completed electronically, however can similarly be built utilizing electromagnetic transfers, electronic diodes, liquids, optical or on the other hand even mechanical components. Cardinal attributes of the rationale entryways are:

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- The ability to interface with single or two information wires
- The ability to interface with one yield wire
- The ability to get an incentive from an associated input wire
- The ability to convey an incentive to an associated yield wire
- The capacity to figure right yield esteem, given current info value(s).

The four kinds of fundamental rationale doors are AND, OR, XOR and NOT entryways. With these four, any possible Boolean condition can be gotten through. By the by, for accommodation, the determined kinds NAND, NOR and XNOR are additionally rehearsed, which frequently utilize less circuit components for a given condition than a usage based exclusively on AND, OR, XOR and NOT would do.

III. LITERATURE REVIEW

N. Hamed et al. [1], right now, circuits for XOR/XNOR and concurrent XOR-XNOR capacities are proposed. The proposed circuits are profoundly improved as far as the force utilization and postponement, which are because of low yield capacitance and low short out force dissemination. We likewise propose six new half breed 1-piece full-viper (FA) circuits dependent on the novel full-swing XOR-XNOR or XOR/XNOR entryways. Every one of the proposed circuits has its own benefits as far as speed, power utilization, power-defer item (PDP), driving capacity, etc. To explore the exhibition of the proposed structures, broad HSPICE and Cadence Virtuoso recreations are performed. The reproduction results, in view of the 65-nm CMOS process innovation model, demonstrate that the proposed plans have unrivaled speed and force against other FA structures. Another transistor estimating strategy is exhibited to streamline the PDP of the circuits. In the proposed technique, the numerical calculation molecule swarm enhancement calculation is utilized to accomplish the ideal incentive for ideal PDP with fewer cycles. The proposed circuits are researched as far as varieties of the stockpile and limit voltages, yield capacitance, input commotion insusceptibility, and the size of transistors.

Gupta et al. [2], right now, propose a novel full viper configuration utilizing as not many as ten transistors for each piece. Contrasted and other low-door tally full snake structures utilizing pass transistor rationale, the proposed plan highlights lower working voltage, higher processing pace and lower vitality (power defer item) activity. The structure receives inverter cradled xor/xnor plans to reduce the limit voltage misfortune issue generally experienced in pass transistor rationale plan. This issue for the most part forestalls the full snake plan from working in low inventory voltage or falling straightforwardly without extra buffering. The proposed structure effectively inserts the buffering circuit in the full snake plan and the transistor tally is limited. The improved buffering enables the plan to work under lower supply voltage contrasted and existing works. It additionally improves the speed execution of the fell activity essentially while keeping up the exhibition edge in vitality utilization. For execution examination, both dc and performances of the proposed plan against different full snake structures are assessed by means of broad HSPICE reenactments. The recreation results, in light of TSMC 2P4M 0.35-mum procedure models, demonstrate that the proposed plan has the most reduced working V_{dd} and most elevated working recurrence among all structures utilizing ten transistors. It likewise includes the most reduced vitality utilization per expansion among these plans. Also, the exhibition edge of the proposed structure in both speed and vitality utilization turns out to be much progressively huge as the word length of the snake increments

Omid Akbari et al. [3], right now, propose four 4:2 blowers, which have the adaptability of exchanging between the specific and inexact working modes. In the estimated mode, these double quality blowers give higher speeds and lower power utilizations at the expense of lower exactness. Every one of these blowers has its own degree of exactness in the surmised mode just as various deferrals and force disseminations in the inexact and correct modes. Utilizing these blowers in the structures of equal multipliers gives configurable multipliers whose exactnesses (just as their forces and speeds) may change progressively during the runtime. The efficiencies of these blowers in a 32-piece Dadda multiplier are assessed in a 45-nm standard CMOS innovation by contrasting their parameters and those of the best in class surmised multipliers. By and large, 46% and 68% lower postponement and force utilization in the surmised mode. Additionally, the viability of these blowers is surveyed in some picture handling applications.

M. A. Valashani et al. [4], many existing XOR-XNOR cells experience the ill effects of nonfull-swing yields, high force utilization and low speed issues. Right now, new quick, full-swing and low-power XOR-XNOR cell, is displayed.

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Recreation brings about 90-nm CMOS innovation show that the proposed circuit has rail to rail yields Also, we have increased 11%-51%, 2%-19% and 18%-52% improvement in delay, power utilization and force defer item (PDP), individually. So as to do a correlation between the recently detailed XOR-XNOR cells and our proposed circuit, they are inserted in a 4-2 blower circuit and reproduction results demonstrate vitality effectiveness of our own in increasingly confused structures.

P. Bhattacharyya et al. [5], a 1-piece half and half full viper circuit configuration is displayed here utilizing changed XNOR door to improve the territory and speed execution. The plan is first executed for 1-piece cross breed full viper and afterward is reached out to the 32-piece snake. To upgrade the presentation of as far as territory, postponement and force the mix of CMOS, CPL, and transmission door rationale is utilized. For the exhibition investigation of the proposed structure; reenactment is completed in 90nm innovation with 1.2v inventory voltage. The reproduction result for the proposed usage of 1-piece half and half full snake shows the region (13 transistors) and postponement (5.1831nsec) decrease in contrast with the traditional cross breed 1-piece full viper.

Josmin Thomas et al. [6], vedic multiplier is a proficient framework for quicker outcome and streamlined circuit plan. Keeping up higher throughput in number juggling activities is imperative to accomplish the ideal execution in some constant applications. One of the key number-crunching tasks in such applications is to accomplish quicker increase. Vedic Mathematics is one of the quick and low force multiplier. In the present paper, zone, deferral and intensity of a Vedic multiplier is mulled over for the examination. These parameters are thought about for various adders, for example, Carry look forward adder(CLA), Carry select adder(CSLA), Ladner Fischer adder(LFA), Brent Kung adder(BKA), Kogge Stone adder(KSA) and blowers in Vedic multiplier. The quantity of adders can be limited by utilizing exceptional adders called blowers which can include increasingly number of bits one after another. This paper gives data of Urdhva Tiryakbhyam calculation of Vedic Mathematics which is used for increase to improve the speed and zone of multipliers. The force utilization of vedic multiplier relies upon the sort of the snake utilized so a correlation which has just done in RTL Cadence compiler is taken for the near examination here.

IV. EXCLUSIVE OR LOGIC GATES

The Exclusive OR logic gate is one of the logic gates that perform an exclusive or operation; i.e, a true output results if one, and only one, of the inputs to the gate is true. A false output results if both the inputs are false and both are true. XOR represents the inequality function, i.e., the output is high if the inputs are unalike otherwise the output is low. A way to think XOR is 'one or the other, but not both'. XOR can also be seen as addition modulo-2 and it can also called as arithmetic gate. Because of this, XOR gates are utilized to perform binary addition in computers. A basic digital adder is the half adder, which adds two bits, that comprises of an XOR gate for sum and an AND gate for carry. The algebraic expressions A.B1 +A1 .B and (A+B).(A 1 +B 1) either used to represent the XOR gate with inputs A and B and the operation of exclusive OR is summarized in the below truth table named as Table 1.1. XNOR is complementary to XOR. Applications of Exclusive OR logic gates are: The Exclusive OR circuit is the basic building block of various circuits mainly arithmetic circuits like adders, multipliers, compressors, comparators, pseudo random number generators, parity generators or checkers, code converters, correlation & sequence detectors, error detecting and error correcting codes, phase detector circuit in PLL and encryption processor. Hence it is used widely in many VLSI systems as a section of the critical path that determines the altogether performance of the system. So enhancing the performance of the XOR gate is important in reducing the propagation delay and power consumption.

Table 1: Two input Exclusive OR Truth Table

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

V. METHODOLOGY

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby

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enabling high speed performance of the processor which incorporates the same. The compressors used in the proposed architecture are explained as-

4:2 Compressor

A 4:2 compressor is capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X_1, X_2, X_3 and X_4 and 2 outputs Sum and Carry along with a Carry-in (C_{in}) and a Carry-out (C_{out}) as shown in figure 3.1. The input C_{in} is the output from the previous lower significant compressor.

The C_{out} is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders and half adders.

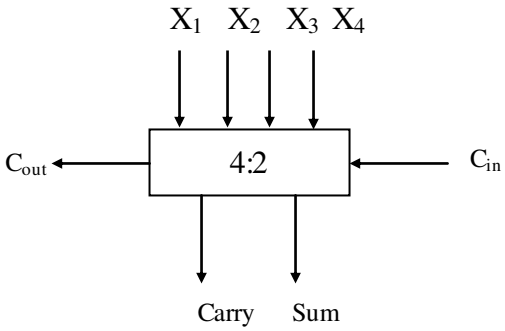

Fig. 1: Block Diagram of 4:2 Compressors

Similar to the 3-2 compressor the 4-2 compressor is governed by the basic equation

$$X_1 + X_2 + X_3 + X_4 + C_{in} = sum + 2*(Carry + C_{out}) \quad (1)$$

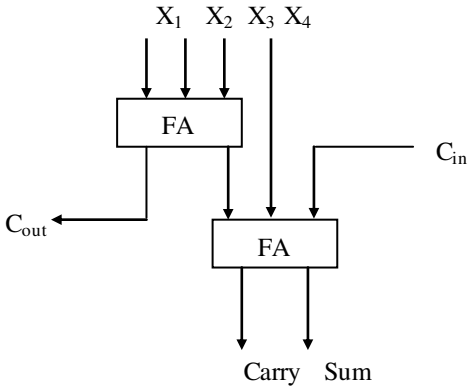

Fig. 2: Logic Diagram of 4:2 Compressors

The standard implementation of the 4-2 compressor is done using 2 Full Adder cells as shown in figure 2. When the individual full Adders are broken into their constituent XOR blocks, it can be observed that the overall delay is equal to 4*XOR.

Modified 4:2 Compressor

The block diagram in figure 3 shows the existing architecture for the implementation of the 4-2 compressor with a delay of 3*XOR. The equations governing the outputs in the existing architecture are shown below

$$Sum = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus C_{in}$$

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$$C_{out} = (X_1 \oplus X_2).X_3 + (X_1 \oplus X_2).X_1$$

$$C_{arry} = (X_1 \oplus X_2 \oplus X_3 \oplus X_4).C_{in} + (\overline{X_1 \oplus X_2 \oplus X_3 \oplus X_4}).X_4$$

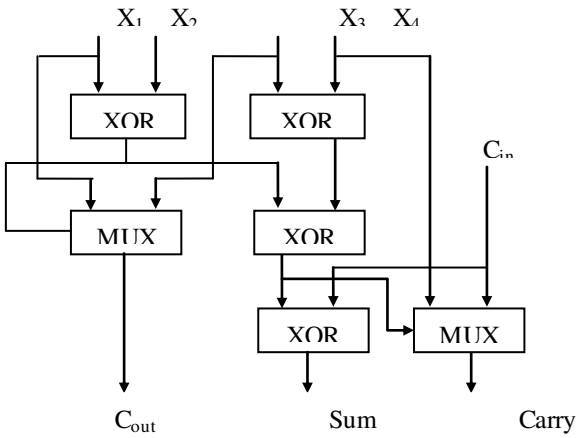


Fig. 3: Logical Diagram of Modified 4:2 Compressor

In show the delay and area all the modified 4:2 compressors. 4:2 compressors replacing some XOR blocks with multiplexer's results in a significant improvement in delay. Also the MUX block at the SUM output gets the select before the input arrive and thus the transistors are already switched by the time they arrive.

VI. CONCLUSION

Various two input and three input XOR and XNOR cells are reviewed from the past to the most recent published research work. (ii) Eight circuits of two new structures for two input XOR/XNOR circuits and compared with existing circuits with respect to parameters like propagation delay, power consumption and noise margin. (iii) Three circuits for three input differential XOR/XNOR circuits and compared with existing circuits with respect to all parameters. (iv) Four input differential XOR/XNOR circuit and compared with existing circuits with respect to all parameters. (v) General structure for multi input XOR/XNOR circuits, where that structure can be used for minimum of fan-in four to any number.

REFERENCES

[1] N. Hamed S. Timarchi "Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates" IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2018.
[2] Low Power Approximate Adders for General Computing Using Differential Transmission Gate" on 28.03.2018 National Conference on Innovations in Communication and Computing NCICC" 18 SNS College of Technology.
[3] Omid Akbari, Mehdi Kamal, Ali Afzali-Kusha, and Massoud Pedram, "Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 34, Issue 7, 2017.
[4] M. A. Valashani S. Mirzakuchaki "A novel fast low-power and high-performance XOR-XNOR cell" Proc. IEEE Int. Symp. Circuits Syst. (ISCAS) vol. 1 pp. 694-697 May 2016.
[5] P. Bhattacharyya et al. "Performance analysis of a low-power high speed hybrid 1-bit full adder circuit" IEEE Trans. Very Large Scale Integr. (VLSI) Syst. vol. 23 no. 10 pp. 2001-2008 Oct. 2015.
[6] Josmin Thomas, R. Pushpangadan and Jinesh, "Comparative Study of Performance Vedic Multiplier on The Basis of Adders Used", International Conference on Electrical and Computer Engineering, pp. 01-05, 2015 IEEE.
[7] Abdoreza Pishvaie, Ghassem Jaberipur and Ali Jahanian, "Compressor CMOS (4:2) recons pour less multiplication binary number", Can. Journal Electronics Computation Engineering, Vol. 36, No. 3, summer 2013.

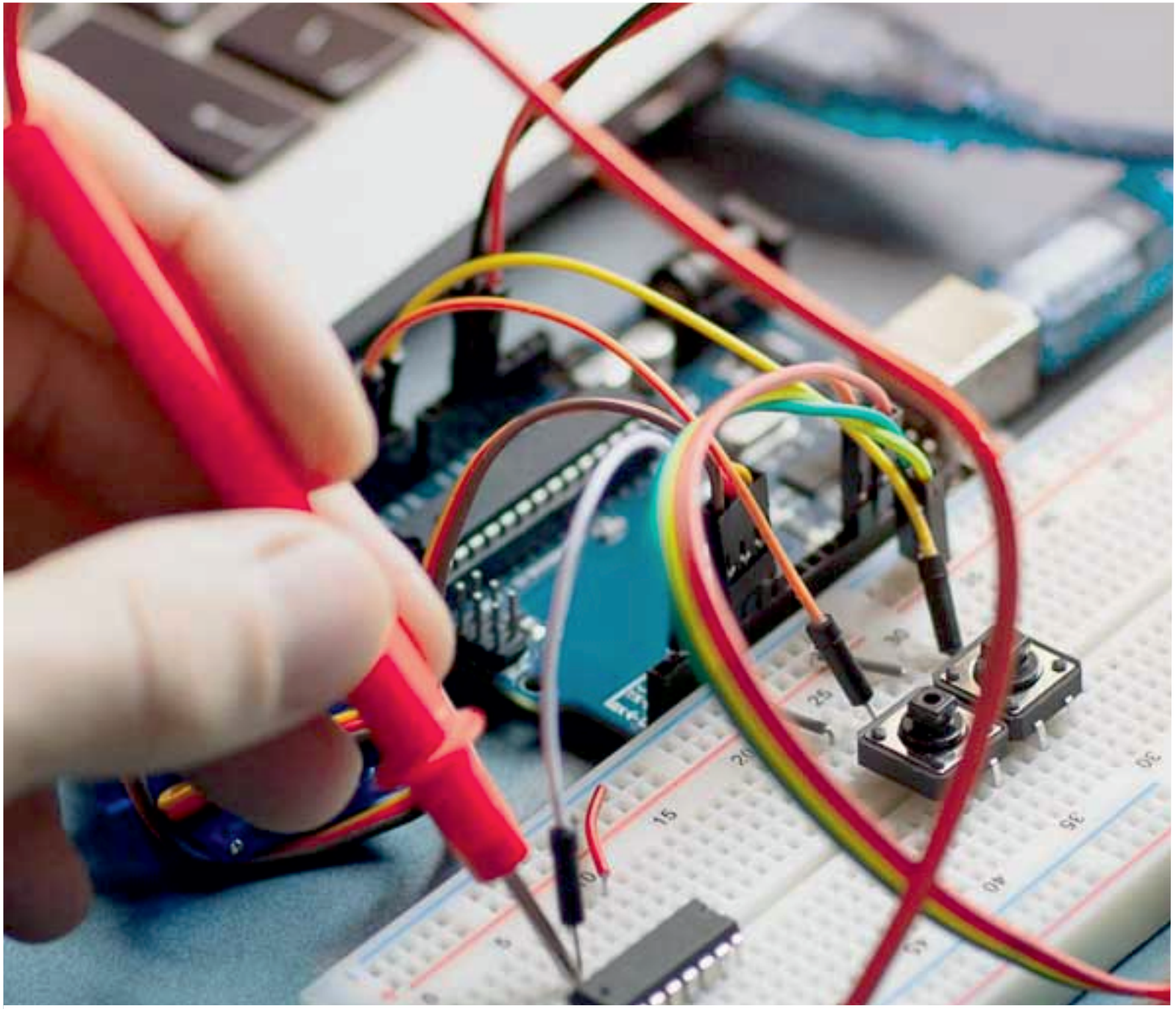
| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 3, March 2021||

DOI:10.15662/IJAREEIE.2021.1003023

[8] Pavan Kumar, Saiprasad Goud and A. Radhika, "FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter", International Conference on Digital Circuit and System, 2013 IEEE.

[9] Abdoreza Pishvaie Ghassem Jaberipur Ali Jahanian "Improved CMOS (4:2) compressor designs for parallel multipliers" Journal of Computers and Electrical Engineering pp. 1703-1716 Sep. 2012.



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