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Multilevel Inverter Based Basic Unit with Reduced Switches

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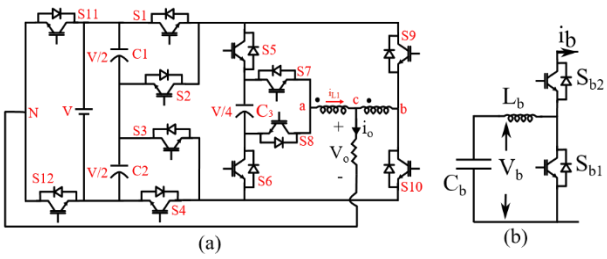
ABSTRACT: Multi Level Inverters (MLI) are commonly used in high voltage and high power applications due to their lower filtering requirements, smaller dv/dt transitions and better EMI/EMC performance. This paper presents a Single Phase Nine Level Inverter (SPNLI) using a coupled inductor. The proposed converter has low switch count, fewer capacitors and better reliability. Detailed operation of the proposed SPNLI and its control in standalone operation are discussed. An active energy buffer is also added to SPNLI to supply double line frequency component thereby reducing DC bus capacitance requirement. MATLAB SIMULINK based simulation results are presented to validate the proposed topology. Index Terms—Multi level, Inverter, Single phase, Coupled inductor, PV.

I.INTRODUCTION

Renewable energy sources play an important role in meeting the rising global power demand. Abundant availability, low cost and tiny carbon footprint make solar Photovoltaic (PV)s a promising power source for the future. Inverters are used to convert DC power from PVs to AC power suitable for AC loads or grid connection. The commonly used inverter for PV applications is the two level inverter. Two level inverters are simple in structure and easy to control. However, they have larger dv/dt transitions, higher filtering requirements and potentially greater EMI/EMC issues. To overcome these drawbacks, multilevel inverters(MLIs) are preferred for high voltage and high power applications. Classical MLI topologies such as Neutral Point Clamped(NPC), Flying capacitor(FC) Cascaded H-Bridge(CHB) converters and Modular Multilevel Converters(MMC) have been improved upon, resulting in hybrid MLIs. The hybrid five level inverter is proposed in has advantages such as fewer capacitors, fewer charging circuits but has higher switch count. A FC based, highly efficient 2-kW single phase seven level topology with energy buffer is presented in . This MLI uses fewer capacitors compared to conventional FC based MLI and achieves capacitors voltage balancing using phase displacement PWM(PDPWM). However, this topology requires more capacitors which decreases its reliability. In, a hybrid five level MLI based on active neutral point converter and flying capacitor H-bridge is proposed. Although producing greater RMS voltage, this MLI requires more number of switches. The FC and NPC based five level converter has equal distribution of losses among the switches but requires more number of diodes. In, a five level topology is proposed. This topology is able to operate robustly under variable modulation indices and load conditions. Level shifted PWM is used in this MLI for voltage balancing of the flying capacitor. A nine level MLI using a three-level FC inverter and cascaded H bridge modules with floating capacitors is proposed in. This MLI has specific advantage of operating at full load with reduced number of voltage levels upon failure of one of H-bridges. The main drawback of the topology is the requirement of more number of switches. In this paper, a single phase nine level inverter(SPNLI) is proposed



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II. CONVERTER AND TOPOLOGY

A block diagram of a multilevel inverter based single phase power conversion system is shown in Fig. 1. The proposed converter topology (Fig 2(a)) consists of 12 switches(S_1-S_{12}), a coupled inductor, two input side capacitors(C_1 and C_2) and one flying capacitor(C_3). The load is connected between node c (midpoint the two

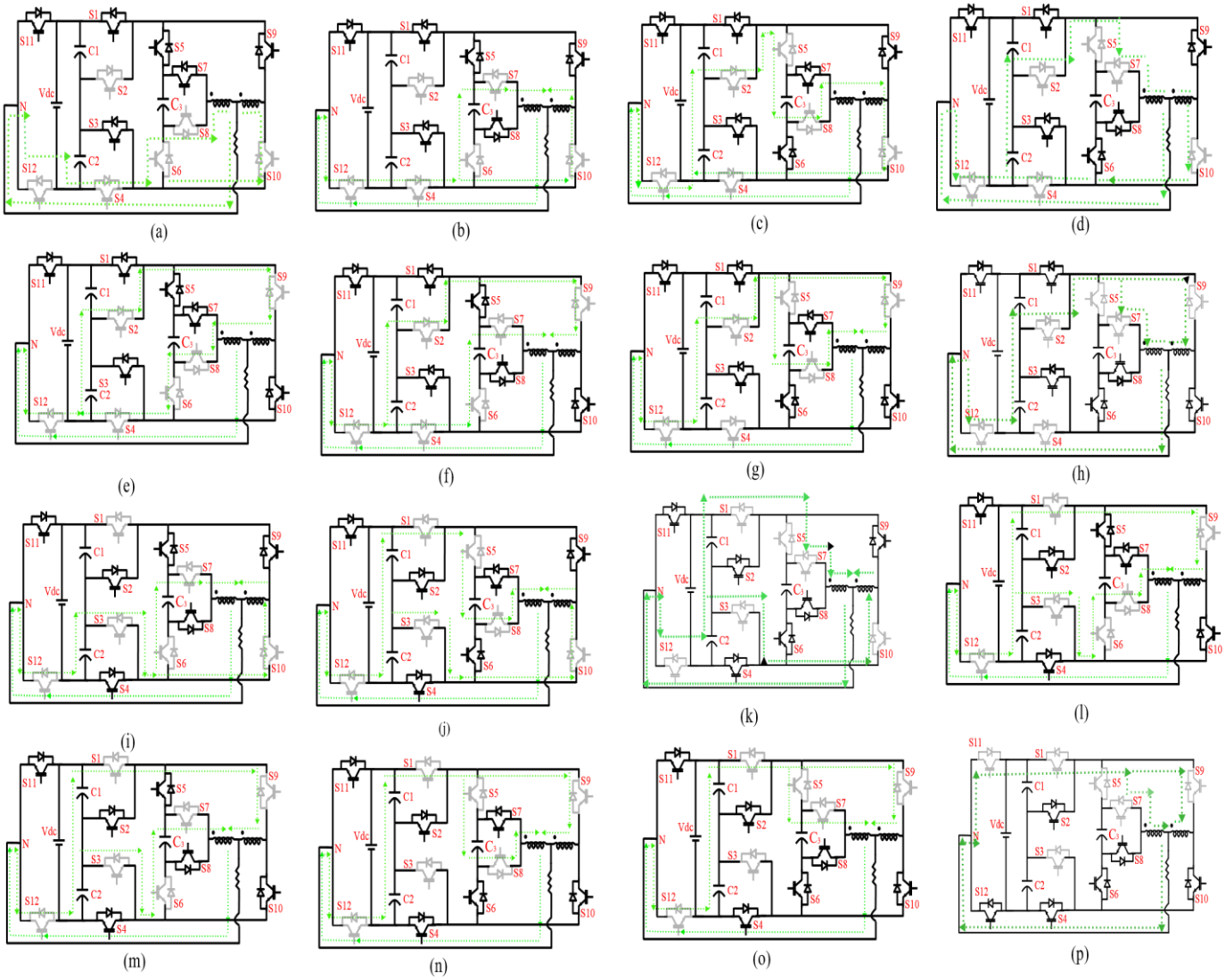

Fig. 3. Converter operational states (a) State 1, (b) State 2, (c) State 3, (d) State 4,(e) State 5, (f) State 6, (g) State 7, (h) State 8, (i) State 9, (j) State 10, (k) State 11, (l) State 12, (m) State 13, (n) State 14, (o) State 15,(p) State 16.

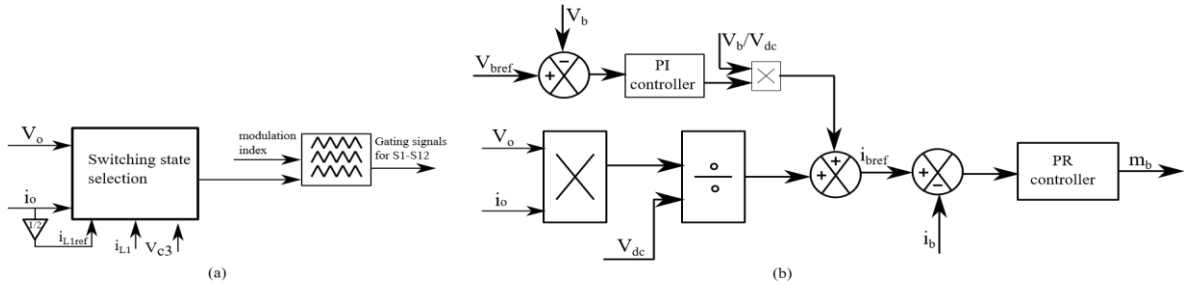

Fig. 4. Control block diagrams: (a) Gating pulses generation for S1-S12 and (b) Control diagram for buffer converter.

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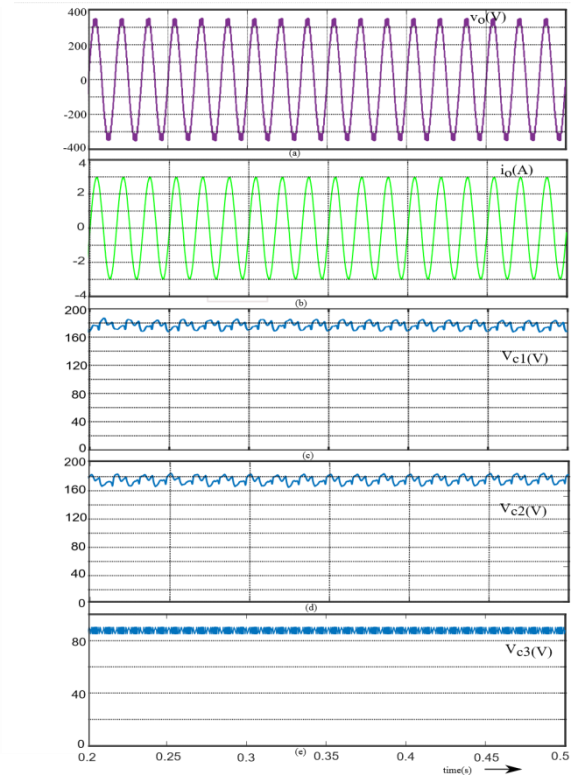
inductors) and node N. The topology can produce voltage inductor (node a) and 0V, ±V/2, ±V at other end (node levels 0V, ±V/4, ±V/2, ±V at one end of the coupled b). This results in nine possible voltage levels across the load: 0V, ±V/8, ±2V/8, ±3V/8, ±4V/8, ±5V/8, ±6V/8, ±7V/8, ±8V/8.

The SPNLI can have a number of possible switching states(SS). Only some of these switching states are needed, as listed in Table I. The switch pairs (S_1&S_2),
(S_3&S_4), (S_5&S_6), (S_7&S_8), (S_9&S_{10}) and (S_{11}&S_{12}) are complementary. The operation of SPNLI is symmetric in both positive and negative half cycles of the output voltage. Therefore, only switching states related to positive half cycle of output voltage are considered in the following explanation. Switching states(SS) are selected to balance the voltage of capacitor C_3based on the direction of inductor current(i_l) and present capacitor voltage.
There are 15 switching states (SS1 through SS15) for the positive half of the fundamental output voltage as shown in Fig. 3. Each has a symmetric complement for the negative half cycle (SS16 through SS30). Table I lists all these switching states along with the effect on the capacitor C_3 (C = Charging and D = Discharging) and the effective instantaneous output voltage V_{cN}. It can be seen that the output voltage can have 9 distinct values from 0 to V in steps of $V/8$.

Selection of switching states:
Based on the voltage level required, the converter checks for the direction of current(i_{L1}) and voltage balance requirement across capacitor (C_3), and selects a switching state as shown in Fig. 4(a). This selection of SS is applicable to all odd voltage levels. For the case of level ‘V/8’ and ‘i_{L1} >0’, SS3 is selected if ‘C_3’ requires charging, and SS2 otherwise. The selection of switching states are as shown in Table II.
For level ‘2V/8’, SS4 is used if ‘i_{L1ref} > i_{L1}’ otherwise SS5. Similarly for level ‘6V/8’, SS11 and SS12 are used to control depending on i_{L1} value.
Level shifted pulse width modulation technique is used for the proposed SPNLI to generate gating pulses. Levelshifted carrier waves are compared with a single modulating wave(m) to determine the instantaneous output voltage required. Eight carriers are used for the positive half cycle. In negative half cycle, eight more different carrier waves are used. Switching states are selected based on the voltage level required as explained above, which are then used to generate the required gate pulses.

III. RESULTS



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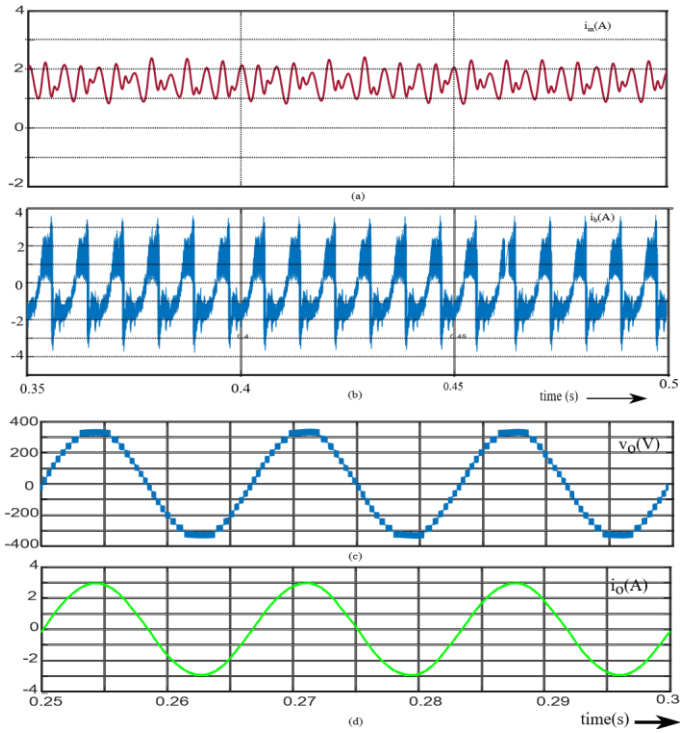

The proposed SPNLI is modeled in MATLAB SIMULINK. The topology is powered by a 350V source and a 240V, 500VA RL load is connected at the output. The coupled inductors (2mH each) have equal turns ratio with 0.95 coupling coefficient. 300μF capacitors are considered for C_1,C_2 and C_3. As wide band gap devices (like GaN) are intended to be used for this inverter, the carrier wave frequency is set at 100kHz.

Steady state results are presented in Figs. 5 and 6. Output voltage(V_o) and output current are shown in Fig. 5(a) and (b). Voltages(V_{c1}, V_{c2} and V_{c3}) across capacitors(C_1, C_2 and C_3) are shown in Fig. 5(c), (d) and (e). The capacitor voltages are seen to be well within limits and no additional balancing circuits are required. Zoomed view of output voltage(V_o) and output current(i_o) are presented in Fig. 6(c) and (d). All nine levels are observed in the output voltage(V_o). Buffer current(i_b) and source current(i_{in}) are shown in Fig. 6(a) and (b), showing the double frequency component.

IV. CONCLUSION

This paper presents a low switch count single-phase nine level inverter with a coupled inductor and low capacitance requirement. Capacitor voltages are balanced using switch state selection and no additional balancing circuitry is required. The output voltage has nine levels and has very low harmonic distortion. An energy buffer supplies the double frequency component of power and reduces DC capacitance requirement. The proposed topology was verified using simulation results. This topology, with its ripple free input current, is highly suitable for high power density PV applications.

REFERENCES

1. S. Augustine, M. K. Mishra, and N. Lakshminarasamma, “An improved droop control algorithm for load sharing and circulating current control for parallel dc-dc converters in standalone dc microgrid,” in *2014 Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD)*, July 2014, pp. 1–6.
2. T. Sreekanth, N. L. Narasamma, M. K. Mishra, and S. Augustine, “A single stage coupled inductor based high gain dc-ac buck-boost inverter for photovoltaic (pv) applications,” in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, June 2015, pp. 1–5.
3. Y. Chen, K. Chen, C. Wei, and J. Dong, “Three-level pwm for grid-connected pv inverter considering switching loss and common-mode voltage,” in *2018 7th International Symposium on Next Generation Electronics (ISNE)*, May 2018, pp. 1–4.
4. B. S. Naik, L. Umanand, K. Gopakumar, and B. S. Reddy,

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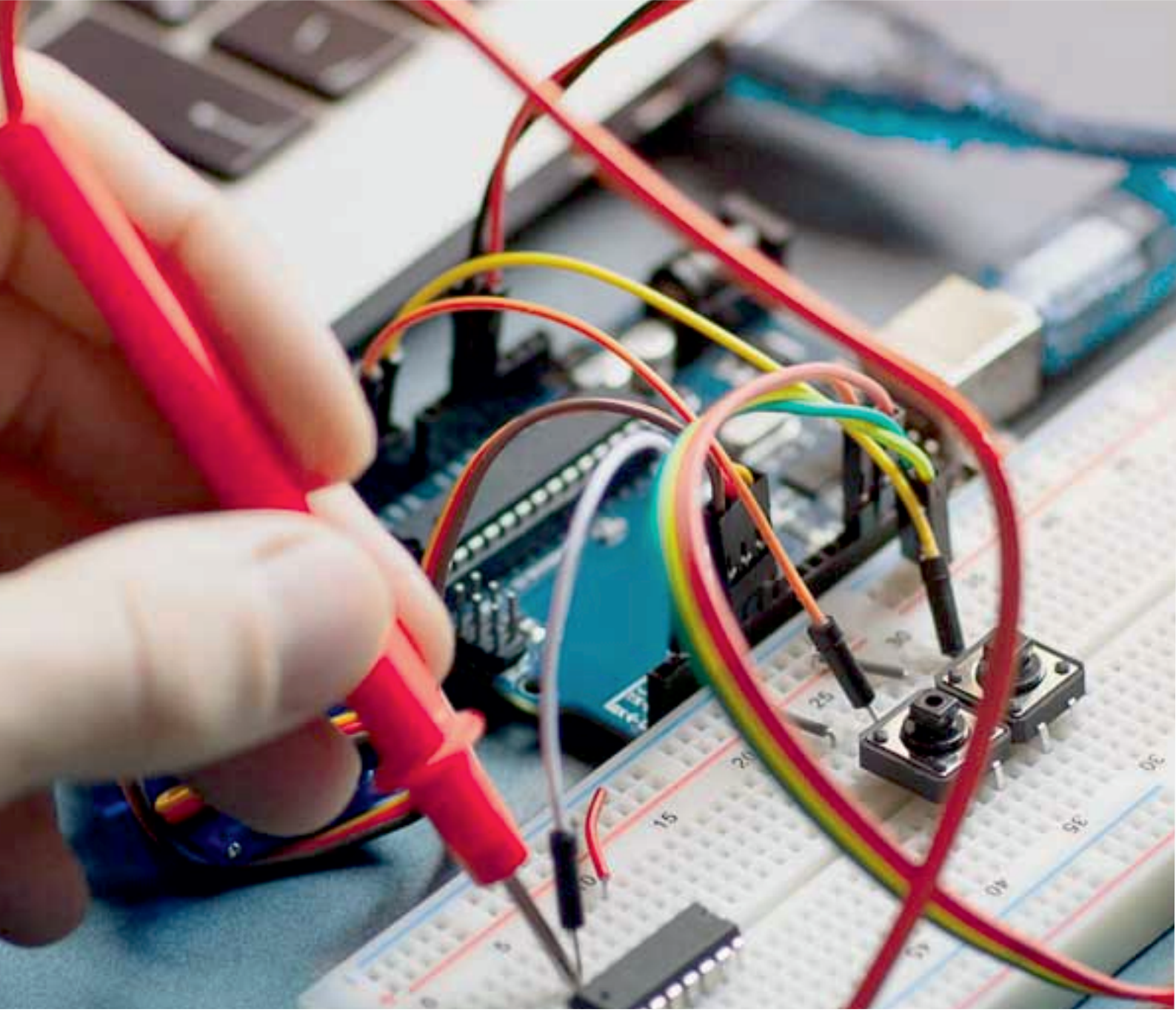
5. "A new two-phase five-level converter for three-phase isolated grid-tied systems with inherent capacitor balancing and reduced component count," *IEEE Journal of Emerging and Selected Topics in Power Electron.*, vol. 6, no. 3, pp. 1325–1335, Sept 2018.
6. S. Kolluri, P. Thummala, R. Sapkota, J. Xu, and S. K. Panda, "Spatial repetitive controller for minimizing circulating harmonic currents in modular multilevel converters for variable frequency applications," in *IEEE IECON 2016*, Oct 2016, pp. 3612–3617.
7. P. Chamarthi, J. Roy, and V. Agarwal, "A hybrid 9-level, 1grid connected multi-level inverter with low switch count and innovative voltage regulation techniques across auxiliary capacitor," *IEEE Trans. Power Electron.*, pp. 1–1, 2018.
8. J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug 2002.
9. J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. on Ind. Appli.*, vol. 32, no. 3, pp. 509–517, May 1996.
10. N. Sandeep and U. R. Yaragatti, "Operation and control of an improved hybrid nine-level inverter," *IEEE Trans. on Ind/ Appli.*, vol. 53, no. 6, pp. 5676–5686, Nov 2017.
11. Y. Lei, C. Barth, S. Qin, W. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8570–8581, Nov 2017.
12. R. Naderi and K. Smedley, "A new hybrid active neutral point clamped flying capacitor multilevel inverter," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 794–798.
13. T. T. Davis and A. Dey, "A hybrid multilevel inverter using single source neutral-point clamped front end and cascaded hbridge with flying capacitor based structures," in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2016, pp. 1–6.
14. P. R. Kumar, R. S. Kaarthik, K. Gopakumar, J. I. Leon, and L. G. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor h-bridges," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3471–3478, July 2015.



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