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Design of a 27-Level Asymmetrical Inverter Using Equal Phase and Half Height Method for Solar PV Applications

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ABSTRACT: With the increase in the demand of high quality electric power, multilevel inverter plays an important role to meet the demand. This work uses Solar PV system as an source with P&O MPPT algorithm. A novel 27 level asymmetric multilevel inverter is proposed which requires lesser Switches and DC sources to attain maximum output level. And a comparative study is carried out between fundamental frequency PWM methods precisely Equal Phase method and Half -Height(HH) method . Which has an advantage of lesser stress on the Switches. Leads to higher efficiency and lower Harmonic Distortion. The model is simulated with the help of MATLAB Simulink Software to demonstrate the performance of the same.

KEYWORDS: P&O MPPT algorithm, MLI, Half- Height(HH) method.

I. INTRODUCTION

Because of the fast depletion of fossil fuel reserves and their environmental impact, power generation from renewable energy resources is rapidly growing. Proper synchronisation is essential when several renewable power units are networked and integrated with the grid. To connect to the grid, an alternating current (AC) connection is necessary, which is obtained by attaching an inverter in the case of a solar PV system, as the generation is DC. A DC-DC Boost converter is designed with Perturb and Observe(P&O) MPPT algorithm. If the inverter output contains harmonics, the power pumped into the grid pollutes the power system. As a result, proper inverter design with minimal distortion is required.

The disadvantage of the typical kind is that as the number of levels increases, so do the components and associated devices. This problem is addressed by a subclass of inverters known as reduced component count (RCC) inverters, which use fewer components to provide the desired voltage levels at the output. This study examines one such RCC inverter and analysed its performance using fundamental frequency PWM techniques such as Half Height (HH PWM), and Equal-Phase PWM, (EP PWM). The performance is examined using MATLAB simulations, and a comparison of harmonic distortion is also shown.[1]-[10]

This paper aims to:To design a multilevel inverter with suitable parameter to achieve 27 level output voltage in asymmetrical configuration.To design a Boost converter with P&O algorithm for Solar PV input. To simulate a 27 level Multilevelinverter with fundamental frequency modulation techniques and to compare the voltage THD.To propose the multilevel inverter with best modulation technique by comparing the simulation results.

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Block- Diagram of PV System:

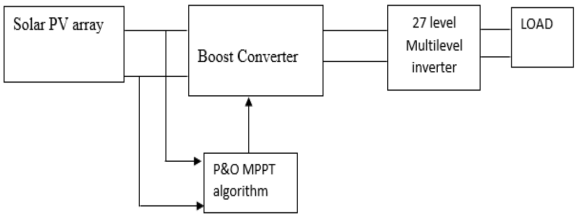

Fig. 1.1 Block Diagram of PV System

The Fig. 1.1 shows the outline of the project. Which describes as follows:

A SunPower SPR-315E-WHT-D module is used to generate a DC voltage. Which is unregulated hence DC -DC boost converter is used to regulate the DC voltage and P&O MPPT algorithm is used to track the Maximum Power point.

A 27 Level asymmetric multilevel inverter is designed using 8 switches , 4 diodes and 4 DC sources. Switching angle are calculated using equal phase method and Half height methodAnd a comparative study will be done between the two method to come with better method which employs lesser %THD.

II. SOLAR PV ARRAY AND BOOST CONVERTER

Solar photovoltaic (PV) panels capture the sun's energy and transform it into electricity using cells made of a semi-conductor substance. Silicon, a plentiful natural resource found in sand, is the most widely used semiconductor material. When light reaches the cell, a certain amount of energy is absorbed by the semiconductor material, throwing electrons, the negatively charged particles that serves as the basis of electricity, loose.

In the proposed system a solar array is used to generate a DC Voltage. For the multilevel inverter 4 DC supply is needed. A series parallel combination is made to generate a voltage in the ratio of 1:2:4:6.

Table2.1: Electrical Characteristics Data of SunPower SPR-315E-WHT-D PV module

Maximum Power- Pmax	315.072W
Voltage at Pmax – Vmp	54.7V
Current in Pmax – Imp	5.76A
Short- Circuit current – Isc	6.14A
Open-circuit voltage -Voc	64.6V
Number of Cells per Module	96

Since output voltage of PV module is not constant hence to regulate the DC voltage DC DC Boost converter is designed.

2.1 BOOSTCONVERTER

A boost converter (step-up converter) is a type of power converter that increases the voltage from its input (supply) to its output (load). It is a kind of switched-mode power supply (SMPS) that has at least two semiconductors (a diode and a transistor) and at least one energy storage element: a capacitor, inductor, or the two combined, to reduce output voltage ripple, as illustrated in Fig. 2.1

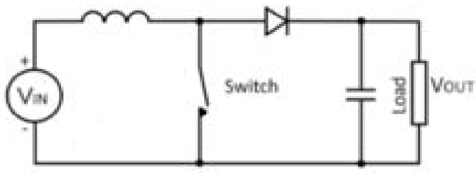

Fig. 2.1 Boost Converter

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A boost converter's core operation consists of two separate states:

MODE 1:

When the switch is closed as shown in Fig. 2.3, the battery charges the inductor and stores the energy. Inductor current rises (exponentially) during this mode; nevertheless, for simplicity, we assume that inductor charging and discharging are linear. Because the diode stops current flow, the load current, which is provided by the discharge of the capacitor, remains constant.

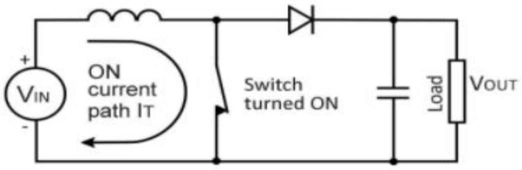

Fig. 2.2ON State of DC-DC Converter

MODE 2:
In mode 2, the switch is open, causing the diode to short circuit. The inductor's stored energy is released via opposing polarities, which charge the capacitor. Throughoutthe procedure, the load current stays constant.

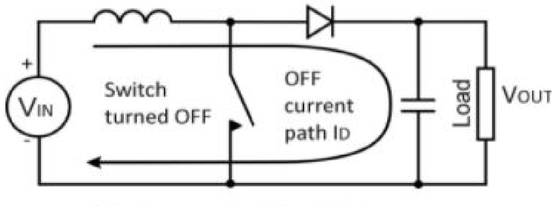

Fig. 2.3 OFF state of DC-DC Converter

Table 2.2: Boost converter Design values

Capacitor (C1)	12mF
Inductor (L1)	5mH
Input Capacitor(Cin)	100µF
Resistor(R)	10Ω

The simplest way is Perturb & Observe (P&O). It employ only one sensor, the voltage sensor, to sense the PV array voltage in this case, which reduces the cost of implementation and makes it easier to install. The temporal complexity of this approach is relatively low, but when it gets very near to the MPP, it does not stop there and continues to perturb in both directions.

According to the Perturb & Observe method, when the operating voltage of the PV panel is disturbed by a tiny increment, if the resultant change in power P is positive, we are moving away from the direction of MPP and the sign of perturbing is also moving away from the direction of MPP. If P is negative, we are deviating from the MPP direction, and the sign of the perturbation must be corrected.

Fig. 2.5 depicts the flowchart for the P&O algorithm. Implementation of this done using MATLAB Simulink software.

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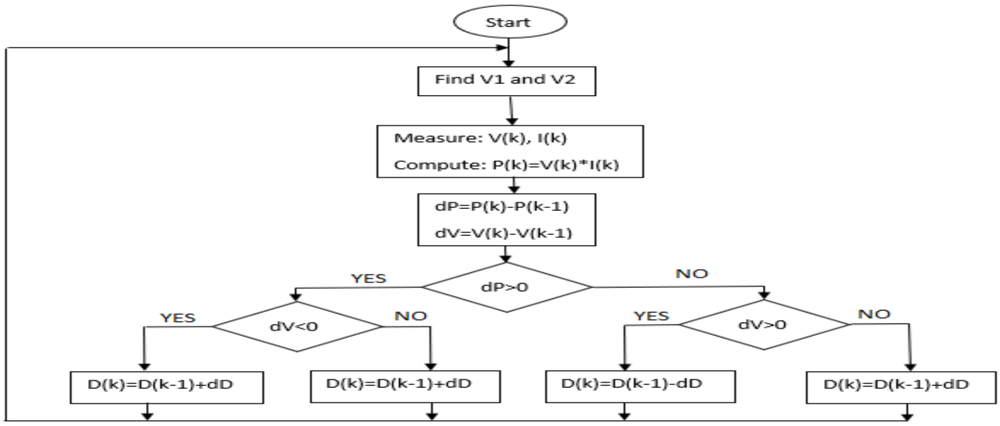

Fig. 2.5 Flowchart of the P&O algorithm.

III. PROPOSED 27 LEVEL ASYMMETRICAL MULTI LEVEL INVERTER:

The proposed new Hybridised H-bridge Asymmetrical Multilevel inverter topology with the arrangements of components containing 8 switches, 4 diodes and 4 DC sources with different magnitude are arranged as shown in the circuit diagram below. The switches used in this circuit can be either IGBT/MOSFET with antiparallel diode. The proposed topology uses unequal DC Voltage sources V1, V2, V3, V4 in the ratio of 1:2:4:6.

The switching states for the presented 27 level Asymmetrical MLI is shown in the table 1 for which the state condition ‘0’ entitled the non- conducting sate and ‘1’ entitled the conducting state. Which have 13 positive levels, 13 negative levels and 1 zero level.

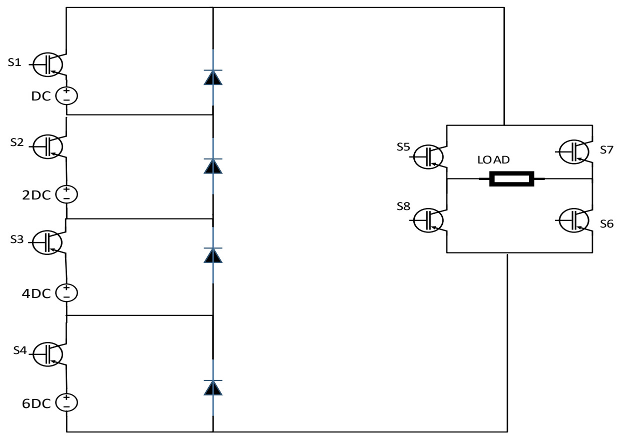

Fig. 3.1 Proposed 27 Level Asymmetrical MLI Circuit Diagram

3.1 MODULATION TECHNIQUE

Modulation technique for multilevel inverter are broadly divided into two categories, Fundamental switching frequency and High switching frequency PWM.

Equal Phase (EP) Switching Modulation Technique: In this technique the switching angles are distributed averagely over the full complete cycle ranging from 0-360 degrees. The equation to calculate the switching angles by Equal Phase (EP) method is given as;

$$\alpha_p = p * \frac{180}{N}$$

Where p=1,2,3,4......... 2N and N= number of output voltage levels.

Half Height (HH) Switching Modulation technique:

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In the half height switching modulation technique the total period from (0-360 degrees) of the output waveform are divided into four quadrants i.e.

- The period from 0 to 90 degree is referred as the main switching angle which is calculated as

$$\alpha_P = \sin^{-1}\left(\frac{2P-1}{N-1}\right)$$

Where p=1, 2, 3, 4................ $\left(\frac{N-1}{2}\right)$ and N-Number of output voltage levels

Table 3.1 Switching Table of proposed Inverter

SWITCHING STATE	S1	S2	S3	S4	S5	S6	S7	S8	OUTPUT VOLTAGE (V0)
1	1	0	0	0	1	1	0	0	1V
2	0	1	0	0	1	1	0	0	2V
3	1	1	0	0	1	1	0	0	3V
4	0	0	1	0	1	1	0	0	4V
5	1	0	1	0	1	1	0	0	5V
6	0	0	0	1	1	1	0	0	6V
7	1	0	0	1	1	1	0	0	7V
8	0	1	0	1	1	1	0	0	8V
9	1	1	0	1	1	1	0	0	9V
10	0	0	1	1	1	1	0	0	10V
11	1	0	1	1	1	1	0	0	11V
12	0	1	1	1	1	1	0	0	12V
13	1	1	1	1	1	1	0	0	13V
14	0	0	0	0	1	0	1	0	0V
15	1	0	0	0	0	0	1	1	-1V
16	0	1	0	0	0	0	1	1	-2V
17	1	1	0	0	0	0	1	1	-3V
18	0	0	1	0	0	0	1	1	-4V
19	1	0	1	0	0	0	1	1	-5V
20	0	0	0	1	0	0	1	1	-6V
21	1	0	0	1	0	0	1	1	-7V
22	0	1	0	1	0	0	1	1	-8V
23	1	1	0	1	0	0	1	1	-9V
24	0	0	1	1	0	0	1	1	-10V
25	1	0	1	1	0	0	1	1	-11V
26	0	1	1	1	0	0	1	1	-12V
27	1	1	1	1	0	0	1	1	-13V

- The period from 90 to 180 degree is referred as the second quadrant switching angle which is calculated as

$$\left(\frac{\alpha_N+1}{2}\right) = \pi - \alpha\left(\frac{N-1}{2}\right), \pi - \alpha\left(\frac{N-2}{2}\right), \pi - \alpha_1$$

The period from 180 to 270 degree is referred as the third quadrant switching angle

which is calculated as

$$\alpha_P = \pi + \alpha_1, \ldots., \pi + \left(\frac{\alpha_N - 1}{2}\right)$$

The period from 270 to 360 degree is referred as the final quadrant switching angle which is calculated as

$$\alpha\left(\frac{N-1}{2}\right) = 2\,\pi - \alpha\left(\frac{N-1}{2}\right), \pi - \alpha\left(\frac{N-2}{2}\right), 2\pi - \alpha_1$$

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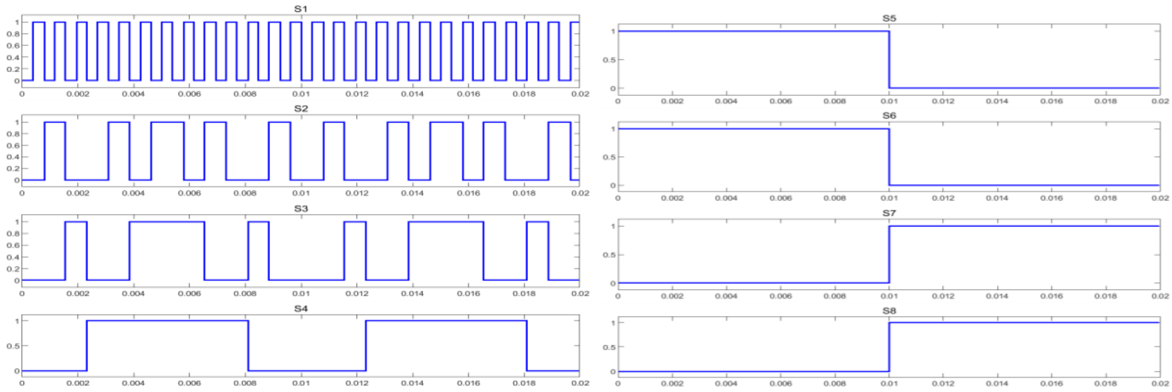

Fig. 3.2 One complete cycle switching pulse using equal phase method

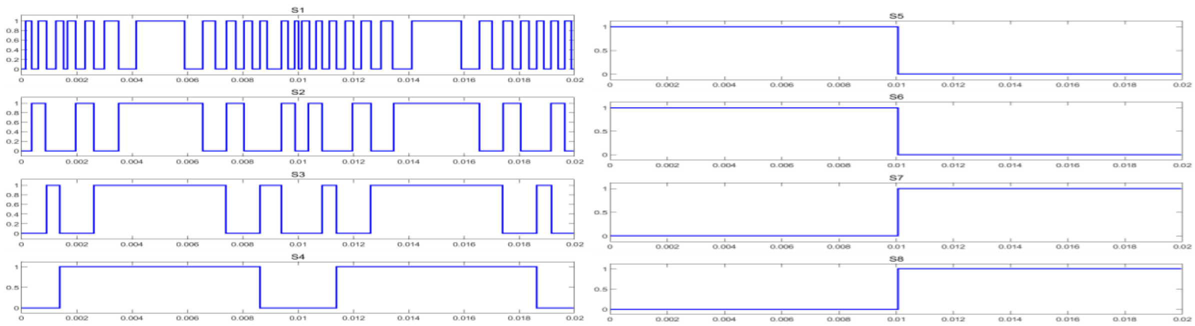

Fig. 3.3 One complete cycle switching pulse using Half Height method

IV. SIMULATION AND RESULT DISCUSSION

The proposed asymmetrical multilevel inverter is simulated for equal angle method and Half Height method in the MATLAB/Simulation environment. The results are analysed for resistive load. The load is resistive with a value of 100 ohms. The asymmetric DC input voltages are used in the ratio of 1:2:4:6. Fig 4.1 represents the simulation circuit of the proposed 27 level inverter.

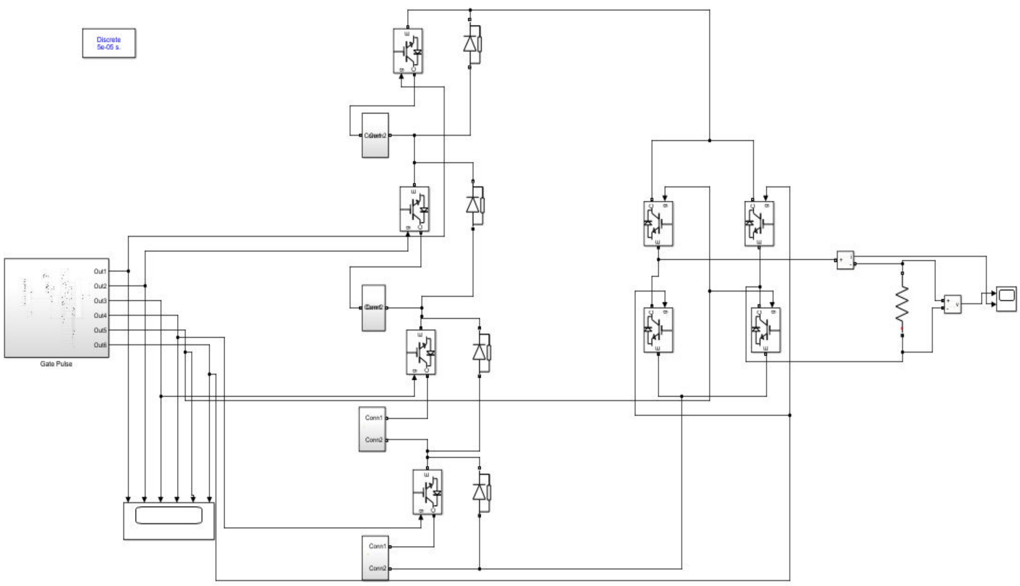

Fig 4.1 Simulation circuit of the proposed 27 level inverter with solar PV input

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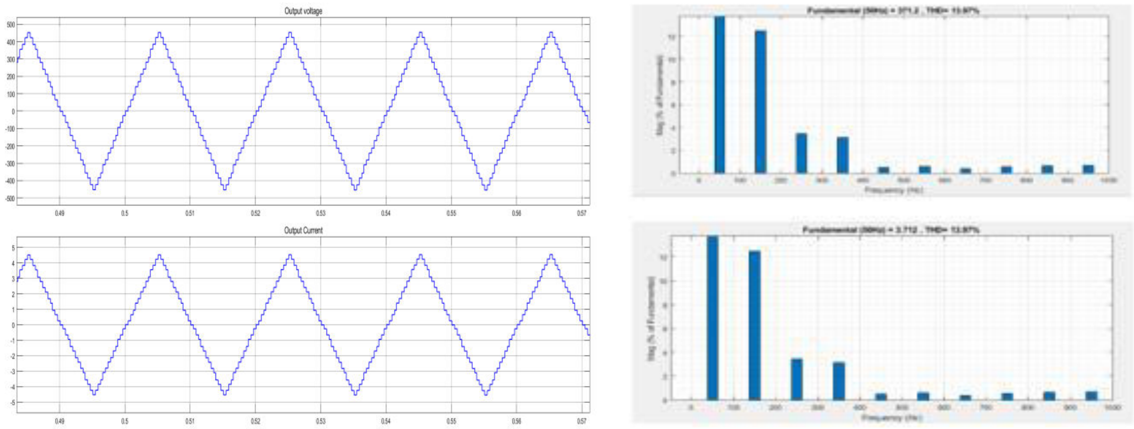

Fig.4.2 (a) output voltage waveform (b) output current waveform(c) Output voltage harmonic spectrum (d) Output current harmonic spectrum of the 27 level Type MLI for Equal Phase method

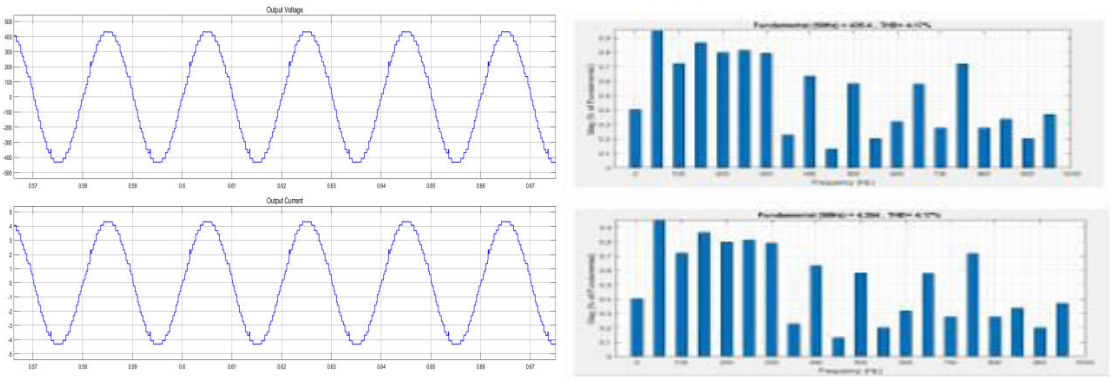

Fig. 4.3 (a) output voltage waveform (b) output current waveform (c) Output voltage harmonic spectrum (d) Output current harmonic spectrum of the 27 level Type MLI for Half-Height method

The Equal Phase switching angle calculation technique and the Half Height switching angle calculation techniques for the 27 level Asymmetrical Rhombus Type MLI and it can be summarized that the 27 level Asymmetrical Rhombus Type MLI using Half Height method offers very less value of THD, when compared with the 27 level Asymmetrical Rhombus Type MLI and Equal Phase method.

Table4.1 Comparison of results obtained from different methods for load of 100Ω

Inverter Topology	Switching technique	Load	Load Voltage THD%
27- level Asymmetric Inverter	Equal Phase method	100 Ω	13.97
	Half Height method	100 Ω	4.17

V. CONCLUSION AND FUTURE SCOPE:

In the proposed work, a solar PV system serves as a renewable energy source, and a boost converter is used to manage the DC voltage. This is assigned to a 27-level asymmetrical MLI. The results of two modulation techniques, Equal Phase and Half Height, are compared. The equal phase approach produces 13.97 % total harmonic distortion, whereas the half height

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method produces 4.17 % total harmonic distortion, and the AC output voltage waveform closely mimics the sine waveform. To summarise, the Half Height technique produces superior THD outcomes than the Equal Phase method.

For future investigations, this project may be extended to any higher levels by increasing the number of DC input voltage sources or modifying the ratios of DC input voltage values.

REFERENCES

[1]. L. Sabari Nathan, S. Karthik, S. Ravi Krishna, “The 27-Level Multilevel Inverter for Solar PV Applications”, 5th India International Conference on Power Electronics (IICPE), IEEE 2012.

[2]. A. A. KhodadoostArani, H. R. Zaferani, M. J. Sanjari, G. B. Gharehpetian, “Using Genetic Algorithm and Simulated Annealing for 27-level PV Inverter THD Minimization”, 2014 Smart Grid Conference (SGC), IEEE 2014.

[3]. Anjali Krishna R,L. Padma Suresh, “A Brief Review on Multi Level Inverter Topologies”, International Conference on Circuit, Power and Computing Technologies (ICCPCT), IEEE 2016.

[4]. J. Rodriguez, Jih - Sheng Lai, Fang Zheng Peng, “Multilevel Inverters: A Survey of Topologies, Controls, and Applications”, IEEE Transactions on Industrial Electronics, 2002.

[5]. Nageswara Rao. Jalakanuru, MeseretYenesewKiber, “Switching Angle Calculation By EP, HEP, HH And FF Methods For Modified 11-Level Cascade H-Bridge Multilevel Inverter”, International Journal of Engineering Science Invention ISSN, IJESI 2017, Volume 6 Issue 12, PP. 69-75.

[6]. Md. Tariqul Islam, Md. Shahidul Islam, Arnob Kumar Bairagi “A New Single Phase 21 Level Inverter Topology with Reduced Number of Switches and Sources for Renewable Energy Applications”, 4th International Conference on Electrical Engineering and Information & Communication Technology (iCEEiCT), IEEE 2018.

[7]. Mahdi Vijeh, Emad Samadaei, Mohammad Rezanejad, Hani Vahedi, Kamal Al-Haddad “Design and Implementation of a New Three Source Topology of Multilevel Inverters with Reduced Number of Switches”, IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, IEEE 2016.

[8]. Muhammad Fayyaz Kashif and Amir KhurrumRashid,”A Multilevel Inverter Topology With Reduced Number of Switches,” 978-1-4673- 8753-8/16/$31.00 ©2016IEEE

[9]. Mahdi Vijeh, Emad Samadaei, Mohammad Rezanejad, Hani Vahedi, Kamal Al-Haddad,” A New Asymmetrical Cascaded Multilevel Inverter with Reduced Number of Components,” in IEEE Conference 2018.

[10]. E. Samadaei, A. Sheikholeslami, S. A. Gholamian and J. Adabi, "A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters," in IEEE Transactions on Power Electronics, vol. 33, no. 2, pp. 987-996, Feb. 2018.