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Evaluation of Phase Disposition and Phase Shift PWM Techniques for Reduced Switch Multi-Level Inverter

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ABSTRACT:The main aim of this paper is that, in depth analysis of Phase Disposition(PD) and Phase Shift(PS) PWM control techniques performance with respect to 21-level reduced switch multi-level inverter. In this paper, a 21-level reduced switch multi-level inverter topology has been presented which uses 24 switches to generate 21-level output voltage. This reduced switch multi-level inverter is designed for domestic applications and simulated using MATLAB/SIMULINK. To control the switching states of multi-level inverter(MLI) phase disposition and phase shift PWM control techniques has been used. By comparative study between both the control techniques, performance evaluation has been done. Here, multi-level inverter performance parameters such as Total Harmonic Distortion, power losses, voltage regulation and efficiency are considered for performance evaluation of phase disposition and phase shiftPWM control techniques.

KEYWORDS: Multi-Level Inverter(MLI), Phase Disposition(PD), Phase Shift(PS), Total Harmonic Distortion(THD), Pulse Width Modulation (PWM), MATLAB/SIMULINK

I.INTRODUCTION

The Multi-Level Inverter(MLI) is a power electronics device which converts DC supply voltage into AC output voltage which is almost a sinusoidal in nature. Nowadays, Multi-Level Inverters are state of the art technology in power electronics field for high voltage, high power applications due to its advantages over conventional two level inverter. Some of the advantages of MLI's are, output voltage waveform will have reduced harmonic content,it can be used for high voltage applications without increasing the ratings of the switches, it can be operate at both fundamental and high switching frequencies, there are lower switchinglosses, better electromagneticcompatibility and higher power quality which eliminates filters and reduces size and cost of inverters.The multi-level inverters are used in applications such as wind turbine power plants, photovoltaic grid inverters, Motor drives, flexible AC transmission systems and in HVDC applications.

The effective operation of the multi-level inverter is depends on the topology involved in making the inverter and the control technique used for controlling switches. So, one should choose topology and control techniques carefully for making the multi-level inverters. In multilevel inverters, with the increase in number of voltage levels, the components required for manufacturing multilevel inverters will also increase which will in turn increases cost and size of the inverter. Hence, there are many researches are going on to reduce the power electronics components requirement in making multi-level inverters. In the same effort, in this paper a reduced switch inverter topology has been presented which use 24 switches to generate 21-level output voltage. An effective control technique will make switches to operate smoothly and reduces the harmonic content in the output waveform and thus improves the power quality.Some of the control techniques used in multi-level invertersareselective harmonicelimination(SHE) technique, space vector modulation(SVM) technique, Multi-Carrier PWM technique etc. In this paper, Multi-carrier PWM techniques has been chosen for the study and among Multi-Carrier PWM technique, there are different types such as phase disposition(PD),phase opposite disposition(POD), phase alternate opposite disposition (APOD), phase shift (PS) PWM techniques. From literature survey it is found that among Multi-Carrier PWM techniques, phase disposition(PD) and phase shift(PS) pulse width modulation (PWM) techniques are having better performance and they are simple in circuitry so that the implementation of control technique will be easier. Hence, both the control techniques have been chosen for further in depth analysis.

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II.PROPOSED METHODOLOGY AND DISCUSSION

Topology: The figure 2(a) shows the general diagram of the reduced switch multi-level inverter topology. The switches S11, S12 and DC source V1 makes the cell-1 and switches S21, S22 and DC source V2 makes cell-2. In order to generate 21-leveloutput voltage 10 such cells are required. These cells are connected in series to produce higher voltage levels. To alter the polarity of the output voltage, there is a need of one H-Bridge which is connected across the 10 cells as in figure 2(a). The switches Q1, Q2, Q3 and Q4 makes the H-Bridge. Therefore, there will be total 24 switches required to make 21-level inverter.

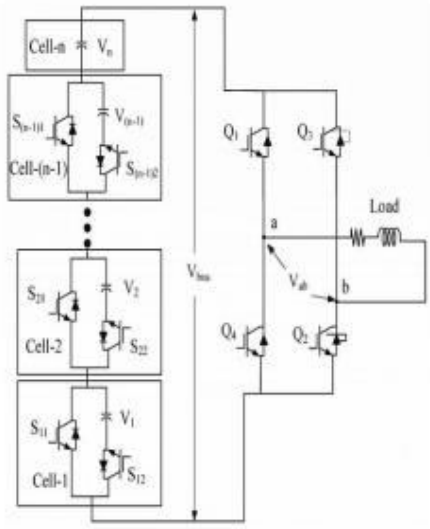

Figure 2(a) general diagram of reduced switch multi-level inverter topology

The table 2(a) shows the switching states at different voltage levels. At every instance, there will be 12 switches in conduction and other 12 switches will be in OFF state.

Sl No.	Conducting Switches	Output voltage levels
1	S11,S21,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	0
2	S12,S21,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+Vdc
3	S12,S21,S32,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-Vdc
4	S12,S22,S31,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+2Vdc
5	S12,S22,S31,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-2Vdc
6	S12,S22,S32,S41,S51,S61,S71, S81,S91,S101,Q1,Q2	+3Vdc
7	S12,S22,S32,S41,S51,S61,S71, S81,S91,S101,Q3,Q4	-3Vdc
8	S12,S22,S32,S42,S51,S61,S71, S81,S91,S101,Q1,Q2	+4Vdc
9	S12,S22,S32,S42,S51,S61,S71, S81,S91,S101,Q3,Q4	-4Vdc
10	S12,S22,S32,S42,S52,S61,S71, S81,S91,S101,Q1,Q2	+5Vdc
11	S12,S22,S32,S42,S52,S61,S71, S81,S91,S101,Q3,Q4	-5Vdc
12	S12,S22,S32,S42,S52,S62,S71, S81,S91,S101,Q1,Q2	+6Vdc
13	S12,S22,S32,S42,S52,S62,S71, S81,S91,S101,Q3,Q4	-6Vdc
14	S12,S22,S32,S42,S52,S62,S72, S81,S91,S101,Q1,Q2	+7Vdc
15	S12,S22,S32,S42,S52,S62,S72, S81,S91,S101,Q3,Q4	-7Vdc
16	S12,S22,S32,S42,S52,S62,S72, S82,S91,S101,Q1,Q2	+8Vdc
17	S12,S22,S32,S42,S52,S62,S72, S82,S91,S101,Q3,Q4	-8Vdc
18	S12,S22,S32,S42,S52,S62,S72, S82,S92,S101,Q1,Q2	+9Vdc
19	S12,S22,S32,S42,S52,S62,S72, S82,S92,S101,Q3,Q4	-9Vdc
20	S12,S22,S32,S42,S52,S62,S72, S82,S92,S102,Q1,Q2	+10Vdc
21	S12,S22,S32,S42,S52,S62,S72, S82,S92,S102,Q3,Q4	-10Vdc

Table 2(a) switching states and output voltages of 21-level reduced switch multi-level inverter.

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Control Techniques: Phase Disposition(PD) PWM control technique requires(n-1) carrier waveformsto generate gate pulses for n-level multi-level inverter. In this technique, all n-1 carriers are identical in magnitude and frequency but they are vertically shifted as shown in figure 2(b). All the carrier waveforms are arranged one over other and all the carrier waveforms must be in phase with each other.

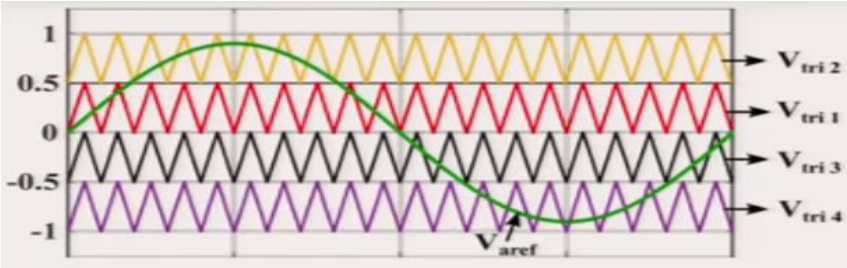

Figure 2(b) carrier waveform arrangement in PDPWM

Phase Shift(PS) PWM control technique also requires(n-1) carrier waveformsto generate gate pulses for n-level multi-level inverter.In this technique, all n-1 carriers are identical in magnitude and frequency but they are having phase delay of an angle Φwhich can be calculated as shown below

Φ=360/(n-1) where n is number of levelsi.e 2

Φ=360/(21-1)=18degree

On Simulink, the phase delay is given in terms of milliseconds and it can be calculated as follows, the carrier waveform frequency considered is 1000Hz and that means the carrier waveform's time period Tc=(1/1000)=1ms. Then phase delay in milliseconds=(18*1ms)/360=0.05ms. All the carrier waveforms are arranged such that all carriers should have phase delay of 0.05ms.

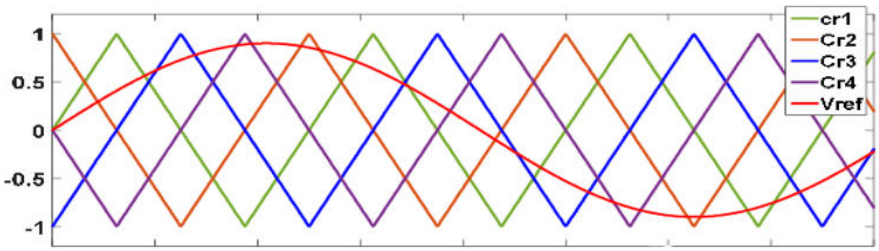

Figure 2(c) carrier waveform arrangement in PSPWM

The table 2(b) shows the logic for implementation of both PDPWM and PSPWM control techniques on SIMULINK for two cells and same can be extended for all others cells in the multi-level inverter. The logic implementation is same for both the control techniques but difference is that their carrier waveforms arrangement. By comparing magnitude of all carrier waveforms with the magnitude of sinusoidal reference waveform, gate pulses have been generated. In table 2(b), Vr refers to magnitude of sinusoidal reference waveform and Vc1,Vc2,Vc3 and Vc4 refers to the magnitude of four carrier waveforms and switches naming are followed as discussed in topology section previously.

Logic	
Cell-1	
If Vr> Vc1 or Vr< Vc3 then	S11 is ON and S12 is OFF
If Vr< Vc1 or Vr> Vc3 then	S12 is ON and S11 is OFF
Cell-2	
If Vr> Vc2 or Vr< Vc4 then	S21 is ON and S22 is OFF
If Vr< Vc2 or Vr> Vc4 then	S22 is ON and S21 is OFF

Table 2(b) Logic for implementation of both control techniques with reduced switch MLI

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Design Aspects: The power rating of the21-level reduced switch multi-level inverter is considered to be 3000watts and 230Volt output voltage. The design of various parameters of MLI are as follows,

$Po=V_{orms}*I_{Lrms,}$ where V_{orms} is RMS value of output voltage and$I_{Lrms}$is RMS value of the load current,

$Po=3000W$ $V_{orms}= 230V$ then $I_{Lrms}=Po/V_{orms}=3000/230=13.04A$ is the full load current,

Then load Resistance $R=V_{orms}/I_{Lrms}=230/13.04=17.64Ohm$.

The drain to source on state resistance of MOSFET switch is considered as 0.039ohm and DC voltage supply to the each cell is 33Volt to get 230volt at output. The reference sinusoidal waveform will have frequency of 50Hz and all triangular carrier waveforms will have frequency of 1000Hz. The amplitude modulation index for both the control techniques has been considered as one.

III.SIMULATION RESULTS

Simulation Results of 21-level reduced switch MLI with Phase Disposition(PD) PWM control technique

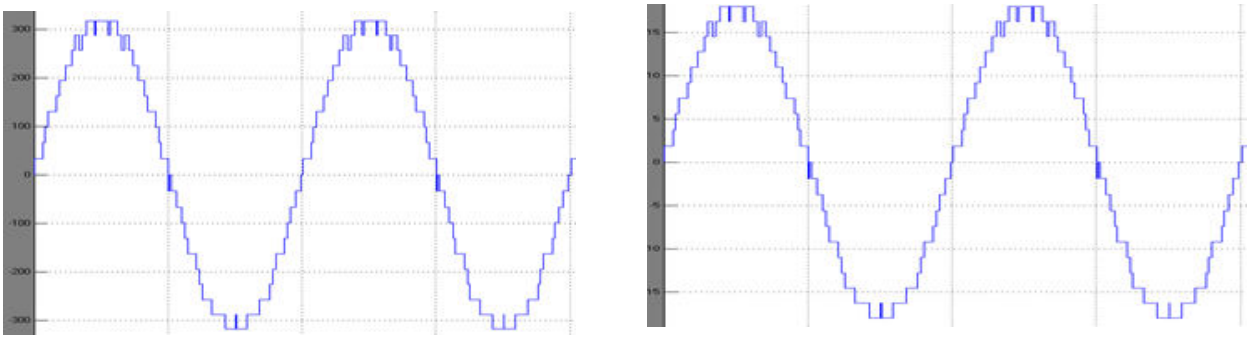

Figure 3(a) output voltage waveform and (b) Load current waveform

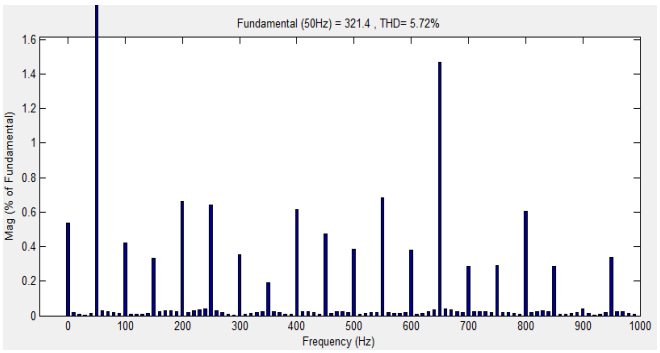

Figure 3(c) Total Harmonic Distortion(%)

Calculated Load Current $I_{o(calc)}$(A)	Load Resistance R(ohm)	RMS output voltage (Volt)	Measured load current (A)	THD (%)	Supply Power (W)	Output power (W)	Power Losses (W)	Efficiency (%)
13.04	17.64	227.7	12.91	5.72	2970	2930	40	98.65

Table 3(a) simulation results of 21-level reduced switch-MLI with PDPWM technique

With Phase Disposition PWM technique, 21-level reduced switch-MLI has no-load voltage of 234.2Volt and full load voltage of 227.7volt. The voltage regulation of the Multi-level Inverter is calculated as,

$$\text{Voltage Regulation} = ((V_{no\_load} - V_{full\_load})/V_{full\_load})*100$$
$$= ((234.2-227.7)/227.7)*100$$

= 2.85%.

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Simulation Results of 21-level reduced switch MLI with Phase Shift(PS) PWM control technique

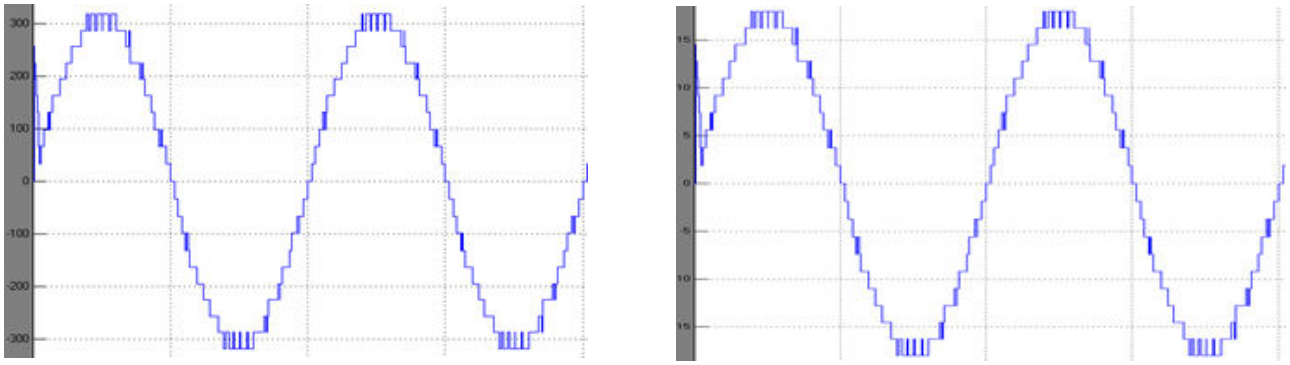

Figure 3(d) output voltage waveform and (e) Load current waveform

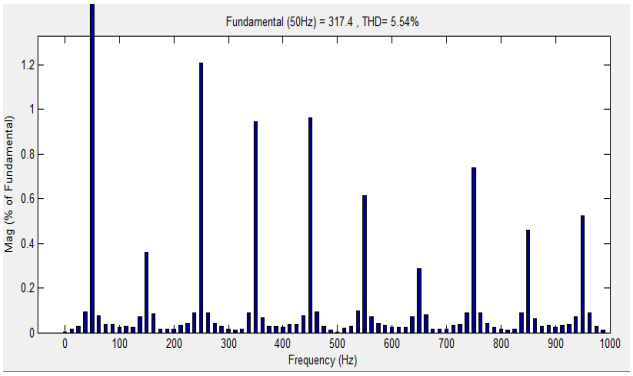

Figure 3(f) Total Harmonic Distortion(%)

Calculated Load Current $I_{o(calc)}$(A)	Load Resistance R(ohm)	RMS output voltage (Volt)	Measured load current (A)	THD (%)	Supply Power (W)	Output power (W)	Power Losses (W)	Efficiency (%)
13.04	17.64	224.9	12.75	5.54	2990	2860	130	95.65

Table 3(b) simulation results of 21-level reduced switch-MLI with PSPWM technique

With Phase Shift PWM technique, 21-level reduced switch-MLI has no load voltage of 231.3Volt and full load voltage of 224.9volt. The voltage regulation of the Multi-Level Inverter is found by formula $((V_{no_load} - V_{full_load})/V_{full_load})*100$and that is ((231.3-224.9)/224.9)*100 = 2.84%.

The table 3(c) shows the average currentIavg through each MOSFET switch, voltage drop Vdrop and conduction losses in each MOSFET switches of 21-level reduced switch multi-level inverter with both PDPWM and PSPWM control techniques.

Switches	Phase Disposition PWM			Phase Shift PWM		
	I_{avg} (Amp)	V_{drop} (Volt)	Conduction Losses(Watts)	I_{avg} (Amp)	V_{drop} (Volt)	Conduction Losses(Watts)
S11	11.62	0.453	5.266	9.566	0.373	3.568
S12	$5.6*10^{-6}$	$0.22*10^{-6}$	$1.2*10^{-12}$	5.399	0.211	1.14
S21	11.44	0.446	5.102	9.533	0.371	3.637
S22	0.1797	$7*10^{-3}$	$1.26*10^{-3}$	5.397	0.210	1.133

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S31	11.23	0.438	4.92	9.79	0.382	3.739
S32	0.382	0.015	$5.73*10^{-3}$	5.088	0.198	1.007
S41	10.99	0.429	4.715	9.702	0.378	3.667
S42	0.63	0.025	0.016	5.169	0.202	1.044
S51	10.4	0.405	4.212	9.854	0.384	3.784
S52	1.217	0.047	0.057	4.961	0.193	0.957
S61	9.57	0.373	3.57	9.88	0.385	3.804
S62	2.04	0.079	0.161	4.834	0.188	0.909
S71	8.86	0.345	3.056	9.823	0.383	3.762
S72	2.753	0.107	0.294	4.899	0.191	0.936
S81	7.969	0.311	2.478	9.783	0.381	3.727
S82	3.647	0.142	0.517	4.942	0.193	0.954
S91	6.221	0.242	1.505	9.767	0.381	3.721
S92	6.395	0.249	1.592	5.003	0.195	0.976
S101	3.357	0.131	0.440	9.74	0.379	3.691
S102	8.288	0.323	2.677	5.113	0.199	1.017
Q1	9.17	0.734	6.730	9.02	0.722	6.512
Q2	9.17	0.734	6.730	9.02	0.722	6.512
Q3	9.089	0.727	6.607	9.017	0.721	6.501
Q4	9.089	0.727	6.607	9.017	0.721	6.501
Total V_{drop} and Conduction Losses		7.043	67.260		8.089	72.479

Table 3(c)average current, voltage drop and conduction losses in all switches

The table 3(d)shows thecomparison between Phase Disposition PWM and Phase Shift PWMcontrol techniques with the various performance parameters of Multi-level inverter based on simulation results.

Parameters	Phase Disposition(PD) PWM	Phase Shift(PS) PWM
Total Harmonic Distortion	5.72%	5.54%
Total voltage drop across all switches	7.043Volt	8.089Volt
Voltage regulation of MLI	2.85%.	2.84%.
Total conduction Losses	67.260watt	72.479watt
Total Power Losses	40watt	130watt
Efficiency	98.65%	95.65

Table 3(d)Comparison between PDPWM and PSPWM

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IV.CONCLUSION

The simulation results of 21-level reduced switch multi-level inverter with both Phase Disposition and Phase Shift PWM control techniques shows that, the multi-level inverter with Phase Disposition PWM technique has better performance compared to Phase Shift PWM technique in all the various performanceparameters considered except Total Harmonic Distortion(THD) parameter. The IEEE standard 519-2014states that in a power system, at any common coupling point(PCC) the Total Harmonic Distortion must be below 8% if the operational voltage at PCC is below 1kv. For both the control techniques, THD is within the limits as specified in IEEE std 519-2014. So, one can choose Phase Disposition PWM technique over Phase Shift PWM control technique. The 21-level reduced switch multi-level inverter presented in this paper requires less power electronic components and has high efficiency. So, reduced switch multi-level inverter topology presented in this paper is preferable over other types of multi-level inverters.

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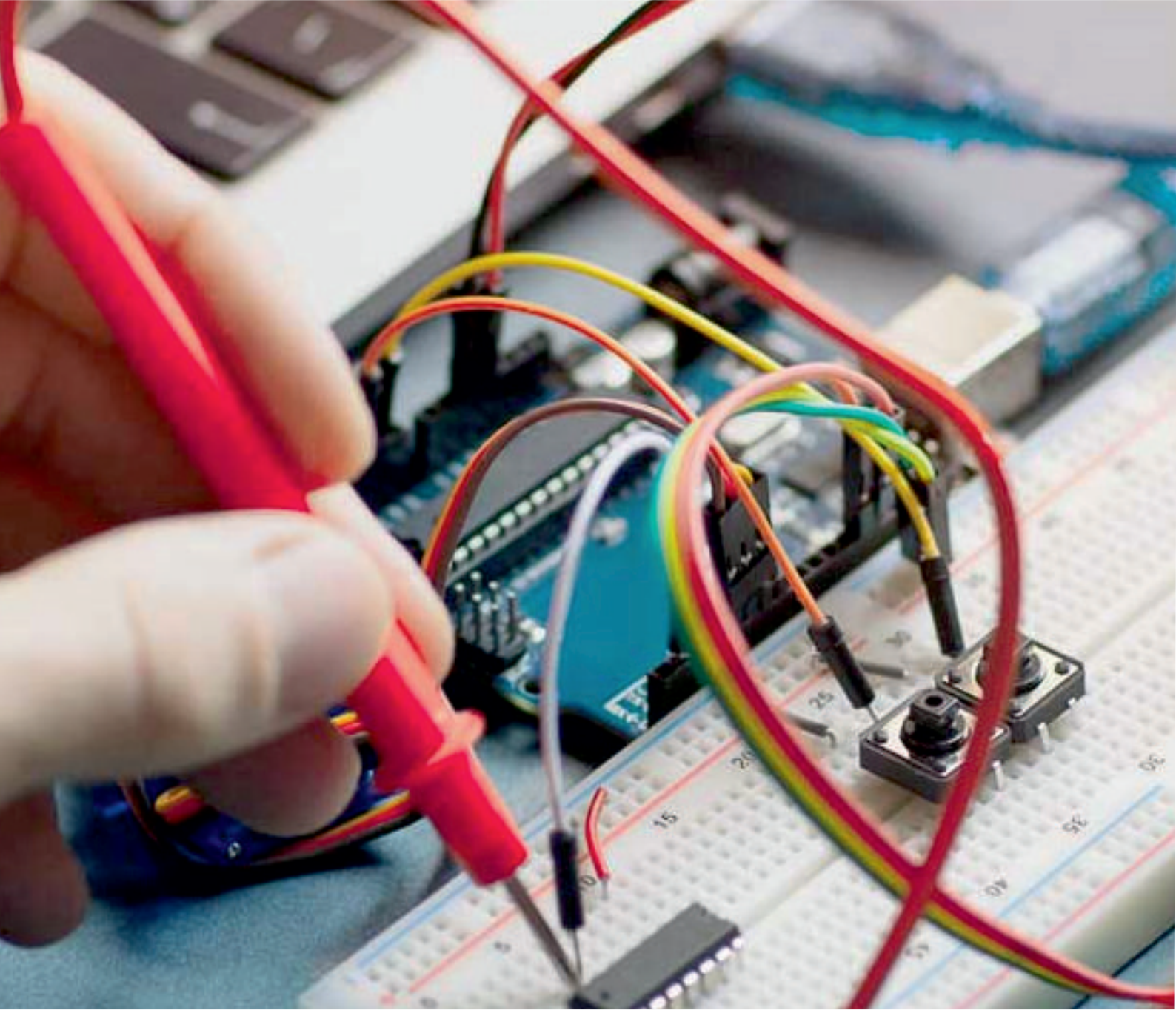

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