IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

Volume 10, Issue 4, April 2021

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.122

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

Hardware Implementation of Low Data Rate Burst Transceiver for Satcom application

Anantha Padmanabha[1], NNSSRK Prasad[2], Vinod L Kannur[3]

Scientist-F, CEMILAC, DRDO, Bangalore, Karnataka, India[1]

Scientist-H, Technology Director, Aeronautical Development Agency, Bangalore, Karnataka, India[2]

Senior Engineer, Alpha Design Technologies Limited, Bangalore, Karnataka, India[3]

ABSTRACT: The communication system on-board airborne military platform has seen inexorable growth in the recent past. The Radio functionality earlier limited to voice alone is now being extended to data, video, data link and networking operations in clear and secured modes. Accordingly, the existing hardware centric communication systems are being replaced with software intensive digital radio systems called Software-Defined Radio (SDR). The SDR deployed on combat platforms invariably consists of one Satellite Communication (Satcom) channel. A satcom involves an artificial satellite that relays and amplifies radio signals of different band of frequency via a transponder. It creates a communication medium between a transmitter and a receiver at different locations on Earth. Communications satellites are used in military applications, where optical fibre, mobile telephony and other modes of communications are impractical. It provides the war fighter, a single hop communication solution. Since the satellite has a limitation on power, the receiver must be capable of receiving very low power signals. This paper describes the design and digital implementation of complete Transmitter and Receiver chains. The intended application involves the low data rate satcom in Ultra High Frequency (UHF) band in the burst mode. The digital hardware used in transceiver architecture includes, Field Programmable Gate Array (FPGA), Digital Signal Processor (DSP) and General Purpose Processor (GPP).

KEYWORDS: SDR, Satcom, Burst, FPGA, DSP, UHF, GPP.

I.INTRODUCTION

The satcom system essentially consists of transmitter and receiver chain. In this paper we focus on the digital implementation of the transmitter and receiver for the Line of Sight (LoS) based satcom application. In the hardware selection, the first choice of hardware was the programmable device whose building blocks can be reconfigured. Field Programmable Gate Array (FPGA) belongs to this class. Since no single silicon device can meet the design requirements of efficient processing system, the need for DSP and GPP was also envisaged in the design. Accordingly, the hardware environment chosen for implementation of the proposed low data rate burst transceiver is Artix-7 FPGA evaluation board. The board provides embedded processing systems, Memory, Peripheral Component Interconnect (PCI) Express Interface, Ethernet Interface, General Purpose I/O and Universal Asynchronous Receive Transmit (UART) interface. In addition, RF platform is provided by FMCOMMS3-RFIC EVM development board, that has four functional partitions v.i.z receive path, transmit path, clocking and power supply. The data path is fully integrated into high performance highly integrated RF transceiver AD9364. Simulink platform is used for system modelling & HDL coder is used for HDL code generation.

In the proposed low data rate burst transceiver design, the Modem is implemented using programmable hardware. The novel approach in the current design is, the implementation of algorithms in FPGA for coarse carrier recovery, fine carrier recovery, timing recovery and phase ambiguity recovery for Quadrature Phase Shift Keying (QPSK) modulation scheme.

II.ARCHITECTURE OF LOW DATA RATE BURST TRANSCEIVER

The hardware architecture of burst transceiver consists of a GPP, DSP, FPGA and RFIC device. Each device is supported with flash memory, clocks and power supply (Not shown in the diagram). Each device has its own data and

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

control interfaces. The GPP is the AM335x series processor, which is connected with Ethernet and UART I/O interfaces.

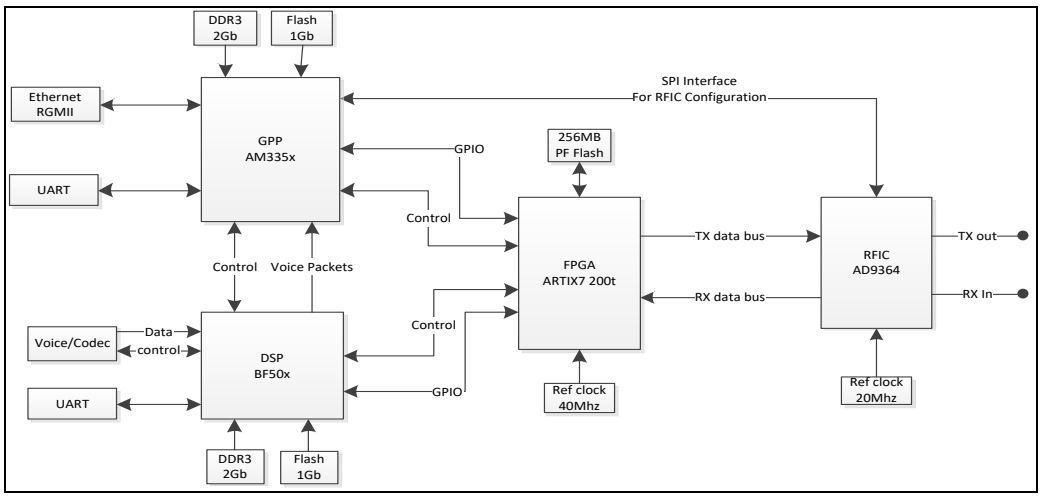


Fig-1: Architecture of Burst Transceiver.

The GPP is connected to DSP by Serial peripheral Interface (SPI) lines for control and General Purpose Input /Output (GPIO) lines for data interface. It is connected to FPGA by GPIO lines for data interface and SPI lines for control interface.GPP controls the configuration of RFIC device AD9364 through the SPI interface. DSP is the BF50x series processor which has Voice /Codec input interface and UART interface. It is connected to FPGA by GPIO lines for data interface and SPI lines for control interface.DSP controls the configuration of Codec device and receives data from Codec. The FPGA ARTIX 7 has 256 Mb platform flash, which is used to store the binary image. It has reference clock of 40MHz. The RFIC has 20MHz dedicated stable clock source. FPGA manages the Transmit and Receive data interface with the RFIC device. The Burst Modem data source is Ethernet and is configured for 1Gbps speed which transfers data, images and video. The voice is transferred by Codec to GPP via DSP. The selection of the source of the data is user configurable. The data packets from the Ethernet packets/Voice packets are stored in the FIFO memory for the rate transition. Data bits are modulated by QPSK modulator along with interpolation and pulse shaping. The filtered samples are sent to RFIC over Transmitter data bus with interleaved in-phase and Quadrature samples.

The RFIC converts the digital data into analog and then up converts it to UHF RF as configured by the SPI configuration from the GPP. The RF signal is sent to transmitter SMA connector, which is connected to Receiver section either by wired/wireless channel. The receiver signal from RFIC is down converted, digitized and sent over receiver data bus with interleaved In-phase and Quadrature samples to FPGA. The FPGA will recover the symbol from the received signal by carrier recovery, symbol recovery & demodulation process. Then frame synchronization will recover the packets from the received bits. Later, the frames are transmitted over the Ethernet to the user/Host end for verification of data frames for Bit Error Rate (BER) measurement. The implementation is divided into Transmitter and Receiver sections with MODEM processing in FPGA.

III. TRASMITTER SECTION

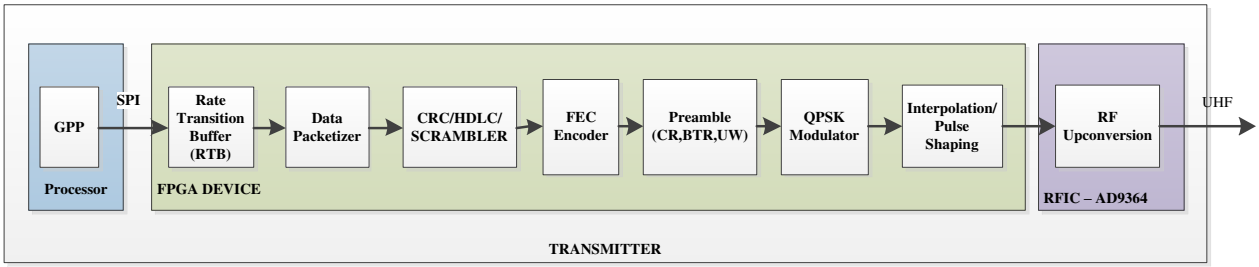


Fig-2: Transmitter Module for Burst Transceiver.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

The Transmitter section shown in Figure-2, indicates the data path through various stages for transmitting data from source to the channel (air medium). The data path consists of external source from user end which is Ethernet.
The Digital signal processing is carried out in the FPGA for Rate Transition, data packetization, Cyclic Redundancy Check (CRC), High-Level Data Link Control (HDLC), Scrambler of the packet, Forward Error Correction (FEC) and Preamble insertion involving Carrier Recovery (CR) and Bit Timing Recovery (BTR) and Unique Word (UW). Next, the packet is modulated by Quadrature Phase Shift Keying (QPSK) modulator to generate the symbols from the bits. The symbols are interpolated and pulse shaping is carried out with Root Raised Cosine (RRC) filter. The symbols are fed to the RFIC device which up-converts the baseband signal to UHF band. The details of the Transmitter section are explained below.

a) **The Data Source (GPP)**: The data generated by the user is transmitted to the processor (GPP) over the Ethernet, which is configured for 1Gbps speed. The data source used for the testing the application is generated by the third party application software that generates packets at constant rate from the user end (computer). The GPP is the master processor to form the user packets which can be either voice or data. The voice packets are received from the DSP processor and data packets are formed and encoded as per the application. The packets are switched between the voice/data in the GPP processor. The packets are subsequently sent to the FPGA for signal processing over the SPI interface with throughput up to 20Mbps.

b) **Rate Transition Buffer (RTB):** The SPI packets received from the GPP are stored in the RTB for Clock Domain Crossing (CDC). The change in the data rate takes place in RTB module. The detailed specifications of the MODEM are mentioned in the table-1.

Table-1: Modem Specifications

Sl.No	MODEM PARAMETERS	Value
1	Data rate	2400 bits/sec
2	Interpolation	8
3	Sample rate	19200 Ksps
4	E_b/N_o	0 to 12 dBm
5	Frequency Offset	+/- 4 KHz
6	CR/BTR/UW	32 Bytes
7	Flag	2 Bytes
8	Payload Length	124-512 Bytes

c) **Data Packetizer:** The data packets are divided into sub frames in this module. The sub frame length is the payload of the burst frame. The payload of the burst frame can vary from 124 bytes to 512 bytes; the burst length is decided by the application.

d) **CRC/HDLC/Scrambler**: The CRC is used to verify the integrity of the payload received at the receiver. While transmitting, the Frame Check Sequence (FCS) or CRC checksum of 16 bits is appended. At the receiver, the CRC checksum is calculated again on the frame and the checksum is compared with the received checksum. If the checksum matches, then there are no errors in the frame, else error is present in the frame. The CRC hardware implementation use Consultative Committee for International Telephony and Telegraphy (CCITT) -CRC Polynomial $X^{16} + X^{12} + X^5 + 1$.The truncated polynomial for the CRC16-CCITT is 0x1021H. The CRC calculation is realized with a shift register and XOR gates. Each bit of the data is shifted into the CRC shift register (Flip-Flops) after being XOR'ed with the CRC's Most Significant Bit (MSB). The data is treated by the CRC algorithm as a binary number. This number is divided by another binary number called the polynomial. The rest of the division is the CRC checksum which is appended to the transmitted message. The Frame is appended by 16 bits of CRC checksum at the end of the frame.The CRC will add 2 bytes of data at the end of the payload.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

The CRC appended to payload is subjected to High Level Data Link (HDLC) protocol. It's a bit oriented protocol. It uses synchronous transmission. All transmissions are in the form of frames and a single frame format is sufficient for all types of data control exchanges. The flag address and control fields are known as header.
The Frame Check Sum (FCS) and flag fields are referred to as trailer, which is a Cyclic Redundancy Check (CRC) checksum of the frame which is appended as shown in Figure-3.

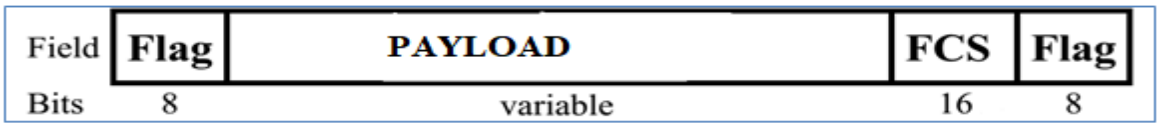


Fig-3: Hardware implementation of CRC16

The HDLC encoder processes the user supplied input bytes and generates the HDLC output bit stream. This consists of initial flags and a user-defined number of repeated "01111110" sequence and one or more frames containing the user-supplied data. Each time when five consecutive 1's are present the encoder inserts a 0. Flag is a unique bit sequence of 8 bit length present in the frame. The flag pattern is "01111110" present at the beginning and end of the frame.

The scrambler implemented here are self-synchronizing, which are given in the CCITT recommendation V.35. Scramblers and descramblers are used to prevent a long stream of either "1"s or "0"s in the data. The scrambler uses an additional Pseudo-Noise (PN) code selected with short runs of "1"s and "0"s which is combined with the data sequence. This is accomplished by performing a modulo-2 addition to the digital signal in the transmitter. The code used for the scrambler/descrambler contains no data and adds no cost and complexity. This technique further prevents drifts in Voltage Controlled oscillators (VCO) due to large change in DC values caused by no change in data states for long period of time. The polynomial used for scrambler is $1+X^{-1}+X^{-15}$ shown in Figure-4. The Initial state for the scrambler is 6959H.

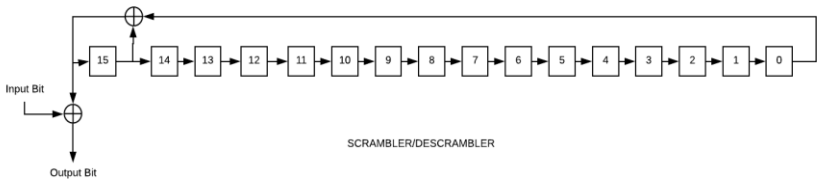


Fig-4: Hardware implementation of Scrambler/Descrambler

e) **FEC ENCODER:** The convolutional encoder is used as Forward Error Correction technique. It accepts a stream of message symbols and produces a sequence of code symbols. It uses a sliding window to calculate parity bits by combining various subsets of bits in the window. If a convolutional encoder produces 'R' parity bits per window and slides the window forward by one bit a time, its rate is 1/R, higher the value of R, the higher the resilience of bit errors. In our implementation we have used R=2, which generates 2 bits per 1 bit input.

f) **QPSK MODULATOR:** The burst packets received are converted to serial bits and modulated using QPSK modulation scheme. In QPSK, the binary input data are combined into two bits group, called dibits. Each dibit code generates one of the four possible output phases (+45°, +135°, -45°, and -135°).The symbol mapping uses the QPSK Modulator lookup table in order to map the two bit input value [0,1,2,3] onto the appropriate complex valued symbol [1+1i, -1+1i, 1-1i, -1-1i] respectively. Mapping (Grey) the symbols in this manner allows for a 2 bit value to be used to represent each symbol. The serial bits are modulated and In-phase & Quadrature symbols are generated. These symbols are having a step transition which generates infinite bandwidth. To avoid this, we will make the transition smooth by inserting more samples per symbol and filtering using Square Root Raised Cosine (SRRC) filter before transmitting to channel.The QPSK signal waveform S_n can thus be analytically

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

described as:

$$S_n(t) = \sqrt{\frac{2\,E_s}{T_s}}\cos\left(2\,\pi f_c t + (2n-1)\frac{\pi}{4}\right), n = 1,2,3,4$$

Where, the carrier frequency f_c is an integer multiple of the symbol rate $1/T_s$. E_s is Signal energy.

g) **Interpolation and Pulse shaping:** The Pulse Shaping component uses Finite Impulse response (FIR) Interpolation filter featuring an up-sampling factor of eight and a Root Raised Cosine (RRC) impulse response. To avoid bandwidth spreading over large span, the signal is passed through RRC filter. The output signal will have finite bandwidth after the filtering. The Pulse shaping technique is used to avoid very large bandwidth occupancy due to sudden transitions present in the symbols. The bandwidth spread is controlled by the Roll off factor. The transmitter bandwidth is calculated by knowing the roll-off factor of RRC.

Bandwidth = (Data rate * (1+ Roll of factor)/2).

h) **RF UP-Conversion:** The received baseband signals are up-converted to UHF band. The baseband to RF up-conversion process is done by highly integrated RF transceiver AD9364. The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. The device combines a RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers,

IV. RECEIVER SECTION

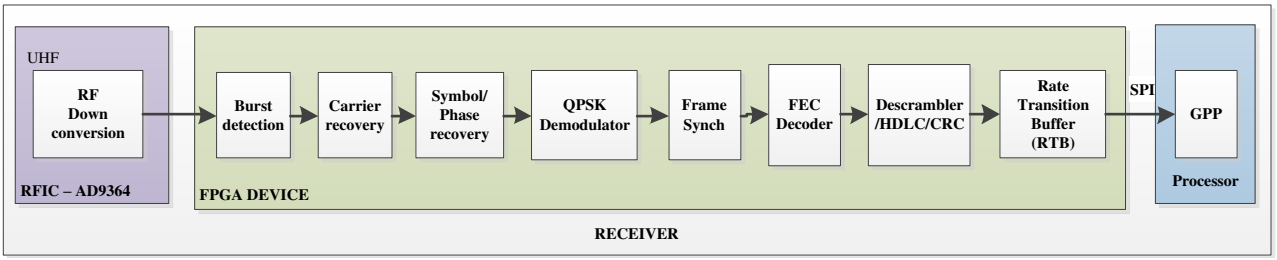


Fig-5: Receiver module for the burst transceiver.

a) **RF down conversion:** The incoming signal from an antenna is fed to RF Transceiver AD9364 which down-converts it from UHF band carrier signal to baseband signal. The receiver chain includes, Automatic Gain Control (AGC), DC offset correction, Quadrature correction and digital filtering thereby eliminating the need for these functions in the digital baseband. The down converted baseband signals are passed to FPGA for further processing.

b) **Burst Detection**: The received baseband signal is checked for Burst detection, which is implemented hare as a simple energy threshold mechanism, where the input signal's energy is calculated. When the detected value rises above a certain threshold value, the samples are captured and tagged as a burst frame start.

$$InputSignalPower = \frac{[absolute(RxSignal)^2]}{2}$$

c) **Carrier Recovery:** Carrier frequency offset occurs when the local oscillator of the receiver and does not synchronize with the carrier signal of the transmitted signal. Most receivers display a frequency offset compared to the transmitted frequency. In case of low data rate applications, the frequency offset is a critical parameter which needs to be found and compensated by the receiver. The magnitude of the frequency offset may vary for each transmitter and receivers. In some scenario, the frequency offset of the received signal may go beyond the capacity of the receiver carrier recovery limits. In such cases, we need to employ additional techniques to compensate the

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

offset present in the signal. The carrier recovery is carried out in two stages v.i.z coarse carrier recovery and fine carrier recovery.

Coarse Carrier Recovery*:* Fast Fourier Transform (FFT) based Carrier Frequency Offset (CFO) estimation is carried out to find the frequency offset. The signal is transformed to frequency domain to find frequency. To estimate the offset, FFT is calculated and index of the maximum amplitude across the frequency band is found and its index is used to find the peak frequency present in the input frame within the acquisition duration. The equation to find the Frequency offset using the FFT based estimation is given below.

$$\text{Freq Offset} = \text{Index of Max Amplitude} * \frac{Rx\ Sampling\ rate}{\text{FFT Length}}$$

Index of Max Amplitude is the index of FFT output, where the maximum amplitude peak has appeared. FFT Length is the FFT order at which the FFT is processed. Rx Sampling rate is the sampling rate of the input samples fed to FFT block. The estimated frequency offset value is converted to phase increment parameter for the configuration of Direct Digital Synthesizer (DDS). The phase increment value is used to generate the complex sinusoids and the receiver signal is multiplied. The phase increment value is calculated by the following equation.

$$\text{Phase Increment} = \frac{(\text{RequiredFreq}) * 2^{\text{phasewidth}}}{\text{FrequencyInput}}$$

Phase width is the value of DDS accumulator bits. Frequency input is the one, at which DDS is clocked. Required frequency is fed by estimation parameter.

Fine Carrier Recovery (FCR): The purpose of FCR module is to compensate for the Phase offset and Frequency offset, which remains even after the coarse carrier recovery. The FCR is based on Phase Lock Loop (PLL) algorithm which consists of PLL, Phase Error Detector (PED), Numerical Controlled Oscillator (NCO) and a multiplier. The PLL tracks the residual frequency offset and the phase offset in the input signal. A maximum likelihood Phase Error Detector (PED) generates the phase error. The tunable proportional-plus-integral Loop Filter is used to filter the error signal and then feeds to Direct Digital Synthesizers (DDS) block. The DDS generates the compensation frequency which nullifies the offset when we multiply it with the input signal.

d) **Symbol/Phase Recovery:** The aim of symbol recovery is to recover the optimal sampling moments for the data symbol detection. The powerful feed forward (FF) estimators for symbol timing recovery has been chosen for efficient acquisition since it is a burst modem. The zero crossing Timing Error Detector (TED) is used to detect the timing errors. The Symbol recovery generates one output sample for every two input samples.

In Phase recovery, the phase ambiguity present in the signal is recovered. The QPSK modulation scheme introduce 90° phase shift. To correct the ambiguity, the UW is inserted in preamble of every packet. The UW is tested for the phase changes and test results are compared with the ideal UW phase. With the difference in the ideal and received preamble phases, the phase shift is known. The conjugate value of phase shifted value is multiplied with the incoming frame, by that the ambiguity is compensated. Cross correlation function is implemented to recover the phase ambiguity. Cross correlation equation is shown below. Where x(n) in stored UW and y(n) is stream of bits from the receiver block.

$$R_{xy} = \sum_{n=0}^{N-1} x(n)y(n-k)$$

e) **QPSK Demodulation:** The symbols received after the phase recovery is used for symbol to bits conversion which is done using demodulator. The incoming Real and Imaginary channels are fed to this demodulator, where the magnitudes of the signals are compared with the Lookup table values. For QPSK the Lookup table values are [1 +

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

1i, -1 + 1i, 1 - 1i, -1 - 1i], If the quantized input matches the table values, then [0,1,2,3] binary outputs are generated respectively.

f) **Frame Synchronization:** The frame synchronization module will detect the unique word in the incoming data traffic by correlation. Once the correlation results of preamble are above the expected threshold value, then the data is considered as required data. The required data is then supported with a valid signal, by which packets are identified and the unwanted signal is removed from processing. The required payload data is sent to FEC decoder.

g) **FEC Decoder:** Viterbi decoder is one of the decoding algorithms used with convolution encoding. It has the advantage of fixed decoding time. It is well suited to hardware decoder implementation. But its computational requirements grow exponentially as a function of the constraint length. Therefore, its use is limited to constraint lengths of K = 9 or less. Convolutional coding with Viterbi decoding has been the predominant FEC technique used in space communications. Thus, it is employed in our satellite communication burst transceiver design.

h) **Descrambler/HDLC/CRC:** The scrambler and descrambler which are implemented here are self-synchronizing, given in the CCITT recommendation. The hardware for the scrambler and descrambler remains same. The hardware implementation uses 16 bit shift registers using flip-flops. The registers are initialized with the Hexadecimal initial value 0x6959. The shift register values are shifted with clock, according to the polynomial and the initial values XOR'ed, which generates the resulting bit which is further XOR'ed with the incoming frame bit results. The extracted frame data bytes are sent to the output. In HDLC, identification of the flag is done. It is a unique bit sequence of 8 bit length present in the frame. The flag pattern is 01111110 present at the beginning and end of the frame.

The correlator is used at the receiver to identify the flag in order to achieve frame synchronization. CRC is used to verify the integrity of the frame received. During transmission, the frame check sequence or CRC checksum of 16 bits is appended. At the receiver, the CRC checksum is calculated again on the frame and the checksum is compared with the received checksum. If the checksum matches, then there are no errors in the frame else error is present in the frame.

i) **Rate Transition Buffer (RTB):** The valid frames are stored in the buffer for sending it to tester device or UART. The Packet error rate is calculated at this stage to find the efficiency of the modem. The stored data is transmitted to GPP over SPI interface. The GPP will route the packet to the respective destination as per the configuration.

V. RESULTS AND DISCUSSIONS

The proposed design is implemented in the FPGA evaluation board AD9364. The implementation uses a fixed data source, which is modulated in FPGA and up-converted to UHF. The frequency offset is introduced to check the receiver performance. The signal with large frequency offset (+/-4 KHz) is fed to the receiver channel of AD9364 which is down-converted to baseband. It is further fed to FPGA for processing that includes burst detection, removal of frequency offset and recovery of data from symbols. The recovered data is applied to FEC decoder to detect and correct the errors.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

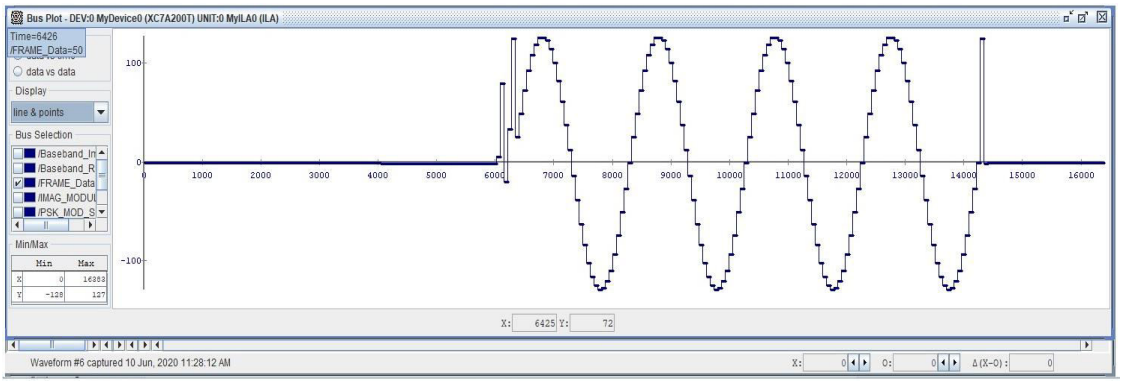


Fig-6: Transmitter Burst Frame captured in FPGA

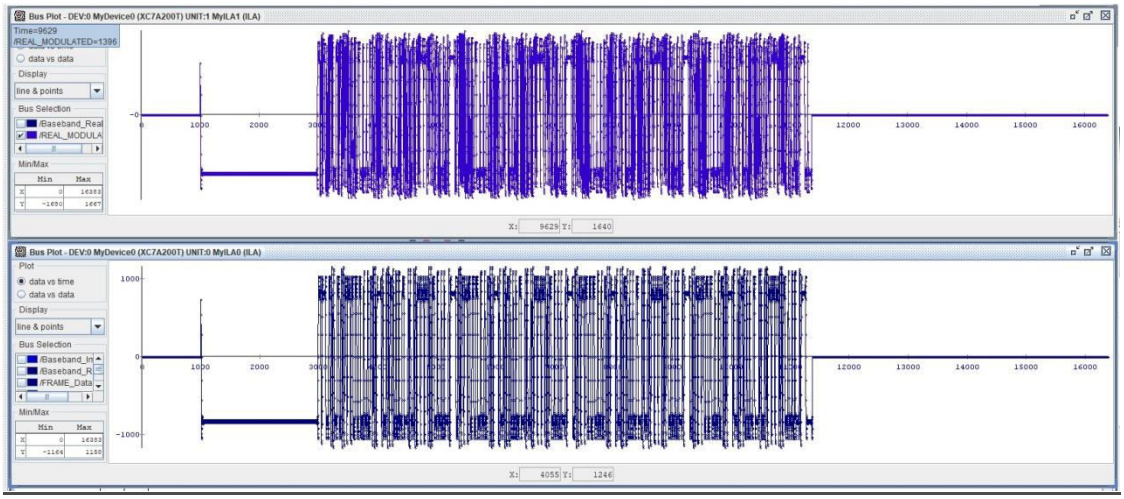


Fig-7**:** QPSK MODEM I, Q symbols of the Transmitter Burst packet in FPGA.

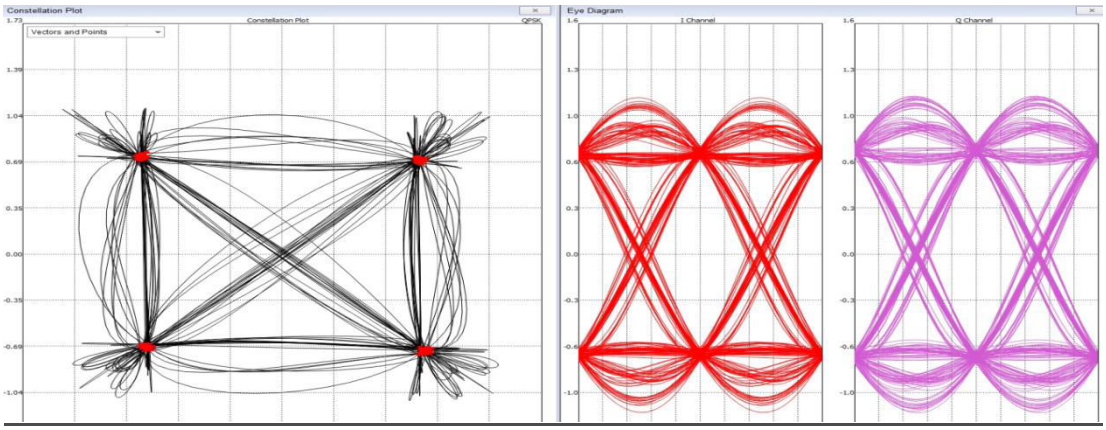


Fig-8**:** QPSK transmit signal Constellation, Eye diagram observed in spectrum analyser

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

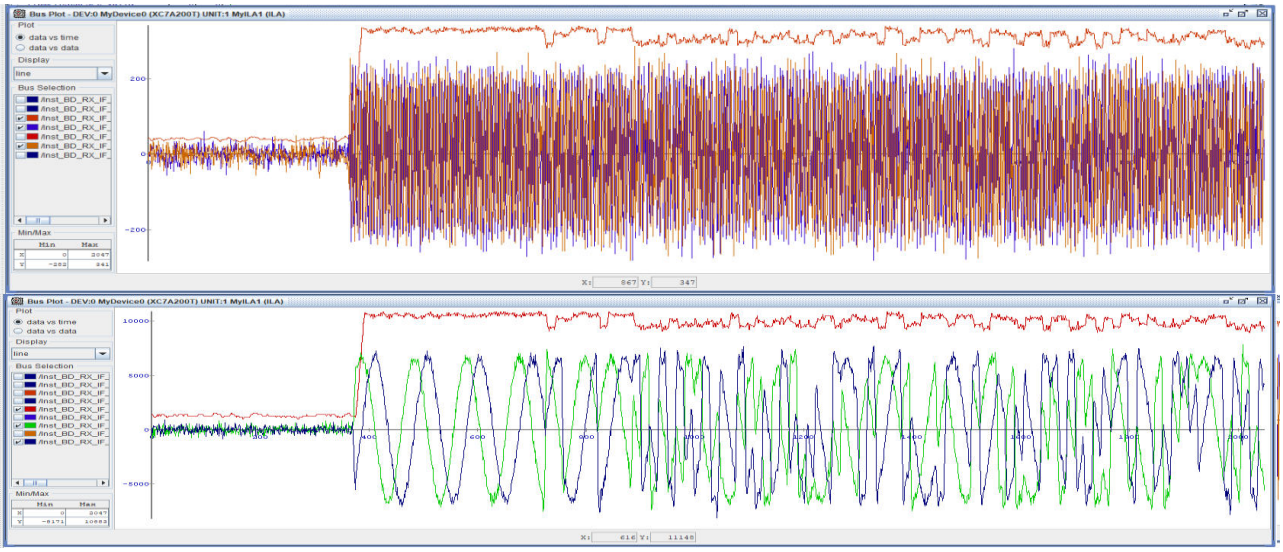


Fig-9: Row1- Receiver Burst detection of the single frame with large frequency offset, Row2- Received Signal after Coarse compensation for frequency offset, shows change in the frequency content. Captured in FPGA

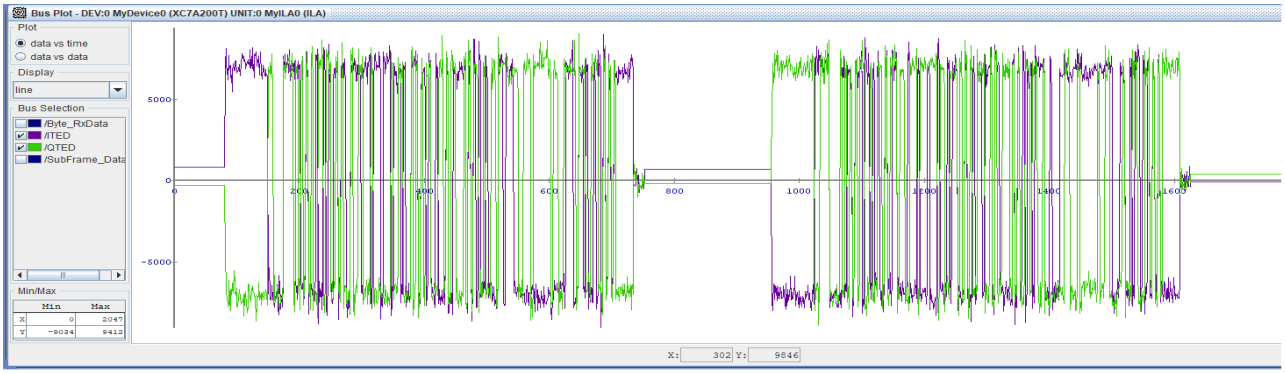


Fig-10: Received signal burst captured after Fine carrier recovery in FPGA.

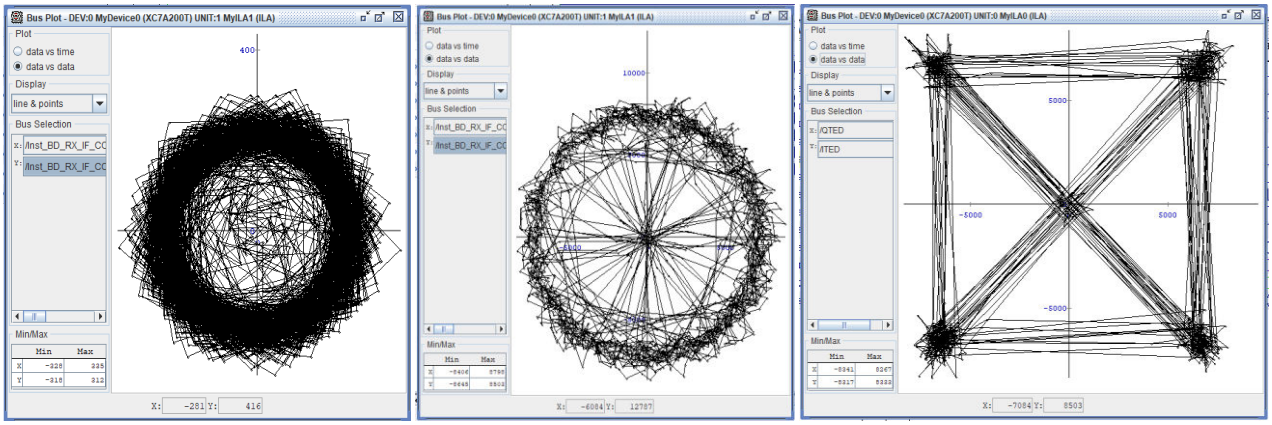


Fig-11**:** The Receiver (RX) QPSK constellation captured in FPGA (Left to Right), 1-RX signal with large Frequency offset, 2-RX signal constellation after coarse carrier recovery, 3- RX signal constellation after fine carrier recovery showing proper QPSK constellation.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

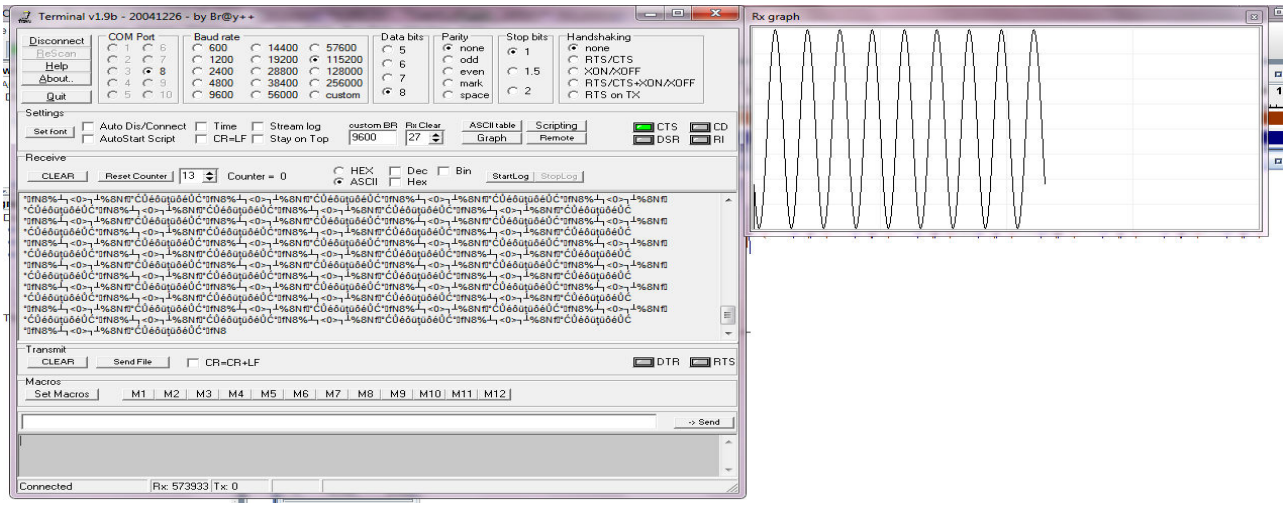


Fig-12**:** The Receiver frames captured in the UART receiver (PC).

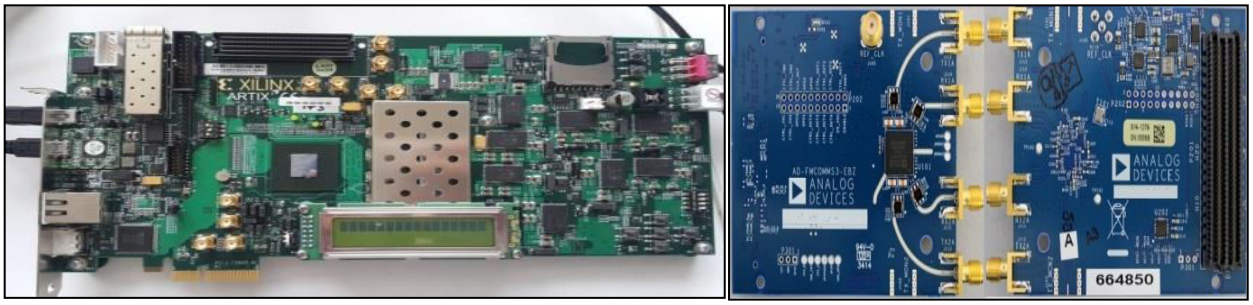


Fig-13**:** The AC701 EVM for the Artix®-7 FPGA (left), RFIC AD9364(FMCOMMS3) EVM board(right).

VI. FPGA DEVICE RESOURCE CONSUMPTION

Table 2 : Shows non exhaustive device utilization summary for FPGA (ARTIX7).

Table 2: Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	8,086	269,200	3%
Number of Slice LUTs	7,742	134,600	5%
Number used as logic	6,289	134,600	4%
Number used as Memory	771	46,200	1%

VII.CONCLUSION

In this proposed work, Low data rate burst transceiver is successfully implemented on FPGA. The results were compared with the Simulink simulation results. The constellation and eye diagram indicated in the results clearly shows the recovery of burst signals for QPSK. System was tested for large frequency and phase offsets wherein, carrier was successfully recovered.

ACKNOWLEDGEMENT

The authors acknowledge the support and guidance extended by Chief Executive (Airworthiness), CEMILAC, DRDO in writing this paper.Authors also acknowledge the guidance & the support extended by VTU, Belgaum & their

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

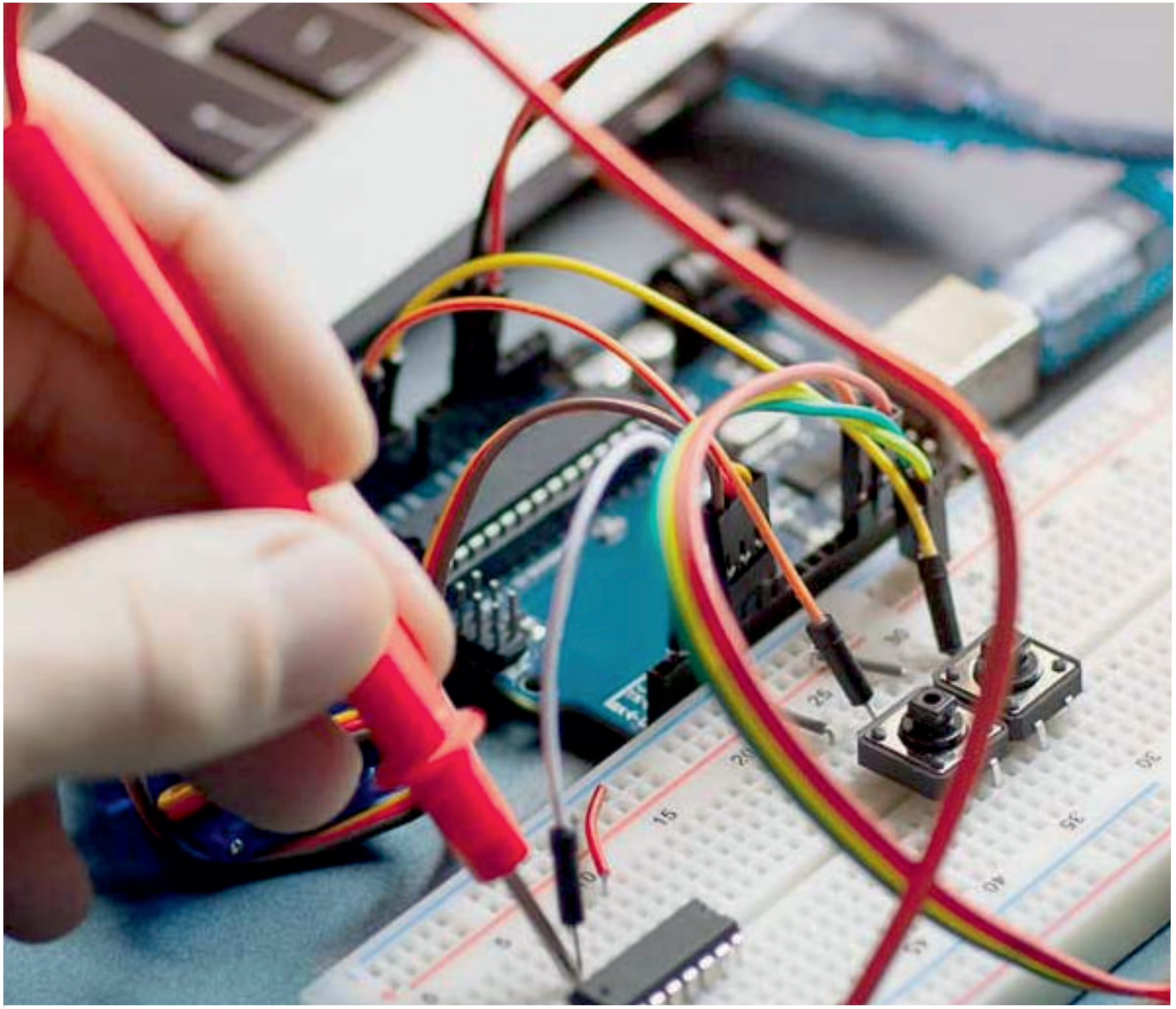
||Volume 10, Issue 4, April 2021||

DOI:10.15662/IJAREEIE.2021.1004037

doctoral team for their continual review.

REFERENCES

[1] Linda.M. Davis, DavidHaley,AndrePollok, Ying Chen-"Satellite Links and Software Defined Radio for Remote Communications and Sensor Data Gathering"-Institute of telecommunications research university of South Australia.
[2] Pedro Pinho, Mario Vestias-"AHigh-Rate MIMO Receiver in an FPGA" -IEEE Xplore 2012.
[3] Kevin Skey John Bradley, Karl Wagner - "A reuse approach for FPGA-based SDR waveforms"- MITRE Corporation Bedford MA.
[4] Emre Gunduzhan, K.Dewayne Brown- "Narrowband satellite communications: challenges and emerging solutions"-John Hopkins APL Technical Digest, Volume 33 Number1(2015), www.jhuapl.edu/techdigest.
[5] Durga Digdarshini, Mahesh Kumar, Gopichand Khot, TVS Ram,VK Tank- "FPGA implementation of automatic modulation recognition system for advanced SATCOM system"-2014 International Conference on Signal Processing and Integrated Networks(SPIN).
[6] Shahana K, Ravi Kumar Gupta, K.S. Parikh- "SDR implementation of low frequency trans-receiver on FPGA"-2014 International conference on signal processing and integrated networks (SPIN).
[7] Uma Devi, Madhavi D, Akshay Kumar "Carrier recovery and clock recovery for QPSK Demodulation"-IJRET: International Journal of Research in Engineering and Technology.
[8] Deepak Mishra, KS Dasgupta, S Jit- "Efficient QPSK Burst demodulator for onboard application"-Deepak Mishra et al/(IJCSIT) International Journal of Computer Science and Information Technologies Vol.3(3), 2012, 4053-4058.



INNO SPACE
SJIF Scientific Journal Impact Factor

Impact Factor:
7.122

ISSN INTERNATIONAL STANDARD SERIAL NUMBER INDIA

निस्केयर NISCAIR

International Journal of Advanced Research

in Electrical, Electronics and Instrumentation Engineering

9940 572 462 6381 907 438 ijareeie@gmail.com

www.ijareeie.com

Scan to save the contact details