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Mitigation of Interharmonics in PV Systems with Maximum Power Point Tracking Modification

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ABSTRACT: Interharmonics are emerging power quality challenges in grid-connected Photovoltaic (PV) systems. Previous studies and field measurements have confirmed the evidence of interharmonic emission from PV inverters, where the Maximum Power Point Tracking (MPPT) is one of the main causes for interharmonics. In that regard, the MPPT parameters such as their sampling rate has a strong impact on the interharmonic characteristic of the PV system. In general, there is a trade-off between the interharmonic emission and the MPPT performance when selecting the sampling rate of the MPPT algorithm. More specifically, employing a faster MPPT sampling rate will improve the MPPT efficiency, but it will also increase the interharmonic emission level. To solve this issue, a new mitigating solution for interharmonics in PV systems is proposed in this paper. The proposed method modifies the MPPT algorithm in a way to randomly select the sampling rate between the fast and the slow value. By doing so, the interharmonics in the output current can be effectively reduced due to the distribution of the frequency spectrum. On the other hand, the MPPT performance of the proposed method can be maintained similar to the case when employing a fast MPPT sampling rate. The effectiveness of the proposed interharmonic mitigation has been validated experimentally on a single-phase grid-connected PV system.

KEYWORDS: SOLAR PANEL, POWER TRANSFORMER,MOSFET,POWER SUPPLY .

I INTRODUCTION

With an increasing penetration level of Photovoltaic (PV) systems, challenging issues related to the grid integration have been arisen in the last decade. One of the emerging power quality problems for grid-connected PV systems is the inter-harmonics, which are defined as the frequency components that are non-integer times of the fundamental frequency. Recent studies have reported that PV inverters are the potential source of inter-harmonics emission for PV systems, which have been observed both in the laboratory testing environment and the field measurements .Although the inter-harmonics standard regarding the emission limit is still under development, the inter-harmonics can cause grid voltage fluctuations, flickering, and unintentionally disconnection of PV systems. Thus, the inter-harmonics emission in PV systems should be avoided and mitigations are needed.According to the previous studies, the Maximum Power Point Tracking (MPPT) operation is one of the main causes for inter-harmonics in PV systems. In particularly, the perturbation of the PV arrays voltage during the Maximum Power Point (MPP) searching inevitably induces power oscillations at the dc side, especially during the steady-state operation. This power oscillation contains a series of low-order frequency components, which is reflected in the frequency components of the amplitude of the output current jig j. When multiplying the amplitude of the output current with the phase angle, the output current ig will contain a certain amount of inter-harmonics frequencies due to the amplitude modulation following the control diagram To address this issue, a model to predict the inter-harmonics characteristic in PV systems has been proposed in, where the results from the inter-harmonics model agree well with the field observation. It has been demonstrated in that the inter-harmonics characteristic is strongly dependent on the MPPT algorithm parameters such as the perturbation step-size v step and the sampling rate MPPT. As discussed, the inter-harmonics emission can be effectively alleviated by reducing the sampling rate of the MPPT algorithm. However, this will inevitably slow down the tracking performance of the MPPT algorithm, which may reduce the MPPT efficiency.

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II PROPOSED SYSTEM

With the conventional MPPT implementation, there is a trade-off between the inter-harmonics emission and the MPPT efficiency when selecting the sampling rate of the MPPT algorithm. To solve this issue, a new mitigating solution for the inter-harmonics in PV systems has been proposed in this paper. The proposed method modifies the MPPT algorithm by randomly selecting the sampling rate of the MPPT algorithm during the operation. By doing so, the frequency spectrum of the output current can be smoothening and the amplitude of the dominant inter-harmonics can be significantly reduced. Moreover, the MPPT performance of the proposed mitigating solution can be maintained close to the conventional MPPT operation with a fast MPPT sampling rate, where similar tracking efficiency during a dynamic operating condition can be achieved. The performance of the proposed method has been validated experimentally under both steady-state (e.g., inter-harmonics) and dynamic operations (e.g., MPPT efficiency).

The experimental test in this paper is conducted based on the single-stage single-phase PV inverter, where the system parameters are given, In this configuration, the PV inverter is employed to control the power extraction from the PV arrays and convert it to the ac power delivered to the grid. In order to maximize the PV energy yield, the operating voltage of the PV arrays (i.e., corresponding to the dc-link voltage vdc) is determined by the MPPT algorithm during the operation. The dc-link voltage vdc is regulated through the control of the output current ig by a current controller, where the phase angle of the output current is obtained using a Phase-Locked Loop.

The proposed system deals with the Three phase inverter, where the gate signal is fed by a PWM generator regulated by SRF-PLL theory. This theory is used in compensating the harmonics and reactive power of the inverter and then fed to the distributing system. PI controller is used in order to normalize and minimize error signal form the system and it is a feedback controller. Here the theory compares the actual real and reactive power with the reference power using Park and Clarke transformation.

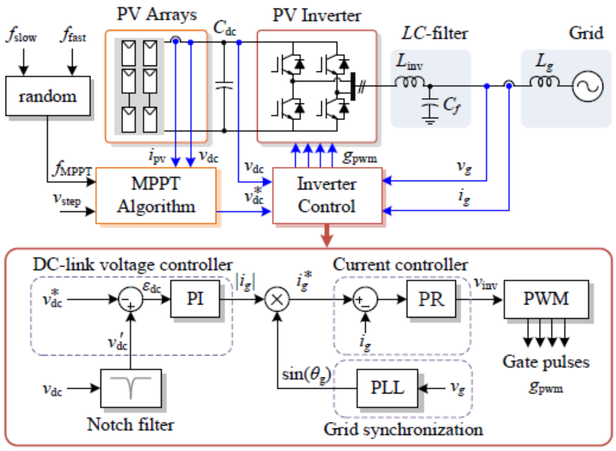

Fig 1 System Configuration

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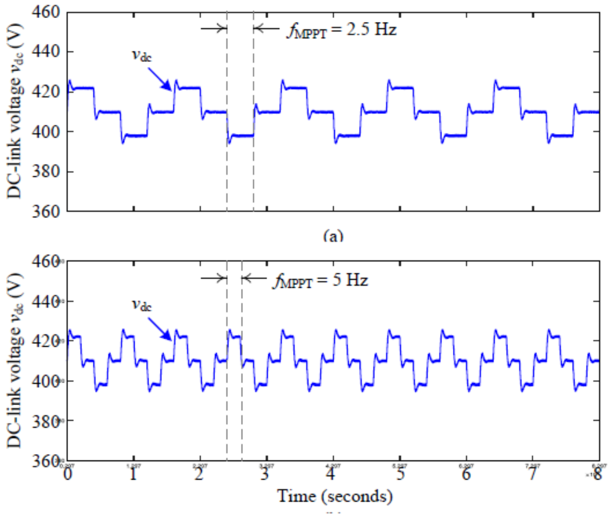

Fig 2 Vdc waveform

2.7 PHOTOVOLTAIC (PV) POWER SYSTEM

PV power system converts sunlight into electricity. The basic unit of a photovoltaic power system is the PV cell, where cells may be grouped to form panels or modules. The panels then can be grouped to form large photovoltaic array that connected in series or parallel. Panels connected in parallel increase the current and connected in series provide a greater output voltage. A photovoltaic system, also PV system or solar power system, is a power system designed to supply usable solar power by means of photovoltaic. It consists of an arrangement of several components, including solar panels to absorb and convert sunlight into electricity, a solar inverter to convert the output from direct to alternating current, as well as mounting, cabling, and other electrical accessories to set up a working system. It may also use a solar tracking system to improve the system's overall performance and include an integrated battery solution, as prices for storage devices are expected to decline. Strictly speaking, a solar array only encompasses the ensemble of solar panels, the visible part of the PV system, and does not include all the other hardware, often summarized as balance of system (BOS). As PV systems convert light directly into electricity, they are not to be confused with other solar technologies, such as concentrated solar power or solar thermal, used for heating and cooling.

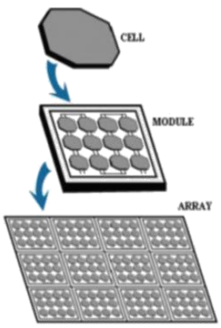

Fig 2.4 Photovoltaic (PV) Power System

2.8 PHOTOVOLTAIC CELL

The solar cells are made from semiconductor materials that able to generate electric current when being exposed to sunlight radiation. When a photon (particle of light) strikes a photovoltaic cell, some of the energy it brings is captured by the semiconductor material. That energy knocks electron loose, allowing them to flow freely. Electric fields created between the positive layer (P-type) and the negative layer (N-type) of the cells then force the loose electrons to go in

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certain direction through a connecting wire as direct current (DC) electricity. Photons in sunlight hit the solar panel and are absorbed by semiconducting materials, such as doped silicon.

Electrons are excited from their current molecular/atomic orbital. Once excited, an electron can either dissipate the energy as heat and return to its orbital or travel through the cell until it reaches an electrode. Current flows through the material to cancel the potential and this electricity is captured. The chemical bonds of the material are vital for this process to work, and usually silicon is used in two layers, one layer being doped with boron, the other phosphorus. These layers have different chemical electric charges and subsequently both drive and direct the current of electrons.

2.9 PHOTOVOLTAIC MODULE

The voltage generated by a single solar cell is very low, around 0.5V. So, a number of solar cells are connected in both series and parallel connections to achieve the desired output. In case of partial shading, diodes may be needed to avoid reverse current in the array. Good ventilation behind the solar panels is provided to avoid the possibility of less efficiency at high temperatures.

A PV module is an assembly of photo-voltaic cells mounted in a framework for installation. Photo-voltaic cells use sunlight as a source of energy and generate direct current electricity. A collection of PV modules is called a PV Panel, and a system of Panels is an Array. Arrays of a photovoltaic system supply solar electricity to electrical equipment.

Fig 2.5 Photovoltaic module

2.10 PHOTOVOLTAIC ARRAY

Again the power produced by a single module is not sufficient to meet the power demands for most of the practical purposes. PV arrays can use inverters to convert the dc output into ac and use it for motors, lighting and other loads. The modules are connected in series for more voltage rating and then in parallel to meet the current specifications.

The voltage generated by a single solar cell is very low, around 0.5V. So, a number of solar cells are connected in both series and parallel connections to achieve the desired output. In case of partial shading, diodes may be needed to avoid reverse current in the array. Good ventilation behind the solar panels is provided to avoid the possibility of less efficiency at high temperatures.

Photovoltaic cells and panels convert the solar energy into direct-current (DC) electricity. The connection of the solar panels in a single photovoltaic array is same as that of the PV cells in a single panel. The panels in an array can be electrically connected together in a series, a parallel, or a mixture of the two, but generally a series connection is chosen to give an increased output voltage. For example, when two solar panels are wired together in series, their voltage is doubled while the current remains the same.

The size of a photovoltaic array can consist of a few individual PV modules or panels connected together in an urban environment and mounted on a rooftop, or may consist of many hundreds of PV panels interconnected together in a field to supply power for a whole town or neighbourhood. The flexibility of the modular photovoltaic array (PV system) allows designers to create solar power systems that can meet a wide variety of electrical needs, no matter how large or small.

It is important to note that photovoltaic panels or modules from different manufacturers should not be mixed together in a single array, even if their power, voltage or current outputs are nominally similar. This is because differences in the solar panels I-V characteristic curves as well as their spectral response are likely to cause additional mismatch

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losses within the array, thereby reducing its overall efficiency.

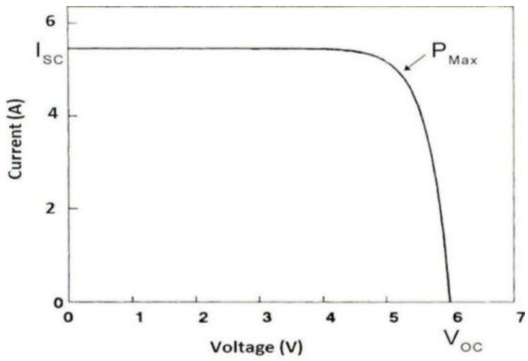
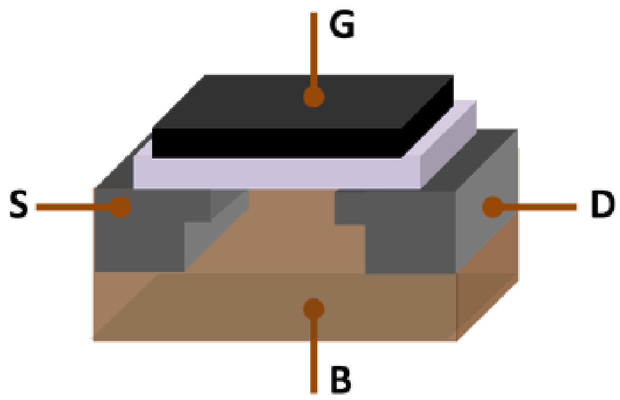


Fig 2.6 Typical I-V characteristics of solar panel

III.METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

The Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET, MOS-FET, or MOS FET) is a type of transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagram.



MOSFET showing gate (G), body (B), source (S) and drain (D) terminals. The gate is separated from the body by an insulating layer (white)

Fig 3.1 MOSFET

The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. In Enhancement Mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts via the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer. The channel can contain electrons (called an nMOSFET or nMOS), or holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate.

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In the less common depletion mode MOSFET, detailed later on, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and conductivity is decreased by application of a field that depletes carriers from this surface layer. The "metal" in the name MOSFET is now often a misnomer because the previously metal gate material is now often a layer of polysilicon (polycrystalline silicon). Aluminium had been the gate material until the mid-1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates. Likewise, the "oxide" in the name can be a misnomer, as different dielectric materials are used with the aim of obtaining strong channels with smaller applied voltages. An Insulated-Gate Field-Effect Transistor or IGFET is a related term almost synonymous with MOSFET. The term may be more inclusive, since many "MOSFETs" use a gate that is not metal, and a gate insulator that is not oxide. Another synonym is MISFET for Metal–Insulator–Semiconductor FET. The basic principle of the field-effect transistor was first patented by Julius Edgar Lilienfeld in 1925.

The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common. In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts *via* the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer.

When a voltage is applied between the gate and body terminals, the electric field generated penetrates through the oxide and creates an "inversion layer" or "channel" at the semiconductor-insulator interface. The inversion channel is of the same type, p-type or n-type, as the source and drain, thus it provides a channel through which current can pass. Varying the voltage between the gate and body modulates the conductivity of this layer and thereby controls the current flow between drain and source.

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM and Intel, recently started using a chemical compound of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETs. Research continues on creating insulators with acceptable electrical characteristics on other semiconductor material. In order to overcome the increase in power consumption due to gate current leakage, a high-κ dielectric is used instead of silicon dioxide for the gate insulator, while polysilicon is replaced by metal gates (see Intel announcement). The gate is separated from the channel by a thin insulating layer, traditionally of silicon dioxide and later of silicon oxynitride. Some companies have started to introduce a high-κ dielectric + metal gate combination in the 45 nanometer node.

3.1 METAL–OXIDE–SEMICONDUCTOR STRUCTURE

The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor. When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor. If we consider a p-type semiconductor (with the density of acceptors, P the density of holes P= NA in neutral bulk), a positive voltage, , from gate to body creates a depletion layer by forcing the positively charged holes away from the gate-insulator/semiconductor interface, leaving exposed a carrier-free region of immobile, negatively charged acceptor ions (see doping (semiconductor)).

If is high enough, a high concentration of negative charge carriers forms in an inversion layer located in a thin layer next to the interface between the semiconductor and the insulator. Unlike the MOSFET, where the inversion layer electrons are supplied rapidly from the source/drain electrodes, in the MOS capacitor they are produced much more slowly by thermal generation through carrier generation and recombination centers in the depletion region. Conventionally, the gate voltage at which the volume density of electrons in the inversion layer is the same as the volume density of holes in the body is called the threshold voltage. When the voltage between transistor gate and source (VGS) exceeds the threshold voltage (Vth), it is known as overdrive voltage. This structure with p-type body is the basis of the n-type MOSFET, which requires the addition of an n-type source and drain regions.

3.2 MOSFET STRUCTURE AND CHANNEL FORMATION

An applied gate voltage bends bands, depleting holes from surface (left). The charge inducing the bending is balanced by a layer of negative acceptor-ion charge (right). Bottom panel: A larger applied voltage further depletes holes but conduction band lowers enough in energy to populate a conducting channel. A metal–oxide–semiconductor field-

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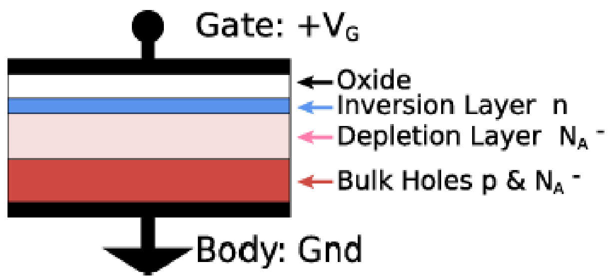
effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide.

If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a "+" sign after the type of doping.



Metal–oxide–semiconductor structure on p-type silicon

Fig 3.1 MOS Structure

If the MOSFET is an n-channel or nMOS FET, then the source and drain are "n+" regions and the body is a "p" region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are "p+" regions and the body is a "n" region. The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel.

3.3 REASONS FOR MOSFET SCALING

Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every year once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip.

The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. In order to meet the demand of high density chips in MOS technology, it is required that MOSFET are scaled down i.e. reduction in the size of transistor, so that high packaging density can be achieved.

Constant electric scaling model and constant voltage scaling model is used for scaling. Explanation: α is used as the scaling factor for linear dimensions where as β is used for supply voltage Vdd, gate oxide thickness etc.

Feature scaling is essential for machine learning algorithms that calculate distances between data. Therefore, the range of all features should be normalized so that each feature contributes approximately proportionately to the final distance.

Scaling, which is not as painful as it sounds, is a way to maintain a cleaner mouth and prevent future plaque build-up. Though it's not anyone's favorite past-time to go to the dentist to have this procedure performed, it will help you maintain a healthy mouth for longer.

3.4 INCREASED GATE-OXIDE LEAKAGE

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is on and to reduce subthreshold leakage when the transistor is off. However, with current gate oxides with a thickness of around 1.2 nm (which in silicon is ~5 atoms thick) the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption. Silicon dioxide has traditionally been used as the gate insulator. Silicon dioxide however has a modest dielectric constant. Increasing the dielectric constant of the gate dielectric allows a thicker layer

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while maintaining a high capacitance (capacitance is proportional to dielectric constant and inversely proportional to dielectric thickness). All else equal, a higher dielectric thickness reduces the quantum tunneling current through the dielectric between the gate and the channel.

3.5 HEAT PRODUCTION

Large heat sinks to cool power transistors in a TRM-800 audio amplifier The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate more slowly at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling devices and methods are now required for many integrated circuits including microprocessors. Power MOSFETs are at risk of thermal runaway. As their on-state resistance rises with temperature, if the load is approximately a constant-current load then the power loss rises correspondingly, generating further heat. When the heat sink is not able to keep the temperature low enough, the junction temperature may rise quickly and uncontrollably, resulting in destruction of the device.

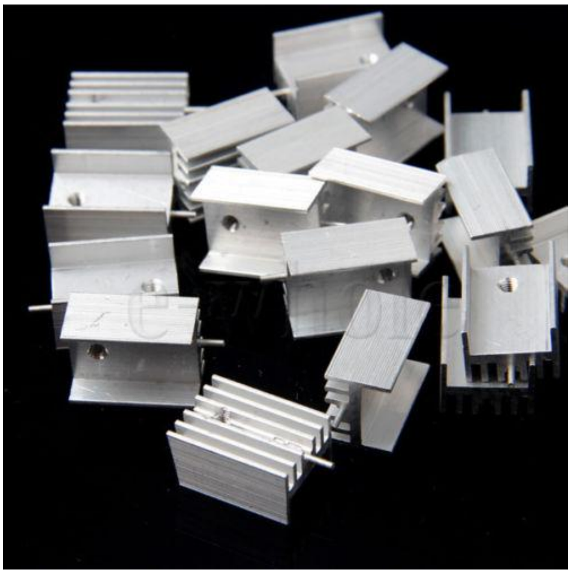

Fig 3.2 Heat Sink

A heat sink is a component that increases the heat flow away from a hot device. It accomplishes this task by increasing the device's working surface area and the amount of low-temperature fluid that moves across its enlarged surface area.

The components that generate the most heat in your computer are the CPU (central processing unit), video card (if your computer has one), and the power supply. They always have some cooling, usually a fan. Other components that may have a heat sink include the north bridge, south bridge, and memory.

A heat sink should be attached to a voltage regulator in order to dissipate excess power that may enter into the regulator. This prevents excess voltage from destroying and overheating the voltage regulator, since the heat sink dissipates the excess power off as heat.

A heat sink for power MOSFETs, some basic calculations must be made. The first step to selecting a heat sink is calculating the total power dissipation of the components in the circuit application. Power dissipation can be determined from circuit calculations or from efficiency measurements.

A heat sink (also commonly spelled heat sink) is a passive heat exchanger that transfers the heat generated by an electronic or a mechanical device to a fluid medium, often air or a liquid coolant, where it is dissipated away from the device, thereby allowing regulation of the device's temperature.

IV.SNUBBER CIRCUIT

A snubber is a device used to suppress ("snub") some phenomenon, such as:

- Voltage transients in electrical systems.
- Pressure transients in fluid systems.
- Excess force or rapid movement in mechanical systems.

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Snubber are frequently used in electrical systems with an inductive load where the sudden interruption of current flow leads to a sharp rise in voltage across the current switching device, in accordance with Faraday's law. This transient can be a source of electromagnetic interference (EMI) in other circuits. Additionally, if the voltage generated across the device is beyond what the device is intended to tolerate, it may damage or destroy it. The snubber provides a short-term alternative current path around the current switching device so that the inductive element may be discharged more safely and quietly. Inductive elements are often unintentional, but arise from the current loops implied by physical circuitry. While current switching is everywhere, snubber will generally only be required where a major current path is switched, such as in power supplies. Snubber are also often used to prevent arcing across the contacts of relays and switches and the electrical interference and welding/sticking of the contacts that can occur.

The diode must immediately enter into forward conduction mode as the driving current is interrupted. Most ordinary diodes, even "slow" power silicon diodes, are able to turn on very quickly,[1] in contrast to their slow reverse recovery time.

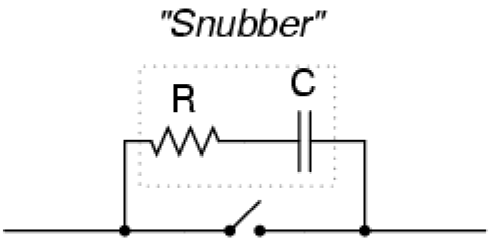

Fig 4.1 Snubber Circuit

4.1 DIODE SNUBBER

When the current flowing is DC, a simple rectifier diode is often employed as a snubber. The snubber diode is wired in parallel with an inductive load (such as a relay coil or electric motor). The diode is installed so that it does not conduct under normal conditions. When the external driving current is interrupted, the inductor current flows instead through the diode. The stored energy of the inductor is then gradually dissipated by the diode voltage drop and the resistance of the inductor itself. One disadvantage of using a simple rectifier diode as a snubber is that the diode allows current to continue flowing for some time, causing the inductor to remain active for slightly longer than desired. Circuit designs must consider this delay in the dropping-out of the actuator.

The diode must immediately enter into forward conduction mode as the driving current is interrupted. Most ordinary diodes, even "slow" power silicon diodes, are able to turn on very quickly, in contrast to their slow reverse recovery time. These are sufficient for snubbing electromechanical devices such as relays and motors. In high-speed cases, where the switching is faster than 10 nanoseconds, such as in certain switching power regulators, "fast", "ultrafast", or Schottky diodes may be required.

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Snubber are frequently used in electrical systems with an inductive load where the sudden interruption of current flow leads to a sharp rise in voltage across the current switching device ("inductive kick"), in accordance with Faraday's law. This transient can be a source of electromagnetic interference (EMI) in other circuits. Additionally, if the voltage generated across the device is beyond what the device is intended to tolerate, it may damage or destroy it. The snubber provides a short-term alternative current path around the current switching device so that the inductive element may be safely discharged. Inductive elements are often unintentional, but arise from the current loops implied by physical circuitry. While current switching is everywhere, snubbers will generally only be required where a major current path is switched, such as in power supplies. Snubbers are also often used to prevent arcing across the contacts of relays and switches, or the electrical interference, or the welding of the contacts that can occur (see also arc suppression).

A simple RC snubber uses a small resistor (R) in series with a small capacitor (C). This combination can be used to suppress the rapid rise in voltage across a thyristor, preventing the erroneous turn-on of the thyristor; it does this by limiting the rate of rise in voltage (dv/dt) across the thyristor to a value which will not trigger it. An appropriately-designed RC snubber can be used with either DC or AC loads. This sort of snubber is commonly used with inductive loads such as electric motors. The voltage across a capacitor cannot change instantaneously, so a

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decreasing transient current will flow through it for a small fraction of a second, allowing the voltage across the switch to increase more slowly when the switch is opened. Determination of voltage rating can be difficult owing to the nature of transient waveforms, and may be defined simply by the power rating of the snubber components and the application. RC snubbers can be made discretely and are also built as a single component

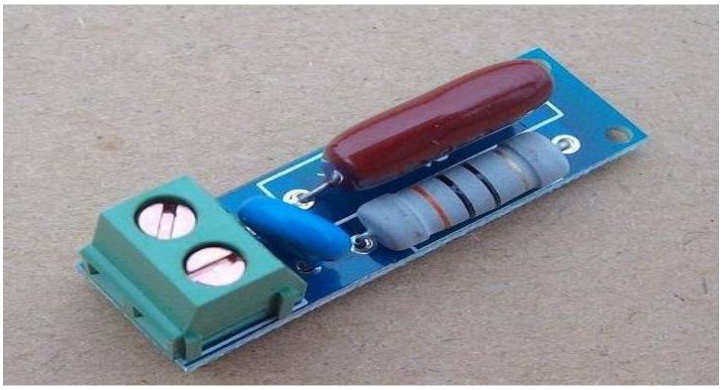

Fig 4.2 Diode Snubber

V.PULSE-WIDTH MODULATION

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a modulation technique that controls the width of the pulse, formally the pulse duration, based on modulator signal information. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors. In addition, PWM is one of the two principal algorithms used in photovoltaic solar battery chargers, the other being MPPT. The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load.

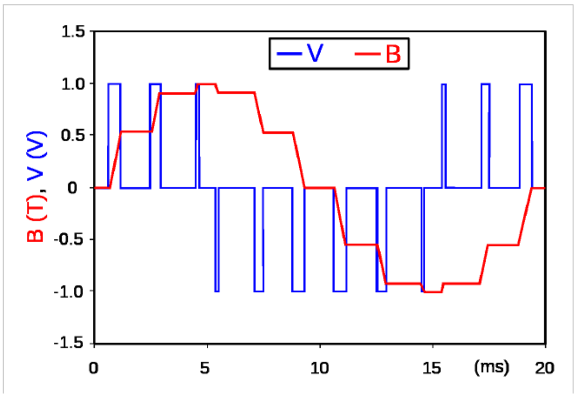

Fig 5.1 PWM

The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resultant waveform perceived by the load must be as smooth as possible. Typically switching has to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

The term duty cycle describes the proportion of 'on' time to the regular interval or 'period' of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully on.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch. Power loss, being the product of voltage and current, is thus in both cases close to zero. PWM also works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

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VI.MAXIMUM POWER POINT TRACKING

Maximum power point tracking (MPPT) is a technique that grid connected inverters, solar battery chargers and similar devices use to get the maximum possible power from one or more photovoltaic devices, typically solar panels, though optical power transmission systems can benefit from similar technology. Solar cells have a complex relationship between solar irradiation, temperature and total resistance that produces a non-linear output efficiency which can be analyzed based on the I-V curve. It is the purpose of the MPPT system to sample the output of the cells and apply the proper resistance (load) to obtain maximum power for any given environmental conditions. Citation needed MPPT devices are typically integrated into an electric power converter system that provides voltage or current conversion, filtering, and regulation for driving various loads, including power grids, batteries, or motors.

1. Solar inverters convert the DC power to AC power and may incorporate MPPT: such inverters sample the output power (I-V curve) from the solar cell and apply the proper resistance (load) so as to obtain maximum power.
2. MPP(Maximum power point) is the product of the MPP voltage(V mpp) and MPP current(I mpp): some solar panels have a higher maximum power than others.

a. This section covers the theory and operation of "Maximum Power Point Tracking" as used in solar electric charge controllers.

An MPPT, or maximum power point tracker is an electronic DC to DC converter that optimizes the match between the solar array (PV panels), and the battery bank or utility grid. To put it simply, they convert a higher voltage DC output from solar panels (and a few wind generators) down to the lower voltage needed to charge batteries.

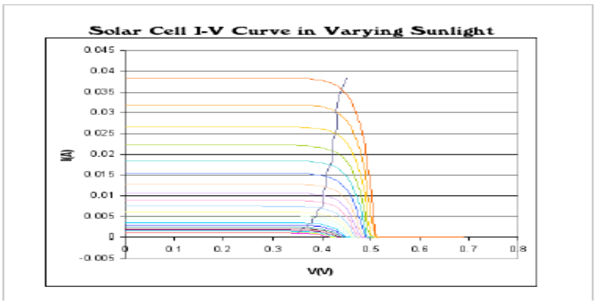

Fig 6.1 I-V Curve

6.1 INTER-HARMONICS REDUCTION

The consequence of randomly applying the MPPT sampling rate is also reflected in the perturbation rate of the output current. In the output current with the proposed randomly applied MPPT sampling rate of f slow = 2.5 Hz and f fast = 5 Hz is shown. The corresponding MPPT sampling rate during the operation is also demonstrated when analyzing the frequency spectrum of the output current .it can be observed from the results that the dominant inter-harmonics in the output current can be reduced significantly. With the proposed method, the peak amplitude of the inter-harmonics is 0.07 A, which is less than half of the case when employing a fast MPPT sampling rate .In fact, the frequency spectrum is more distributed due to the randomly applied perturbation of the output current. This is preferable since a certain inter-harmonics component may trigger an undamped resonance, causing stability problem. Moreover, in the case of parallel-connected PV inverters, the stochastic behavior of perturbation has a high probability to counteract one another due to its randomness. This can potentially smooth out the total power oscillation and thereby further reduce the inter-harmonics in the total output current. significant improvement compared to the case with fMPPT = 2.5 Hz.

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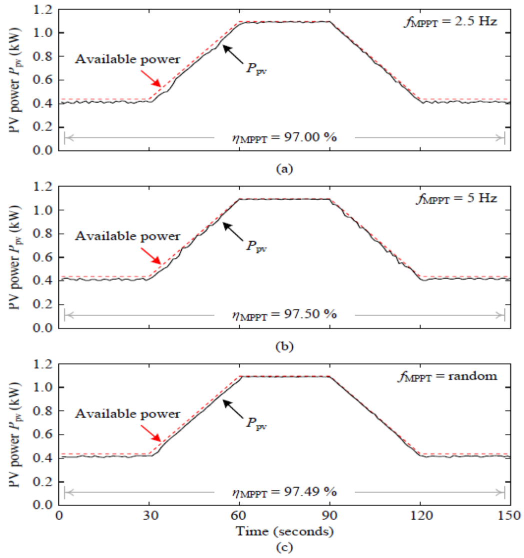

Fig 6.2 Inter Harmonics Reduction

VII. HARDWARE COMPONENTS

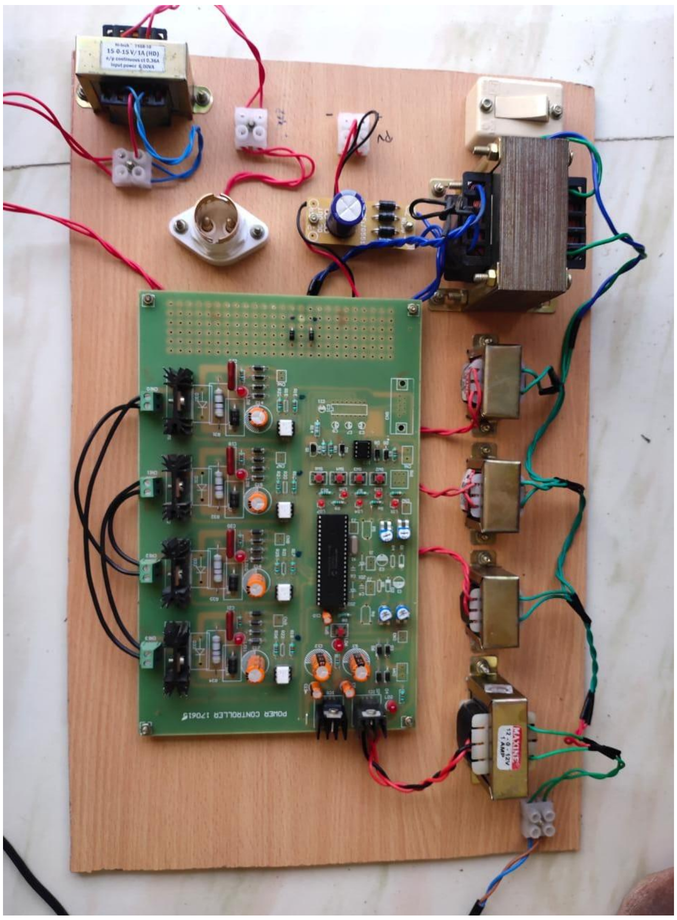

Fig.7.1 Hardware component

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VIII.CONCLUSION

With the conventional MPPT implementation, there is a trade-off between the inter-harmonics emission and the MPPT efficiency when selecting the sampling rate of the MPPT algorithm. To solve this issue, a new mitigating solution for the inter-harmonics in PV systems has been proposed in this paper. The proposed method modifies the MPPT algorithm by randomly selecting the sampling rate of the MPPT algorithm during the operation. By doing so, the frequency spectrum of the output current can be smoothen and the amplitude of the dominant inter-harmonics can be significantly reduced. Moreover, the MPPT performance of the proposed mitigating solution can be maintained close to the conventional MPPT operation with a fast MPPT sampling rate, where similar tracking efficiency during a dynamic operating condition can be achieved. The performance of the proposed method has been validated experimentally under both steady-state (e.g., inter-harmonics) and dynamic operations (e.g., MPPT efficiency).

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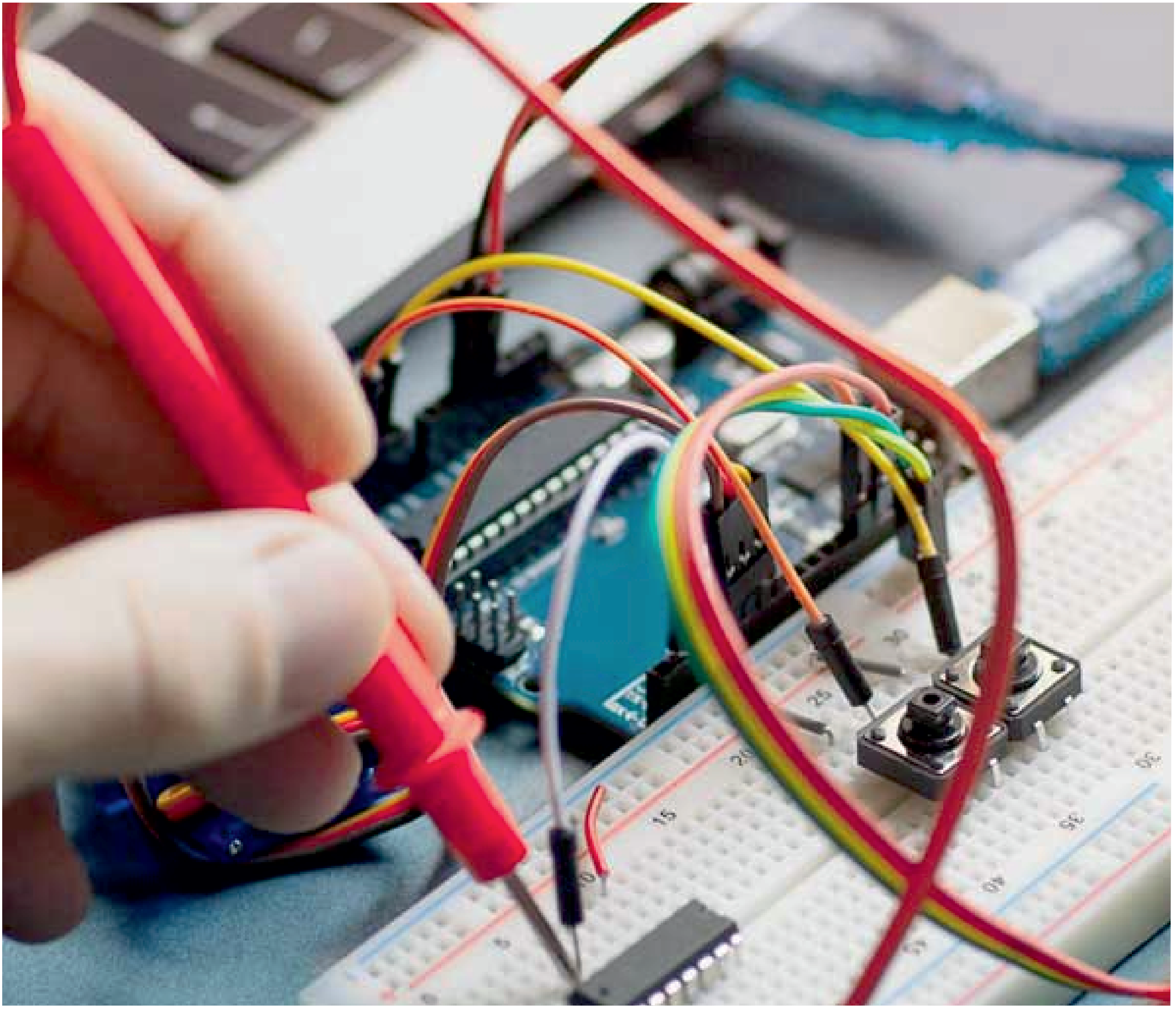

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