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Analysis And Research A Soft Switching Bidirectional DC-DC Converter Without Auxilary Switches Using Fuzzy Logic Controller

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ABSTRACT: In this paper, a new soft switching bridgeless single-phase power factor correction (PFC) converters is presented and analyzed. Employing an auxiliary switch, the input current dead angle that is the main drawback of the existing buck type PFCs is omitted and thus power factor (PF) is improved which is the main contribution of the paper. Proposed PFC converter operates under discontinuous conduction mode (DCM) and draws sinusoidal input current from power supply inherently. All switches and diodes are turned on and off under soft switching which leads to low switching losses and elimination of diode reverse recovery problems. Also, minimum numbers of semiconductor devices are in the power flow path that reduce the conduction losses. A 120W laboratory prototype is implemented and experimental results verify validity of theoretical analysis and show efficiency of 92.1%. In addition, total harmonic distortion (THD) of 3.3% is achieved and the input current harmonics complies with IEC61000-3-2 Class D requirements.

KEYWORDS: power factor correction (PFC), Bridgeless buck converter, dead angle, soft switching

I. INTRODUCTION

Today, the incredible growth in the use of computers, server, telecommunication systems, and some applications such as battery chargers for electrical vehicles and employing more and more power supplies, have increased worldwide energy consumption and global warming and economic issues. Therefore, the standards such as the California Energy Commission (CEC) were set to control the energy efficiency and reduce the energy consumption [1]. Also, in order to minimize the power grid damages resulted by injected harmonics and to achieve high power factor (PF) and low total harmonic distortion (THD) in electrical equipments, standards such as IEC61000-3-2 should be met. Thus, researchers have focused on improving power factor correction (PFC) topologies. The boost converter is widely used as a PFC converter due to its high PF and simplicity. However, boost converter cannot provide low output voltage. High output voltage of boost PFC converter usually increase cost and conduction losses of the post regulator. Although boost converter is the best candidate for several applications [2]-[4], due to inrush current problem and the required low output voltage in some applications such as server, telecommunication, storage systems and networking, the researchers have introduced buck type PFC converters [5]. The main drawback in the buck type PFCs is existence of dead angle when the output voltage is higher than input voltage, which leads to high current distortion and low PF. Usually for power supplies, the universal AC input (90-270 Vrms) is required to be used worldwide that leads to low PF and high THD when buck type PFC is applied. For example, the introduced buck PFC in [6] with universal input cannot pass IEC61000-3-2 (Class D) easily. Therefore, in order to manage this challenge, the output voltage should be designed carefully and much lower than input voltage which results in reduction of efficiency [7] and complicates design of next stage. Also, according to IEC61000-3-2 and Japanese Industrial Standard (JIS-C61000-3-2), the buck type PFC with dead angle in the input current should be employed in applications with lower power levels due to their low PF [8]. Based on abovementioned explanations, the dead angle should be eliminated in buck type PFC. In efforts to

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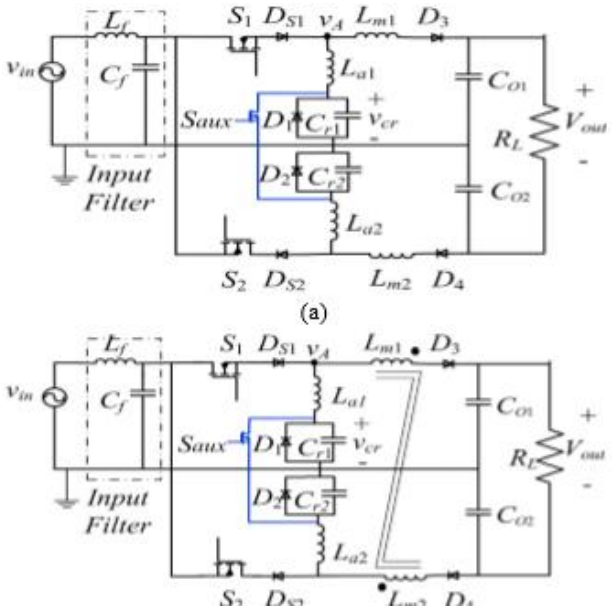
eliminate input current dead angle, [9]-[14] have been proposed. In [9], a buck type converter with coupled inductors and bulky capacitor in positive half-line cycle and a Flyback converter in negative half-line cycle are applied and in [10], an auxiliary switch is added to the buck converter to omit input current dead angle. Both of these topologies operate under hard switching condition and the efficiency is low. Integrated buck-Flyback converters have been introduced in [11]-[13] that Flyback converter can regulate input current during dead angle. However, these structures contain additional extra semiconductors. Also, in [14] Flyback and Forward converters with quasi-resonant control (QR) are merged together. The switch is turned off under hard switching and switch voltage stress is high. Furthermore, it is very hard to implement QR control in this converter. In order to reduce conduction losses of bridge diode which is followed by DC/DC converter as PFC circuit, bridgeless PFC converters are applied. In bridgeless technique, input bridge diode and PFC stages are merged together to reduce the number of simultaneously conducting semiconductor devices. Bridgeless CUK and SEPIC converters have been proposed in [15]-[20]. These topologies do not need large input filter since they have continuous input current even at discontinuous conduction mode (DCM) mode. However, in these converters two inductors and one capacitor are in the power path and increase conduction losses. In [20], the introduced bridgeless PFC has only one switch. However, three semiconductor devices are in power flow path and cannot fulfill bridgeless topology purpose. Also, since all switches operate at hard switching condition in [15]-[20], EMI noise is problematic and results in limited operating frequency, leading to high converter size and cost due to increment of heat sink size. A bridgeless PFC operating in Discontinuous Capacitor Voltage Mode (DCVM) is explained in [21]. Unlike the regular buck PFC, its input current is continuous that reduces input filter size. However



1. Proposed soft switching PFC converters with unity power factor. (a) Type- 1. (b) Type- 2

this type of PFC cannot achieve acceptable PF at light loads. Also, it suffers from high switch voltage stress and zero crossing dead angle in its input current. In bridgeless Flyback PFC [22], RCD snubber is necessary to protect switches against stored energy in leakage inductance that increases switching losses and size. To reduce switching losses and enhance switching frequency, Zero Voltage Transition (ZVT) and Zero Current Transition (ZCT) techniques are adopted for bridgeless converters [23]-[30]. In [23] the diode of auxiliary circuit is in the power path. In [24], the circulating energy of the converter is high and when switches are off, three semiconductors are in the power flow path that increases conduction losses. Structures of auxiliary circuits in [25]-[28] are complex. In [29], the auxiliary switch cannot operate under soft switching condition that decreases efficiency. Also, converter of [30] is based on SEPIC converter and the number of passive elements in the power path is high. The main drawback of applying ZVT and ZCT techniques is increased number of passive elements and semiconductors that reduce power density and increase implementation cost. Based on abovementioned explanations, soft switching step-down PFC converter with high PF and low THD is required. Therefore, in this paper a new step-down bridgeless PFC converter is introduced by applying switched resonator method [31] into bridgeless PFC converter [8] while eliminating input current dead angle with a simple technique as shown in Fig. 1. The introduced bridgeless PFC in [8] suffers from dead angle in the input current and hard switching condition which increases THD and reduces efficiency respectively. Switching losses in buck type

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PFC converters are very high since switch turns off under output current which is very large. All diodes and switches of the proposed PFC in this article turn on and off under zero current switching (ZCS) condition. Voltage stress of switches S1 and S2 is lower than SEPIC and Cuk PFC and minimum number of semiconductors are in the power flow path. In addition, by using reverse voltage blocking switches (such as RB-IGBTas the unidirectional switch for high voltage applications,, series diodes with the main switches can be eliminated [8],[21] and [32]. These features result in reduction of conduction and switching losses. Furthermore, it should be noted that switching losses are very low too due to achieved ZCS condition and elimination of tailing current losses. The resonant capacitors and inductors used in the proposed converter are smaller than passive elements used in conventional SEPIC and Cuk PFCs that reduce size and cost. The proposed PFC operates in DCM that leads to inherent PFC and reduced reverse recovery problems. As demonstrated in Fig. 1(b), the inductors Lm1 and Lm2 in PFC type-1 are coupled on the same magnetic core to reduce size. In order to omit dead angle when output voltage is higher than the input voltage and improve PF, auxiliary switch Saux is employed. It is shown that Saux is switched under zero voltage switching (ZVS) condition. The proposed PFC operates under soft switching condition that leads to low EMI noise. Also, the common mode noise of this structure is low [8]. In this paper, only the proposed bridgeless PFC type-1 will be discussed. In the next section, the PFC circuit structure and operation modes are explained. In section III, design procedure of elements and guidelines are focused. Experimental results are provided in section IV to verify validity of theoretical analysis.

II. OPERATING PRINCIPLES

In this section, proposed bridgeless PFC operating in DCM mode will be analyzed in details. During the positive half-line cycle D1, D3,DS1 ,S1, Saux, Lm1, La1 and Cr1 are active and during the negative half-line cycle D2, D4, DS2, S2, Saux, Lm2, La2 and Cr2 are used. Main switches can be switched by same floating signal and sensing positive and negative halfline cycles is not required. Because of converter symmetrical operation, only the positive half-line cycle of type- 1 converter is analyzed. Also, before analyzing the circuit, it is assumed that all semiconductor devices are off, stored energy in resonant elements is zero and load is supplied by output capacitors.

A. Operating in vin (t) > VO1 When the input voltage is higher than half of the output voltage, the proposed PFC operation modes are described in this section. During this section, Saux is off and S1 keeps switching. Theoretical key waveforms and circuit operations of proposed PFC during a switching period are illustrated in Fig. 2 and Fig. 3 respectively.

Mode 1 [t0-t1]: At the beginning of this mode, S1 and diodes DS1 and D3 are turned on at ZCS due to existence of La1 and Lm1. Lm1 current (iLm) increases linearlyby a slop of $vin(t) - Vo1\ Lm1$. Also, La1 starts a resonance with Cr1 through S1 and La1 current (iLa) increases in sinusoidal fashion. At the end of this mode, iLa and iLm become equal and reach I1. Also, resonant current and voltage equations are:

$$i_{Lm}(t) = \frac{v_{in}(t) - V_{o1}}{L_{m1}}(t - t_0) \qquad (1)$$

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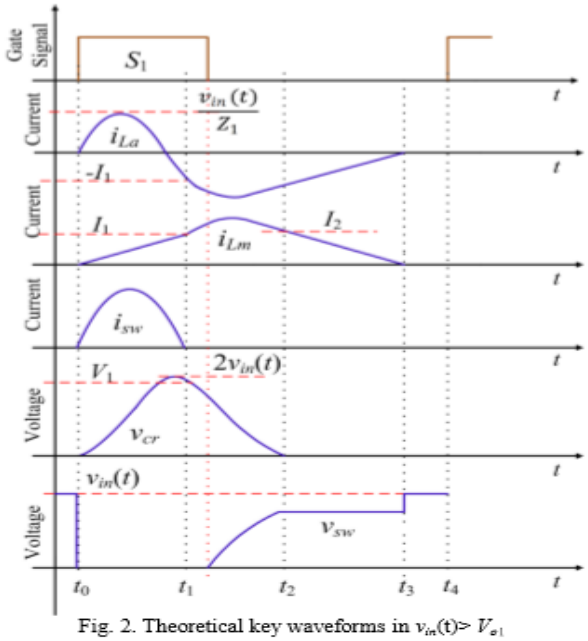

Fig. 2. Theoretical key waveforms in $v_{in}(t) > V_{o1}$

$$i_{La}(t) = \frac{v_{in}(t)}{Z_1} \sin \omega_1 (t - t_0) \quad (2)$$

$$v_{cr}(t) = v_{in}(t) \times \left[1 - \cos(\omega_1 (t - t_0)) \right] \quad (3)$$

$$Z_1 = \sqrt{\frac{L_{a1}}{C_{r1}}} \quad (4)$$

$$T_1 = \frac{2\pi}{\omega_1} = 2\pi \times \sqrt{L_{a1} \cdot C_{r1}} \quad (5)$$

Mode 2 [t1-t2]: At the beginning of this mode, since iLa and iLm are equal, S1 current is zero. Thus, S1 is turned off under ZCS condition. In addition, Lm1 is in series with La1 and Cr1 and begins a resonance until Cr1 voltage reaches zero and diode D1 turns on. Furthermore, based on (7), all of these happen approximately less than half of the resonance period. Hence, duration of this mode is considered as 1 2 *T*2. At the end of this mode, iLm and iLa reach I2. According to (6), iLm is sum of two sinusoidal terms, one of them increases and the other one decreases. Therefore, during this mode, the amplitude of inductors current does not change considerably with respect to its initial value at the beginning of this mode and I2 and I1 are almost equal.

$$i_{Lm}(t) = -i_{La}(t) = \frac{V_1 - V_{o1}}{Z_2} \times \sin(\omega_2 (t - t_1)) + I_1 \cos(\omega_2 (t - t_1)) \quad (6)$$

$$V_{cr}(t) = V_{o1} + (V_1 - V_{o1}) \times \cos(\omega_2 (t - t_1)) - Z_2 I_1 \sin(\omega_2 (t - t_1)) \quad (7)$$

$$T_2 = \frac{2\pi}{\omega_2} = 2\pi \times \sqrt{(L_{a1} + L_{m1}) C_{r1}} \quad (8)$$

$$Z_2 = \sqrt{\frac{L_{a1} + L_{m1}}{C_{r1}}} \quad (9)$$

Mode 3[t2-t3]: At t2, Diode D1 turns on under ZVS. Also, iLa and iLm currents decrease with slop of $Vo1$ $Lm1$+$La1$ since the output voltage is reversely placed across them. At the end of interval, iLm and iLa reach zero and D1 and D3 turn off under ZCS that eliminates reverse recovery problems.

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$$i_{Lm}(t) = -i_{La}(t) = I_2 - \frac{V_{o1}}{L_{a1} + L_{m1}}(t - t_2) \qquad (10)$$

According to (10) and description in mode 2, duration of this mode is:

$$t_3 - t_2 = \frac{L_{a1} + L_{m1}}{V_{o1}} I_1 \qquad (11)$$

Mode 4 [t3-t4]: In this interval, all the semiconductors are off and capacitors Co1 and Co2 supply load. This mode continues to the end of switching period

B. Operating in vin (t) < VO1 When the input voltage is smaller than half of the output voltage, the proposed PFC operation modes are explained in this section. During this section, Saux and S1 are switched together. Thus, two additional modes exist as described. It is noted that two next modes happen before mode 1. Theoretical key waveforms and circuit operations of proposed PFC during a switching period are illustrated in Fig. 4 and Fig. 5 respectively.

B. Operating in vin (t) < VO1 When the input voltage is smaller than half of the output voltage, the proposed PFC operation modes are explained in this section. During this section, Saux and S1 are switched together. Thus, two additional modes exist as described. It is noted that two next modes happen before mode 1. Theoretical key waveforms and circuit operations of proposed PFC during a switching period are illustrated in Fig. 4 and Fig. 5 respectively.

$$i_{La}(t) = \frac{v_{in}(t)}{L_{a1}}(t - t_{a0}) \qquad (12)$$

$$I_{a1} = \frac{v_{in}(t) \times D_{aux} \times T_{sw}}{L_{a1}} \qquad (13)$$

Mode 2a [ta1-ta2]: At this mode, Cr1 and La1 start a resonance. At the end of this mode La1 current reaches zero and Cr1 voltage becomes maximum. At this moment, switch S1 current is zero and can be turned off under ZCS. Then, iLa becomes negative and continues resonance with Cr1 and Lm1. The next three operation modes are similar to the modes 2, 3 and 4.

$$i_{La}(t) = \frac{v_{in}(t)}{Z_1}\sin(\omega_1(t - t_{a1})) + I_{a1}\cos(\omega_1(t - t_{a1})) \qquad (14)$$

$$I_{a2} = \frac{v_{in}(t)}{\sqrt{2}}\left(\frac{1}{Z_1} + \frac{D_{aux}}{f_{sw} \times L_{a1}}\right) \qquad (15)$$

$$t_{a2} - t_{a1} = \frac{1}{\omega_1} \times \left[\pi - \arctan\left(\frac{D_{aux} \times \omega_1}{f_{sw}}\right)\right] \qquad (16)$$

III. DESIGN PROCEDURE

In order to extract equations, it is convenient to define PFC gain and inductors ratio as $G = Vo1\ Vin$ and $K = Lm1\ La1$ respectively. According to description in the mode 1 and section III-D, iLa and iLm should meet each other at 5 8 $T1$ to ensure S1 can be turned off under zero current. By equating (1) and (2) in 5 8 $T1$, K can be defined by PFC gain (G)

$$K = \frac{5\pi\sqrt{2}}{4}(1 - G) \qquad (17)$$

A. Calculating input and output power

According to Fig. 3 (a), input current is equal to average of main switch current over one switching period. Also, switch S1 only conducts during first mode. Therefore, by integrating $i(t)$ over the first mode ($t1 - t0$ = 5 8 $T1$), $isw,avg(t)$ can be determined.

$$i_{sw,avg}(t) = \frac{1}{T_{sw}}\left(\int_0^{\frac{5}{8}T_1} i_{La}(t)dt + \int_0^{\frac{5}{8}T_1} i_{Lm}(t)dt\right) \qquad (18)$$

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By performing the integral, isw,avg(t) can be represented as follow

$$i_{sw,avg}(t) = v_{in}(t) \times C_{r1} \times f_{SW} \left[\frac{7.11 \times (1-G)}{K} + 1.707 \right] \quad (19)$$

The instantaneous input voltage, input current and input power are given by (20)-(22), respectively

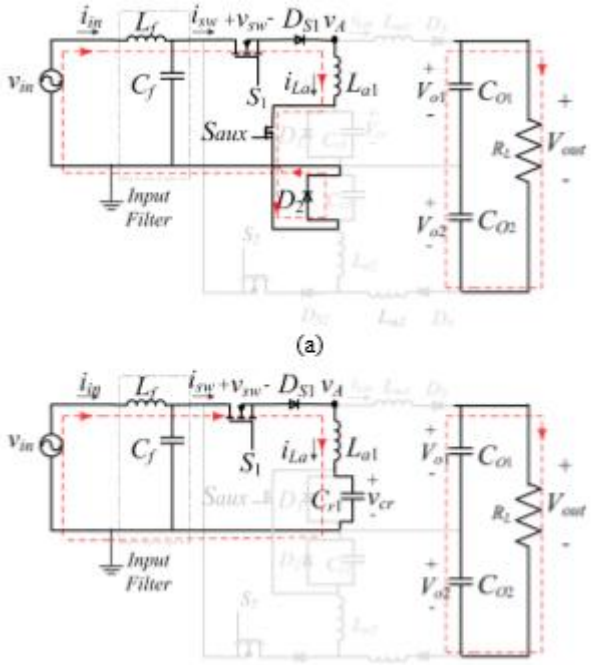

Fig. 5. Equivalent circuits of modes in vin(t)<Vo1 . (a)Mode 1a. (b)Mode 2a

$$v_{in}(t) = \sqrt{2} \times V_{in,rms} \times sin(\omega t) \quad (20)$$

$$i_{in}(t) = \sqrt{2} \times I_{in,rms} \times sin(\omega t) \quad (21)$$

$$p_{in}(t) = v_{in}(t) \times i_{in}(t) = 2 \times V_{in,rms} \times I_{in,rms} \times sin^2(\omega t) = P_{in,max} \times sin^2(\omega t) \quad (22)$$

Therefore, by using (17), (19) and (22), the instantaneous input power can be represented in (23)

$$p_{in}(t) \cong 3.09 \times C_{r1} \times v_{in}^{\ 2}(t) \times f_{sw} \quad (23)$$

If dead angle is eliminated completely, the average of output power can be equal to (24), where η is converter efficiency.

$$P_{o,avg} = 0.5 \times \eta \times P_{in,max} \quad (24)$$

B. Design of Cr1 In PFC converter, input voltage and current are sinusoidal waveforms and their values vary between zero and their maximum amplitude that lead to change in instantaneous amplitude of input power. Therefore, according to (23), the resonant capacitor (Cr1) should have capability of transferring maximum input power. Furthermore, operating under maximum switching frequency ensures that there is no dead time in the switching period and subsequently, the maximum power is being transferring to the load. So, according to these assumptions, Cr1 should be determined in maximum input power and switching frequency. Cr1 can be calculated as follow:

$$C_{r1} = \frac{P_{in,max}}{3.09 \ V_{in,max}^{\ 2} \ f_{sw,max}} \quad (25)$$

C. Design of La1 and K In order to design La1, sum of the modes 1, 2 and 3 durations should be less than 1 fsw, to ensure that converter will not operate in continuous conduction mode (CCM). Therefore, La1 should be small enough to force PFC to work in DCM condition. Note that Safety factor (SF) is used in (26) to guarantee that proposed PFC will not operate in boundary conduction mode

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$$L_{a1} \le \frac{[1+\frac{4\times\sqrt{1+K}}{5}+(1+\frac{1}{K})\times(\frac{1}{G}-1)]^{-2}}{C_{r1}\times(1.25\pi\times SF\times f_{sw,max})^2} \qquad (26)$$

MATLAB solution of (26) shows that La1 is minimum only when input voltage is maximum. Subsequently, K is designed for maximum input voltage too.

D. Maximum and Minimum main switches duty cycle According to first mode, in order to achieve zero current switching for main switch, iLa and iLm must meet each other at the time $t1 \leqslant 3\ 4\ T1$ (iLa reaches its maximum negative value at $t1 = 3\ 4\ T1$). Otherwise, amplitude of iLa decreases and they will not meet each other at all. However, lower t1, results in reduced duration of the first mode and causes extra switch peak current. Therefore, duration of this mode should be considered almost equal to $3\ 4\ T1$. Thus, the control unit should turn main switches off after $5\ 8\ T1$ and less than $3\ 4\ T1$. When switch current in the first mode reaches zero, DS1 becomes reverse biased and node "A" voltage reaches its maximum value (VA,max> vin(t)) and then its voltage reduces to vin(t) . Then diode DS1 becomes forward biased and S1 current begins to rise again and S1 cannot be turned off under ZCS. Therefore, the maximum allowable time that control circuits can keep S1 on should be calculated. Based on Fig. 3, node "A" voltage is as following when switch current is zero

$$v_A(t) = v_{cr} - (\frac{v_{cr}-V_{o1}}{L_{a1}+L_{m1}}\times L_{a1}) \qquad (27)$$

The switch should be turned off before vA reaches vin(t). By solving (27) in MATLAB software, it is concluded when input voltage is in its maximum value, vA reaches vin(t) faster and proper duration for switch on time becomes minimum. Therefore, the maximum allowable on time duration to guarantee ZCS must be calculated for Vin,max. Thus, by replacing Vin,max in vcr and equating (27) to Vin,max , the maximum period that control circuit is allowed to keeps S1 on, will be achieved. E. Auxiliary switch duty cycle It is noteworthy to say that in order to increase PF, the input current should not change abruptly when input voltage becomes larger than half of the output voltage. The phase angle

where input voltage becomes higher than half of z$Vo1$ Vin,x . In order to achieve pure sinusoidal input current, amplitude of input current at this point should be equal to $Iin,max \times \sin\theta$, where $Iin,max = Pin,maxVin,max$. In order to simplify

calculations, switch current waveform which is shown in Fig. 4 can be approximated by waveform in Fig. 6. Also, it is assumed that Δta is equal to 0.25T1. Therefore, iin(t) and isw,avg(t) are calculated as follow

$$i_{in}(t) = i_{sw,avg}(t) = \frac{D_{aux}^2\times v_{in}(t)}{2\times L_{a1}\times f_{sw}} + 0.125\times v_{in}(t)\times T_1\times f_{sw}\times(I_{a2}+\frac{D_{aux}}{L_{a1}\times f_{sw}})+$$

$$0.5\times v_{in}(t)\times I_{a2}\times f_{sw}\times[\frac{1}{\omega_1}\times(\pi-\arctan(\frac{D_{aux}\times\omega_1}{f_{sw}}))-0.25\times T_1] \qquad (28)$$

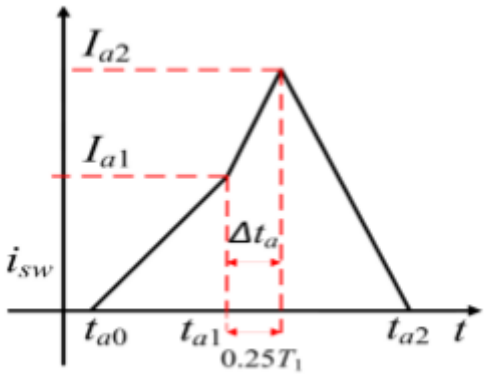

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TABLE I
design parameters of the PFC

Symbol	Parameter
L_f & C_f	2mH & 230nF
L_{a1}~L_{a2}	1.9 µH
L_{m1}~L_{m2}	8.85 µH
C_{r1}~C_{r2}	36 nF
C_{o1}~C_{o2}	4.7 mF
D_1~D_2	MUR860
D_3~D_4	BYV32-200
S_1~S_2	IRFP260
D_{S1}~D_{S2}	BYV32-200
S_{aux}	IRF740

F. Maximum voltage and current stress of semiconductor devices Since the minimum voltage of resonant capacitor is zero, the main switches voltage stress is clamped to input voltage and voltage stress of diodes D3 and D4 are clamped to 0.5Vout. The voltage stress of auxiliary switch, D1 and D2 are equal to peak voltage of resonant capacitors which occurs at the maximum input voltage which is almost equal to 2Vin,max.. In the first mode, sum of La1 and Lm1 currents run through main switch. Thus, according to equation (1) and[i] (2), maximum current stress of main switch is ($in,maxZ1 + Vin,max-0.5VoutLm1 \times 0.5T1$)

IV. EXPERIMENTAL RESULTS

A laboratory prototype of the proposed type 1 PFC (Vin=110Vrms & 50Hz, fsw=100kHz, Vout =48V, Pout=120W) is designed and implemented to verify validity of theoretical analysis. The components of the prototype are presented in Table I. In order to increase efficiency, IGBTs with reverse blocking capability (RB-IGBT) can be employed as main switches [8], [21] and [32] for high voltage applications. In the proposed prototype converter, MOSFET switch with a series diode is used since the input voltage is low. In low voltage applications, usually a series combination of MOSFET and a diode has lower conduction voltage than a RB-IGBT switch. However, at high input voltage applications, since the conduction voltage of high voltage diodes are relatively large and also the drain-source on resistance of high voltage MOSFET switches are high, RBIGBT is a better choice. The proposed PFC converter is compared with exiting PFCs in Table II. Note that, in [8], [9], and [21] semiconductor devices are turned on or off under hard switching conditions. Therefore, their soft switching conditions are illustrated as partial in Table II. The total price of proposed converter and converter of [21] are slightly higher due to applying three switches for proposed converters and semiconductors devices with high voltage rating for converter of [21]. In addition, PSPICE simulations are performed for the proposed PFC and PFCs in [8]-[9] and [21] and efficiency results are reported in the Table II. Introduced PFCs in [8] and [9] are less expensive than proposed type 1 PFC but their efficiency and THD are not desirable.

TABLE II
Comparison of the proposed PFC and the other topologies using PSPICE simulation results.

Item		Type 1	[8]	[9]	[21]
No.of main switch		2 (IRFP260)	2 (IRFP260)	2 (IRFP460)	2 (IRFP460)
No.of auxiliary switch		1 (IRF740)	0 -	0 -	0 -
No.of Diode		6	4	3	5
No.of Magnetic Element		4	2	1	3
No.of conducting simultaneously semiconductor devices	Switch on	2	2	2	3
	Switch off	1	1	1	1
Soft switching Condition		Full	Partial	Partial	Partial
Zero crossing dead angle		No	Yes	No	Yes
Cost/Power		Medium	Low	Low	Medium
Full Load Efficiency (%)		92.7	89.1	90.9	90

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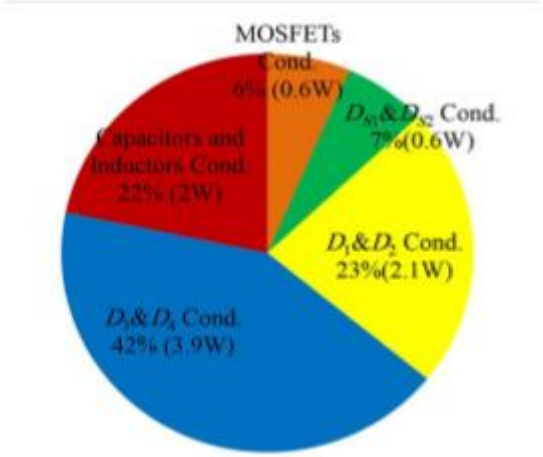

It can be observed from Fig. 7(a) the measured harmonic contents of the input current for various input voltage up to 19th harmonic are well below IEC61000-3-2 Class D limits. As shown in Fig. 7(b), even at 25% nominal load, the efficiency of the proposed converter varies about only 1% that makes the proposed PFC appropriate for applying in electronic devices. Fig. 8 reports the conduction losses of MOSFETs, diodes DS1~DS2, diodes D1~D4 and capacitors and inductors. The Simulation and experimental results and datasheet parameters of elements are used to calculate the losses breakdown. A photo of laboratory prototype of the proposed PFC is provided in Fig. 9 .The experimental waveforms of the input voltage, input current and FFT of input current with series filter are shown in Fig. 10. In Fig. 10(a), the dead angle of the input current is clearly visible, when auxiliary switch is off. However, in Fig. 10(b), auxiliary switch operates during dead angle interval and regulates input current. It is obvious that the dead angle is omitted and the input current shape is perfectly sinusoidal and is in phase with input voltage. In Fig. 10(c), waveforms of input voltage and current at light load are depicted. It shows that proposed PFC can draw sinusoidal current even at light load condition. In Fig. 10(d), the measured input

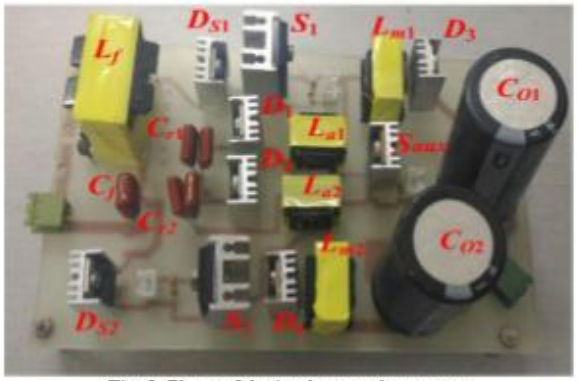

Fig. 9. Photo of the implemented prototype

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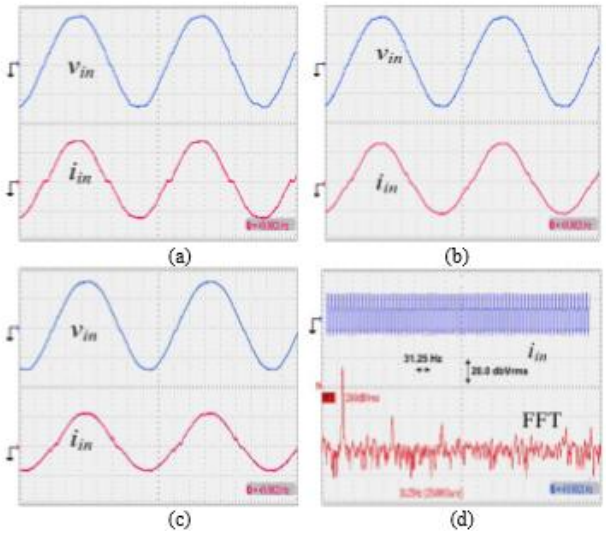

Fig.10. Experimental waveforms of input voltage, input current and FFT (with series filter). (a) Input voltage and current at full load without using auxiliary switch. From top to bottom: vin (100V/div),iin (1.3A/div), (time 2.5ms/div). (b)Input voltage and current at full load by using auxiliary switch. From top to bottom: vin (100V/div), iin (1.3A/div), (time 2.5ms/div). (c) Input voltage and current at light load (30% of nominal load) by using auxiliary switch From top to bottom: vin (100V/div), iin (0.5A/div), (time 2.5ms/div). (d) Input current harmonics at full load

current harmonics are reported. Also, the experimental waveforms of the input voltage and input current without series filter are shown in Fig. 11. Vo1, Vo2 and output voltage are shown in Fig. 12. As can be observed, one of the capacitors is discharged in positive half-line cycle and the other one discharged in negative half-line cycle. Thus, low frequency ripple of Co1 and Co2 cancel each other and Vo ripple which of sum of Vo1 and Vo2 is very low. Fig. 13(a) demonstrates the drain-source voltage, gate-source voltage and current waveforms of the switch S1. It is clear that switches and diodes are turned on and off under ZCS conditions which reduce switching losses and thus efficiency is improved. In addition, the adverse effects of diode reverse recovery in conventional converters are resolved. In Fig. 13(b), the drain-source voltage, gate-source voltage and current waveforms of the auxiliary switch is shown, which confirms that Saux is turned on under ZVS and turned off under almost ZVS condition. In Fig. 14 waveforms of iLa, iLm and vcr are provided.

V. CONCLUSION

A soft switching step-down bridgeless PFC converter has been proposed in this paper. Employing an auxiliary switch which operates under ZVS, the dead angle in the input is omitted and PF is improved. The proposed PFC reduces switching losses by providing ZCS condition for main switches and diodes without using any auxiliary circuits. Also, the number of semiconductors in power flow path is minimized. Both of these features result in improved efficiency. The experimental results verify that soft

switching condition is achieved for all semiconductors and dead angle is omitted. Also, efficiency of 92.1% and THD of 3.3% at 110 Vrms input and 120 W output power are achieved. The improvement on the efficiency of proposed PFC can be justified by the fact that the number of semiconductors in power flow path and switching and reverse recovery losses of diodes are minimized. Also, the proposed PFC can improve THD significantly even at low input voltages.

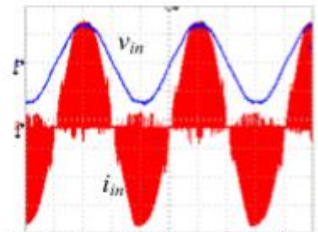

Fig. 11. Experimental waveforms of input voltage and input current (without series filter).From top to bottom: v_{in} (100V/div),i_{in} (10A/div), (time 5ms/div)

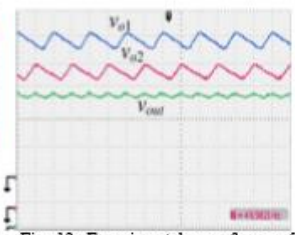

Fig. 12. Experimental waveforms of output voltages. From top to bottom: v_{o1} (5V/div), v_{o2} (5V/div), v_{out} (10V/div) (time 10ms/div)

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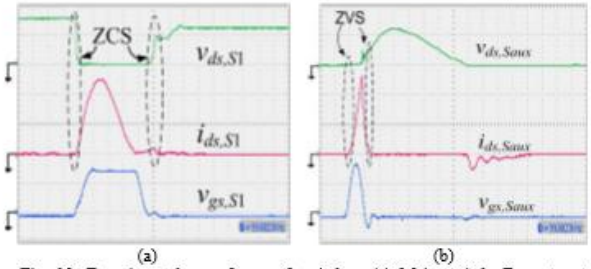
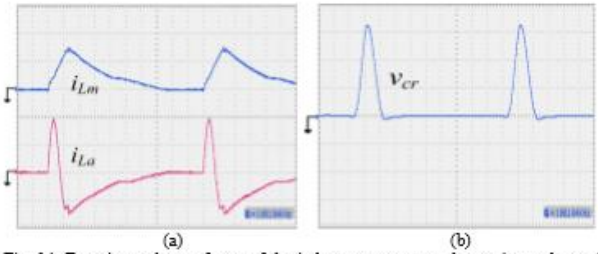


(a) (b)

Fig. 13. Experimental waveforms of switches. (a) Main switch, From top to bottom: $v_{ds,S1}$ (100V/div),$i_{ds,S1}$ (12A/div) $v_{gs,S1}$ (10V/div), (time 250ns/div), for V_{in} =150V. (b) Auxiliary switch, From top to bottom: $v_{ds,Saux}$ (50V/div), $i_{ds,Saux}$ (1A/div) ,$v_{gs,Saux}$ (10V/div), (time 250ns/div) for V_{in} =24V.



(a) (b)

Fig. 14. Experimental waveforms of the inductors currents and capacitor voltage. (a) From top to bottom: L_{m1} current (12A/div),L_{o1} current (12A/div) , (time 1μs/div), (b) C_{r1} voltage (100V/div), (time 1μs/div), for V_{in}=150V.

REFERENCES

[1] California Energy Commission (CEC). (2005). Code of Conduct on Energy Efficiency of External Power Supplies [Online]. Available: http://www.energy.ca.gov/papers/2005-03-03_WILSON.PDF

[2] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," IEEE J Emerg Sel Top Power Electron, vol. 4, no. 3, pp. 799–807, 2016..

[3] H. Ma, J. J. Lai, C. Zheng, and P. Sun, "A High-Efficiency QuasiSingle-Stage Bridgeless Electrolytic Capacitor-Free High-Power AC– DC Driver for Supplying Multiple LED Strings in Parallel," IEEE Trans Power Electron, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.

[4] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," IEEE Trans Power Electron, vol. 25, no. 6, pp. 1406–1415, 2010.

[5] M. H. Rashid, Power Electronics Handbook: Devices Circuits and Applications. New York, NY, USA:Academic, 2010.

[6] X. Wu, J. Yang, J. Zhang, M. Xu, and S. Member, "Design Considerations of Soft-Switched Buck PFC Converter With Constant On-Time (COT) Control," IEEE Trans POWER Electron, vol. 26, no. 11, pp. 3144–3152, 2011.

[7] X. Wu, J. Yang, J. Zhang, and Z. Qian, "Variable On-Time (VOT)Controlled Critical Conduction Mode Buck PFC Converter for HighInput AC/DC HB-LED Lighting Applications," IEEE Trans Power Electron, vol. 27, no. 11, pp. 4530–4539, Nov. 2012.

[8] Y. Jang, Yungtaek Jang, and M. M. Jovanović, "Bridgeless HighPower-Factor Buck Converter," IEEE Trans Power Electron, vol. 26, no. 2, pp. 602–611, Feb. 2011.

[9] M. Malekanehrad and E. Adib, "Bridgeless single-phase step-down PFC converter," IET Power Electron, vol. 9, no. 14, pp. 2631–2636, Nov. 2016.

[10] X. Xie, C. Zhao, L. Zheng, and S. Liu, "An Improved Buck PFC Converter With High Power Factor," IEEE Trans Power Electron, vol. 28, no. 5, pp. 2277–2284, May 2013.

[11] X. Xie, C. Zhao, Q. Lu, and S. Liu, "A Novel Integrated Buck-Flyback Nonisolated PFC Converter With High Power Factor," IEEE Trans Ind Electron, vol. 60, no. 12, pp. 5603–5612, Dec. 2013.

[12] J. Zhang, C. Zhao, S. Zhao, and X. Wu, "A Family of Single-Phase Hybrid Step-Down PFC Converters," IEEE Trans Power Electron, vol. 8993, no. c, pp. 1–1, 2016.

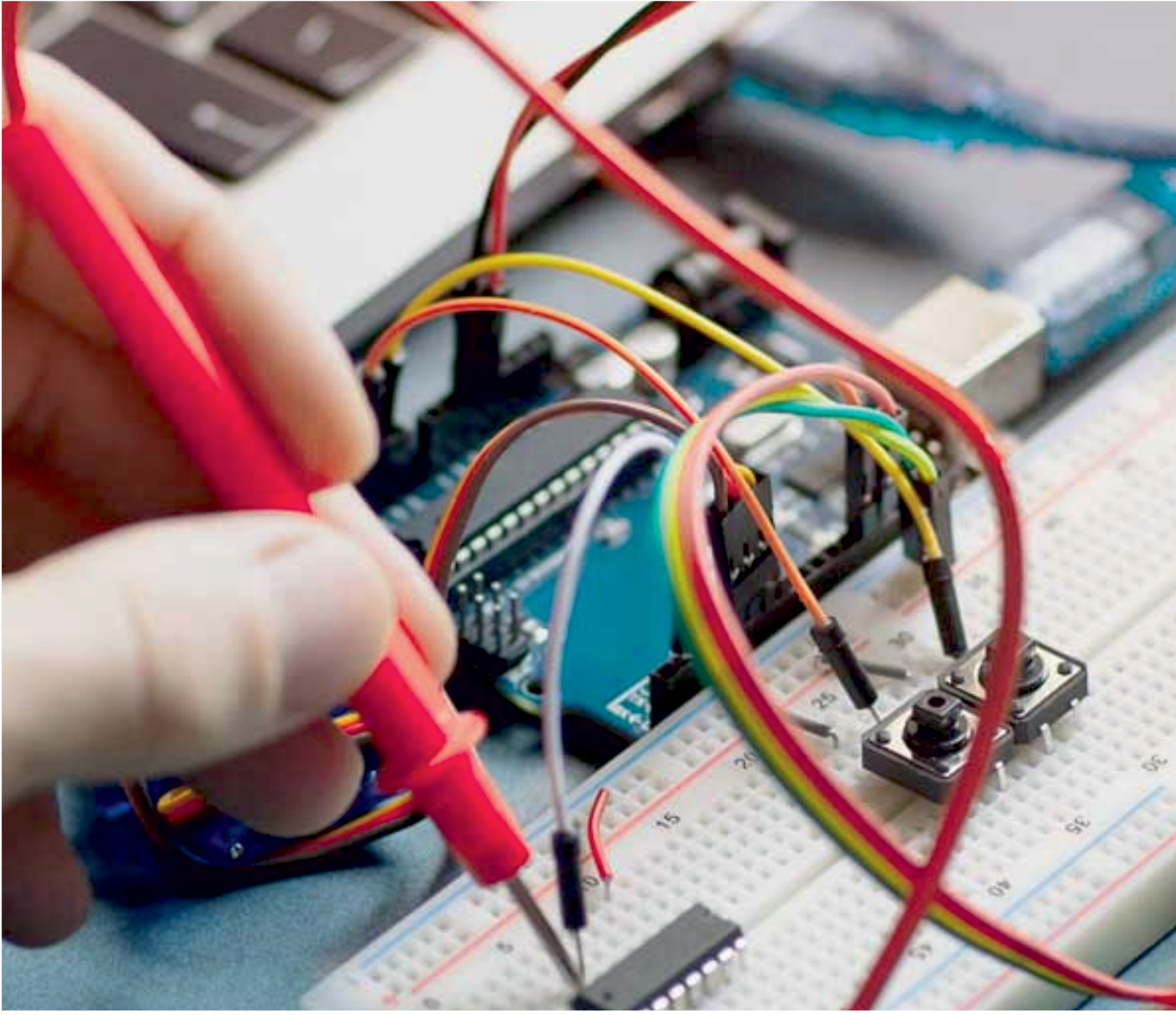
[13] G. Spiazzi and S. Buso, "Power factor preregulators based on combined buck-flyback topologies," IEEE Trans Power Electron, vol. 15, no. 2, pp. 197–204, Mar. 2000.

[14]X. Xie, J. Li, K. Peng, C. Zhao, and Q. Lu, "Study on the Single-Stage Forward-Flyback PFC Converter With QR Control," IEEE Trans Power Electron, vol. 31, no. 1, pp. 430–442, Jan. 2016.

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.122|

|| Volume 9, Issue 9, September 2020 ||

[15]M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," IEEE Trans Ind Electron, vol. 58, no. 9, pp. 4153–4160, 2011.
[16]H. Farzaneh-Fard and M. Mahdavi, "Bridgeless CUK power factor correction rectifier with reduced conduction losses," IET Power Electron, vol. 5, no. 9, pp. 1733–1740, 2012.
[17]A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses," IEEE Trans Ind Appl, vol. 47, no. 2, pp. 873– 881, Mar. 2011
[18]A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless cuk rectifiers for PFC applications," IEEE Trans Power Electron, vol. 27, no. 7, pp. 3292–3301, 2012.
[19]J. Yang and H. Do, "Bridgeless SEPIC Converter With a Ripple-Free Input Current," IEEE Trans Power Electron, vol. 28, no. 7, pp. 3388– 3394, Jul. 2013.
[20]H.-T. Yang, H.-W. Chiang, and C.-Y. Chen, "Implementation of Bridgeless Cuk Power Factor Corrector With Positive Output Voltage," IEEE Trans Ind Appl, vol. 51, no. 4, pp. 3325–3333, Jul. 2015.
[21]A. A. Fardoun, E. H. Ismail, N. M. Khraim, A. J. Sabzali, and M. A. Al-Saffar, "Bridgeless high-power-factor buck-converter operating in discontinuous capacitor voltage mode," IEEE Trans Ind Appl, vol. 50, no. 5, pp. 3457–3467, 2014.
[22]J. Shin, S. Choi, and B. Cho, "High-Efficiency Bridgeless Flyback Rectifier with Bidirectional Switch and Dual Output Windings," IEEE Trans Power Electron, vol. 29, no. 9, pp. 4752–4762, Sep. 2014.
[23]M. Mahdavi and H. Farzanehfard, "Zero-current-transition bridgeless PFC without extra voltage and current stress," IEEE Trans Ind Electron, vol. 56, no. 7, pp. 2540–2547, 2009.
[24]M. Alam, W. Eberle, D. S. Gautam, and C. Botting, "A Soft-Switching Bridgeless AC–DC Power Factor Correction Converter," IEEE Trans Power Electron, vol. 32, no. 10, pp. 7716–7726, Oct. 2017.
[25]M. R. Amini, H. Farzanehfard, A. Emrani, and M. Mahdavi, "Soft switching bridgeless power factor correction with reduced conduction losses and no stresses," IET Power Electron, vol. 5, no. 3, pp. 334–340, 2012.
[26]M. Ramezani and S. M. Madani, "New zero-voltage-switching bridgeless PFC, using an improved auxiliary circuit," IET Power Electron, vol. 4, no. 6, p. 732, 2011.
[27]C.-C. Hua, Y.-H. Fang, and C.-H. Huang, "Zero-voltage-transition bridgeless power factor correction rectifier with soft-switched auxiliary circuit," IET Power Electron, vol. 9, no. 3, pp. 546–552, 2016.
[28]H. Y. Tsai, T. H. Hsia, and D. Chen, "A family of zero-voltagetransition bridgeless power-factor-correction circuits with a zerocurrent-switching auxiliary switch," IEEE Trans Ind Electron, vol. 58, no. 5, pp. 1848–1855, 2011.
[29] I. D. Kim, E. C. Nho, S. H. Choi, and J. S. Lai, "A simple ZVT PWM single-phase rectifier with reduced conduction loss and unity power factor," J. Power Electron., vol. 7, no. 1, pp. 55–63, 2007.
[30]M. Mahdavi and H. FarzanehFard, "Zero-voltage transition bridgeless single-ended primary inductance converter power factor correction rectifier," IET Power Electron, vol. 7, no. 4, pp. 895–902, Apr. 2014.
[31]H. Farzanehfard and M. Reza Amini, "Switched resonator DC/DC converter with a single switch and small inductors," IET Power Electron, vol. 7, no. 6, pp. 1331–1339, Jun. 2014.
[32]B. Zhao, A. Abramovitz, and K. Smedley, "Family of Bridgeless BuckBoost PFC Rectifiers," IEEE Trans Power Electron, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.



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