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Analysis of Transistor-Clamped H-Bridge Multilevel Inverter

Nisha Parveen[1], Rishabh Shukla[2]

Research Scholar, Dept. of EX, OCT, Bhopal, India[1]

Professor, Dept. of EX, OCT, Bhopal, India[2]

ABSTRACT*:* Multilevel inverter offer high force capacity, coming about with lower yield harmonics. Their primary hindrance is their unpredictability, requiring an extraordinary number of intensity devices, and complex hardware. This paper presents another topology of the multilevel inverter with including voltage boosting. The proposed multilevel inverter utilizes transistor clamped MLI. An epic all inclusive control plot is utilized which brings about adjusted dispersion of intensity among H-connect cells. This control plan can likewise be utilized for the accuse balance control of various information DC sources in some random fashion. The examination of the voltage harmonic is done in comparison to existing methods.

KEYWORDS: Multilevel inverter, cascaded H-bridge, multicarrier phase width modulation, Transistor clamped inverter, cascaded neutral –point clamped inverter.

I. INTRODUCTION

There are different application changing from medium voltage to high voltage high force application which expects DC to AC transformation utilizing multilevel inverters. The exploration on multilevel inverter is continuous further to decrease the quantity of switching devices to diminish the assembling cost, capacitor voltage adjusting .The inverters with number of voltage levels equivalent to three or above than that are known as the multilevel inverters. Multilevel inverters are fit for delivering high force high voltage as the interesting structure of the staggered voltage source inverter permits to arrive at high voltages with low harmonics the utilization of transformers or arrangement associated synchronized switching devices. As the quantity of voltage levels increments , the consonant substance of the yield voltage waveform diminishes [1].

There are three major multilevel voltage source inverter topologies neutral-point lamped inverter (i.e diode clamped) , flying capacitor (capacitor-clamped) and cascaded H-bridge multilevel inverter . There are also various other topologies which have been proposed and have successfully adopted in various industrial applications. The novel universal multi-carrier PWM control scheme is used .This paper mainly focuses mainly on the cascaded H-bridge inverter topology. the cascaded multilevel inverter has the potential to be the most reliable out of three topologies . It has the best fault tolerance owing to its modularity a feature that enables the inverter to continue operate at lower power levels after cells failure[29]-[31]. Due to the modularity of the cascaded multilevel inverter it can be stacked easily for high power and high voltage applications. The cascaded multilevel inverter mainly consists of several identical H-bridge cells which are cascaded in series from the output side. The cascaded H-bridge (CHB) may further be classified as symmetrical if the DC bus voltage is equal in all the series power cells and as asymmetrical if the DC bus voltage is not same for each power cell. The symmetrical CHB is more advantageous over the asymmetrical CHB in terms of modularity , maintenance and cost. In case of the asymmetrical CHB DC bus voltage is varied in each power as per the requirement to increase the voltage levels [2],[32]. In case of the symmetrical CHB the voltage level can be increased without varying the DC voltage with same number of power cells. The transistor clamped topology is popular now a days a provides provision to increase the output levels by taking different voltage levels from the series stacked capacitors [12],[33]. In this paper the new configuration of the symmetrical H-bridge is proposed which produces a five-level output voltage similar to conventional transistor clamped topology. instead of three-level as in case of conventional H-bridge. But this new proposed topology produces the boost output voltage in comparison to conventional transistor clamped topology which also produces the five-level output but the output voltage equal to the DC voltage .

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II. CONFIGURATION OF INVERTER

The configuration of conventional cascaded H-bridge inverter consists of DC voltage for each H-bridge and only four switching devices. The value of the DC voltage in each bridge depends whether the configuration is symmetric or unsymmetric. Fig.1 shows the conventional H-bridge. The general configuration of the proposed inverter topology is shown in fig.2 which represents a single cell which produces the five-level output with boost output voltage. It consist of total of 8 switches in a single cell along with an additional bidirectional switch consisting of S11 and S11' which is connected between the first leg of the H-bridge and the capacitor midpoint, enabling five output voltage levels (+2Vdc , +Vdc , 0 , -Vdc , -2Vdc) based on the switching combination . The switches S21,S31,S41,S51 forms the H-bridge and the switches Sa1,Sa2,Sa3,Sa4 are connected in the same leg which plays a role in boosting the voltage and the input DC voltage is connected with positive terminal between the switches Sa1 and Sa2 and the negative terminal between the switches Sa3 and Sa4. The capacitor voltage divider is formed by C1 and C2.

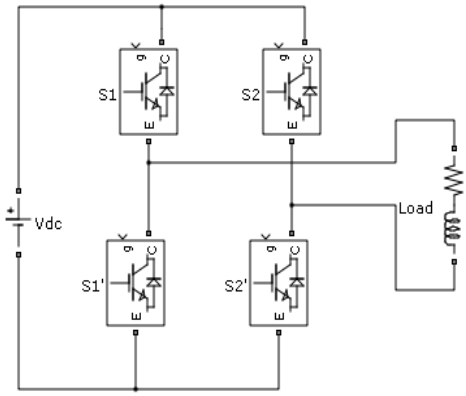

Fig.1 Conventional cascaded H-bridge

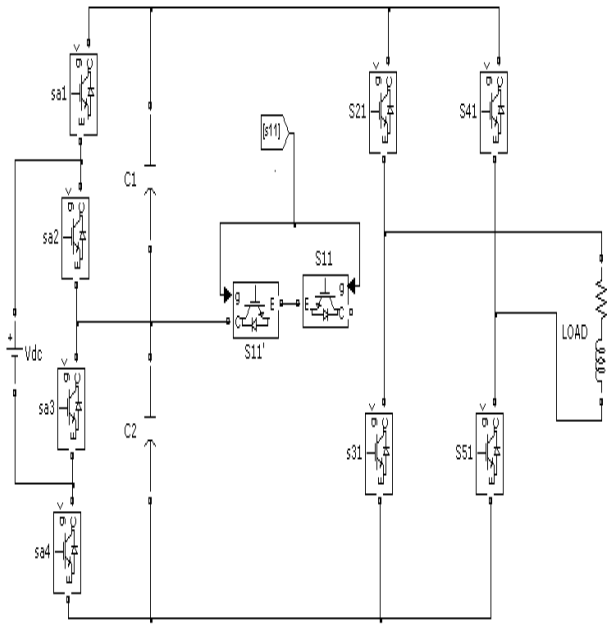

Fig. 2Topology of five-level transistor clamped H-bridge with boost output voltage for each cell

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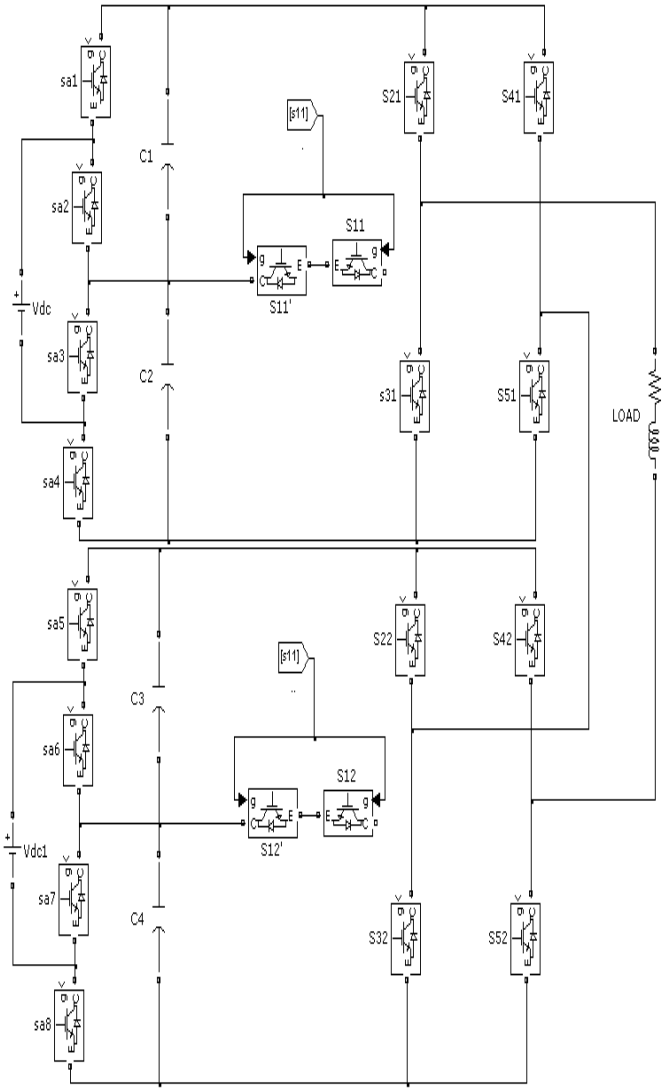

Fig.3 Configuration of the proposed 1-phase transistor clamped cascaded H-bridge inverter using two cells

III. OPERATION OF PROPOSED INVERTER TOPOLOGY

The working of the single cell of the proposed inverter topology is explained telling how the required five level output is produced :

1. Maximum positive output that can be produced is the double of the input DC voltage i.e 2Vdc which is produced when S21 is on connecting the load positive terminal to the load and S51 is on connecting the load negative terminal to the Vdc thus the total output voltage is 2Vdc. The output voltage level Vdc is obtained when Sa1 , S11 , S51 and Sa2 gets turned on other switches remaining off.
2. Maximum negative output is -2Vdc which is produced when switches S41 and S31 gets turned on connecting the negative and positive terminal of the load respectively to the input source. The negative level –Vdc is obtained when switches Sa1 , Sa3 , S11 , S41 are turned on other switches remaining off.

The detailed operation of the proposed topology can also be understand through the look up table . In the look up table 0 and 1 values are assigned to the switches for a particular voltage level. At any level of the output voltage the switches

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which are having value 1 means they are in the ON state at that time and the remaining switches with the zero value are in the OFF state at the same instant of time. The look up table for the proposed inverter is given in the figure given below.

Voltage level	+2Vdc	+Vdc	0	-Vdc	-2Vdc
Sa1	0	0	0	1	0
Sa2	0	1	0	0	0
Sa3	0	0	0	1	0
Sa4	0	1	0	0	0
S11	0	1	0	1	0
S21	1	0	1	0	0
S31	0	0	0	0	1
S41	0	0	1	1	1
S51	1	1	0	0	0

Table.1 Look up table for the proposed TCHB

Voltage level	+4V	+3V	+2V	+1V	0V	-1V	-2V	-3V	-4V
Sa1	0	0	0	0	0	1	1	0	0
Sa2	0	0	1	1	0	0	0	0	0
Sa3	0	0	0	0	0	1	1	0	0
Sa4	0	0	1	1	0	0	0	0	0
S11	0	0	1	1	0	1	1	0	0
S21	1	1	0	0	1	0	0	0	0
S31	0	0	0	0	0	0	0	1	1
S41	0	0	0	0	1	1	1	1	1
S51	1	1	1	1	0	0	0	0	0
Sb1	0	0	0	0	0	0	1	1	0
Sb2	0	1	1	0	0	0	0	0	0
Sb3	0	0	0	0	0	0	1	1	0
Sb4	0	1	1	0	0	0	0	0	0
S12	0	1	0	0	0	0	1	1	0
S22	1	0	1	1	1	1	0	0	0
S32	0	0	0	0	0	0	0	0	1
S42	0	0	0	1	1	1	1	1	1
S52	1	1	1	0	0	0	0	0	0

Table.2 Lookup table for single phase proposed transistor clamped H-bridge inverter

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IV. CONTROL SCHEME

Multilevel inverter has to synthesize a staircase waveform by using the modulation technique to have the controlled output voltage. There are variety of modulation techniques available. Basically the control technique can be classified as the pulse width modulation which is considered as the most efficient method. This PWM is further divided into various PWM techniques such as single pulse PWM, space vector PWM, multiple pulse PWM, phase displacement control. For this proposed topology we are using the multicarrier based control technique which can be applied to all the topologies of the multilevel inverter. For any given number of levels in the output voltage the number of carrier to be used is given as N-1
Where N is the number of levels in the output voltage. Simply a reference signal is taken which is a sinusoidal signal of 50Hz frequency and this reference is compared with the carrier signal which are the triangular wave .The modulation index we are

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using in this modulation technique is 0.95.The advantage of this scheme is that it offers the charge balance control in the input DC sources and voltage across the capacitor are also balanced.

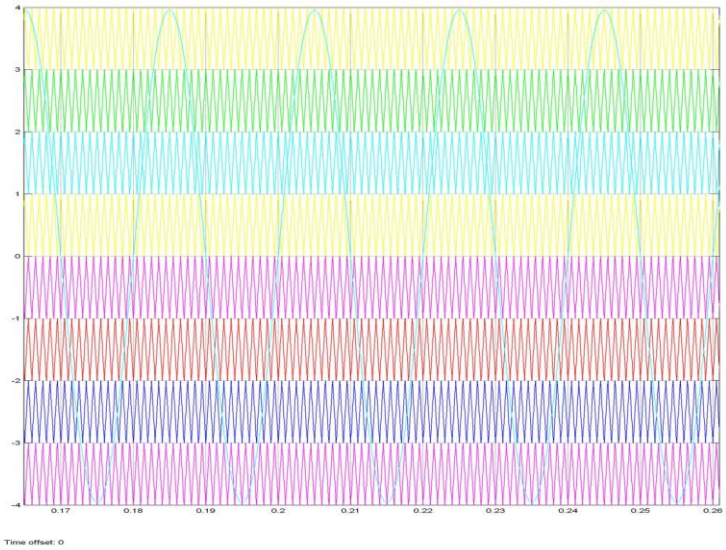

Fig.5 Multicarrier based control scheme for the proposed topology

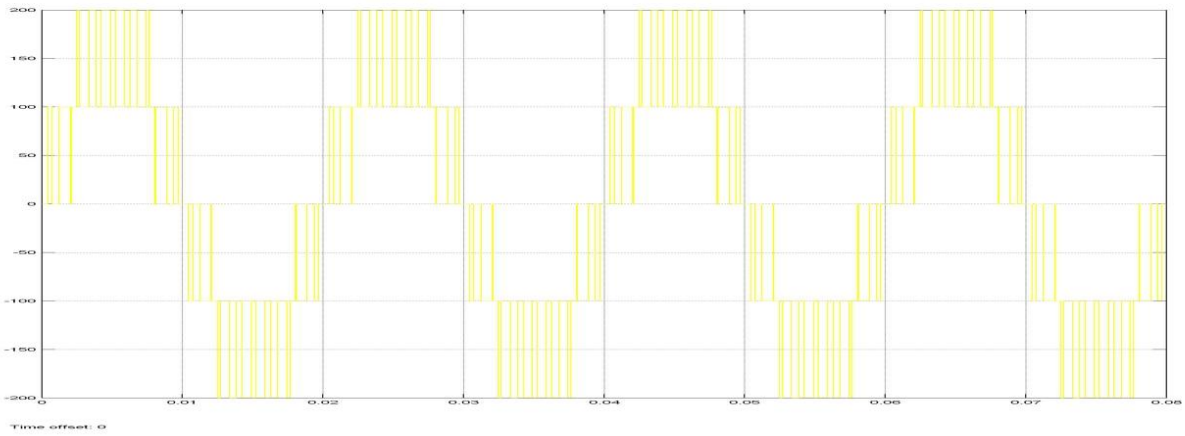

Fig.4 5-level output voltage waveform of single phase cascaded H-bridge inverter with two bridges

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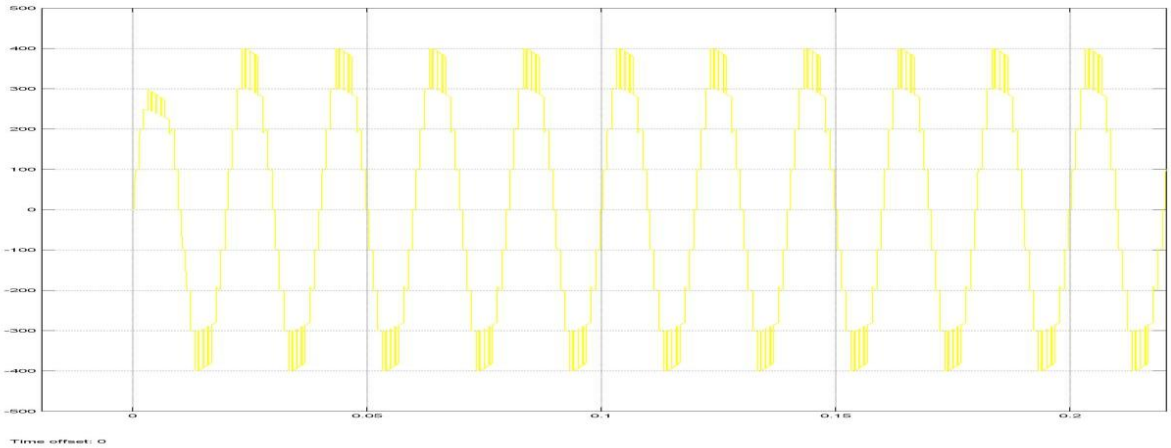

Fig.5 9-level output voltage waveform of single phase proposed transistor clamped H-bridge inverter with two bridge

V. COMPARISON OF PROPOSED TOPOLOGY WITH CASCADED H-BRIDGE TOPOLOGY

The purpose of research for the multilevel inverter includes to get a quality power output with the reduced number of switching devices, balancing of the capacitors, reduced number of clamping diodes in order to reduce the overall cost of the multilevel inverter. In the proposed multilevel inverter topology the number of switches are more in comparison to the conventional CHB but we get the five-level in the output voltage which results in reduced THD. Also the input DC voltage source required is half of the voltage source required in the conventional CHB. much superior than the cascaded H-bridge topology in terms of the number of level in the output voltage, magnitude of the output voltage, total harmonic distortion. To produce the same output voltage the cascaded H-bridge has to use the two cells where as only one cell is required with the proposed topology. Fig.3 is showing the single phase inverter consisting of two cells of the proposed topology each cell is having input 100V DC voltage and the output ac voltage is 400V each of which is producing 200V. The total harmonic distortion produced by the proposed inverter is 11.49% only which is very low as compared to the conventional cascaded H-bridge inverter having THD of 37.64% which is 26.15% more than the proposed topology. In order to produce the nine levels in the output voltage the cascaded H-bridge requires three cells where as the proposed topology requires only two cells . Apart from the advantages the only disadvantage of this proposed topology is that it uses the more number of switching devices in comparison to cascaded H-bridge topology.

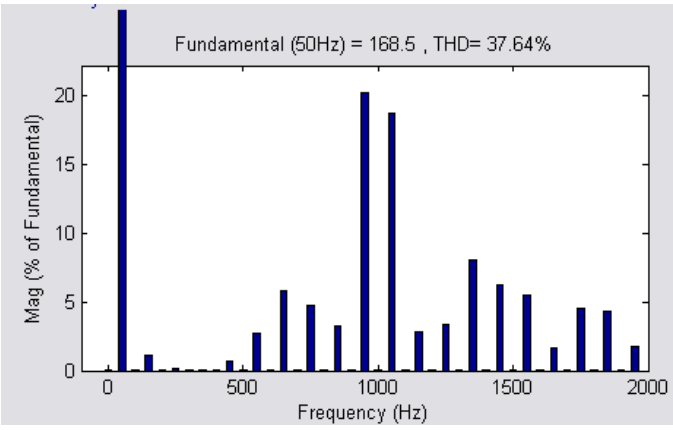

Fig.7 THD in % for single phase cascaded H-bridge multilevel inverter

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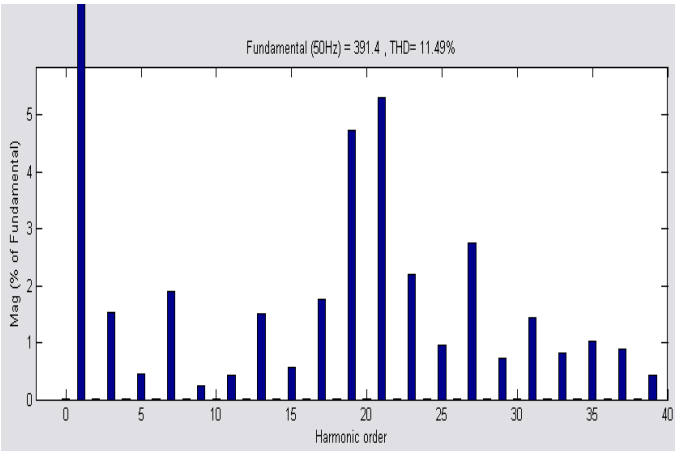

Fig.7 THD in % for proposed multilevel inverter

VI. CONCLUSION

The proposed multilevel inverter topology is much superior than the conventional cascaded H-bridge topology in terms of the number of level in the output voltage, magnitude of the output voltage, total harmonic distortion(THD). To produce the same output voltage the cascaded H-bridge has to use the two cells where as only one cell is required with the proposed topology or in other words input DC voltage sorce required in proposed topologi is half of that required in conventional CHB.

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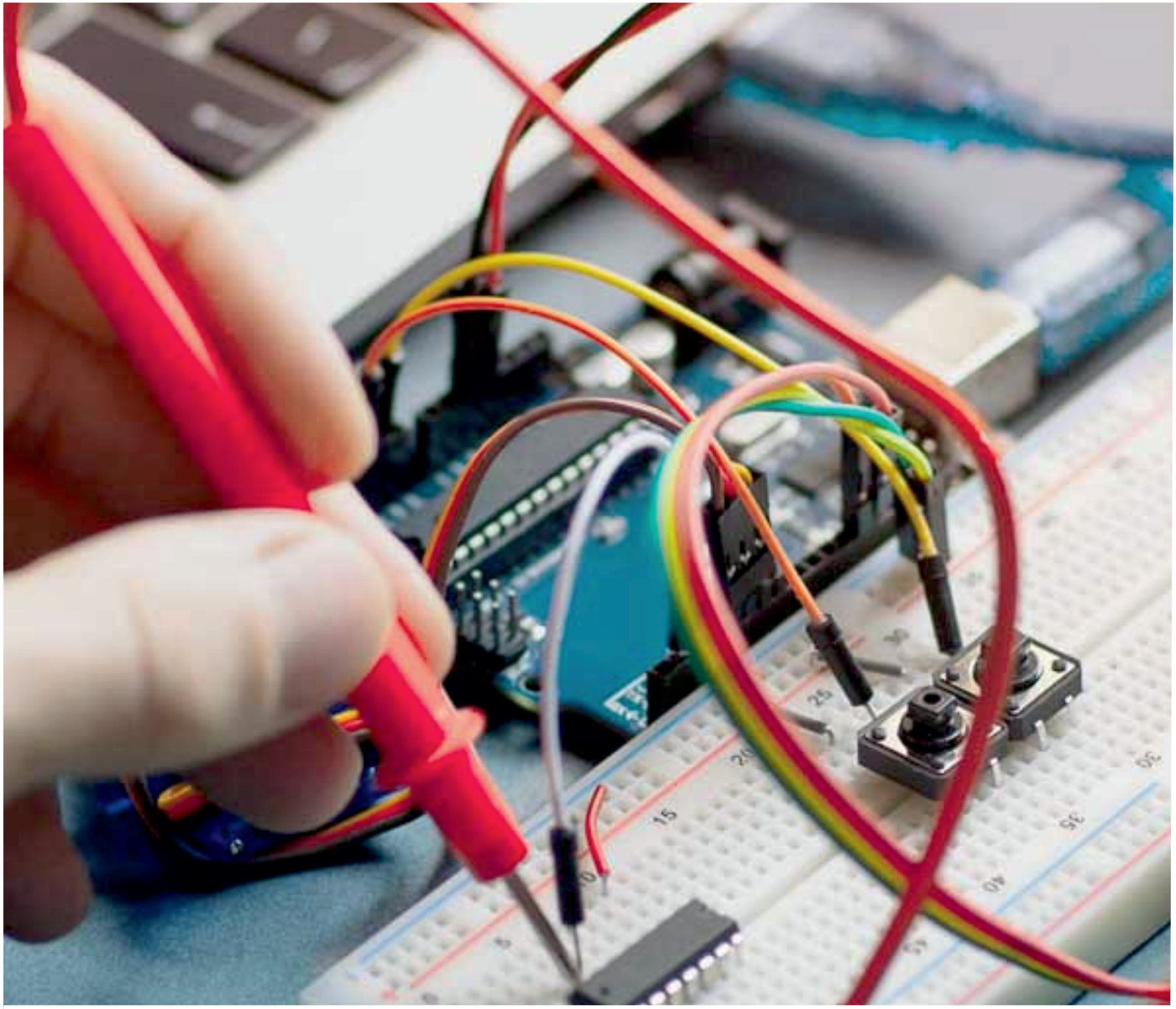

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