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Development of a Small Signal Amplifier with Modeling of BJT-JFET Unit in Sziklai Pair Topology

Sachchidanand Shukla[1], Geetika Srivastava[2], Pratima Soni[3], Ramesh Mishra[4]

Professor, Dept. of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, UP, India[1]

Associate Professor, Dept. of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, UP, India[2]

Research Scholar, Dept. of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya, UP, India[3]

Assistant Professor, Dept. of ECE, I.E.T., Dr. Ram Manohar Lohia Avadh University, Ayodhya, UP, India[4]

ABSTRACT: As a novel approach, two different models of BJT-JFET unit in Sziklai pair topology is used to design Small signal amplifiers. First amplifier circuit provides 28.818 maximum voltage gain, 40.965 current gain, 1.4319MHz bandwidth with 0.87% THD and therefore may find wide applicability in various analog communication circuits. However the second amplifier circuit with 5.738 maximum voltage gain, 5.517 current gain, 13.418Hz bandwidth and 6.30% THD can be used to amplify fluctuations of low frequency and low magnitude such as low frequency waves released by human brain or the seismic waves produced during earthquake or heavy explosion. The present investigation also deals with qualitative analysis of the proposed amplifier circuits.

KEYWORDS: Sziklai Pair, Small Signal Amplifier, Circuit Simulation.

I.INTRODUCTION

Sziklai pair, also referred as Complementary Darlington Pair or Feedback Pair, is often compared with Darlington Pair due to almost identical range of current gain, input resistance, output resistance and voltage gain [1]-[5]. The current gain factor β of Sziklai pair ($\beta_1\beta_2+\beta_1$) is slightly less than Darlington pair ($\beta_1\beta_2+\beta_1+\beta_2$) due to small amount of in-built negative feedback, but for $\beta>100$ both are approximated as $\beta\approx\beta_1\beta_2$ [1]-[6]. However, Sziklai pair holds better linearity (less distortion, if used in audio range amplifiers) with half base-turn-on voltage than Darlington pair [2]-[6],[7]. Sziklai Pairs are being frequently used by electronic industry to design push pull power amplifiers but use of this paired unit in small signal amplifier circuits is still under the developmental phase [3]-[5].

Present investigation is focused around the development and analysis of small signal amplifiers using two different models of the hybrid unit of NPN transistor (driver) and P-channel JFET in Sziklai pair topology.

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II.CIRCUIT DETAILS

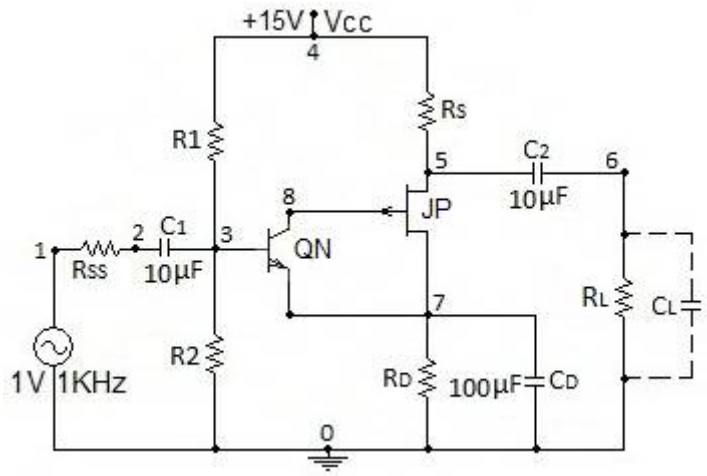

Fig.1. Describing basic structure of the amplifiers under discussion (referred as Circuit-1 and Circuit-2)

PSpice simulation is done to carry present investigations [8]. The basic circuit idea of the two different amplifiers under discussion is depicted in Fig.1. The first amplifier, mentioned in the present discussion as Circuit-1, includes biasing parameters R_1=100KΩ, R_2=47KΩ, R_{SS}=500Ω, R_S=9KΩ, R_D=5KΩ and R_L=10KΩ whereas the second amplifier, referred herein as Circuit-2 accommodates R_1=70KΩ, R_2=40KΩ, R_{SS}=100Ω, R_S=8KΩ, R_D=6KΩ, R_L=20KΩ and C_L=10µF. C_L has to be essentially included in Circuit-2 for the reported observations. Because of using NPN transistor at driver position in both of the hybrid units, the respective device models are treated as to follow N-type Sziklai pair topology [3]-[4].

BJT-JFET hybrid unit of Circuit-1 uses NPN type commercial transistor Q2N2222 (β=255.9) as driver with P-channel type PSpice defined JFET 'Jbreakp' (with V_T=-2) as follower. Similarly, Circuit-2 uses the hybrid paired unit with PSpice defined NPN transistor 'Qbreakn' (with β=100) and P channel JFET 'Jbreakp' [8]. The simulation parameters values used in modeling Sziklai pair unit with BJT and JFET is depicted in Table-I.

TABLE-I: SIMULATION PARAMETERS USED IN DEVICE MODELING

Parameter Description	**Q2N2222 (NPN BJT)**	**Qbreakn (NPN BJT)**	**Jbreakp P-JFET**
IS (p-n saturation current)	14.340000E-15	100.000000E-18	-
BF (Ideal maximum forward beta)	255.9	100	-
NF (Forward current emission coefficient)	1	1	-
BR (Ideal maximum reverse beta)	6.092	1	-
NR (Reverse current emission coefficient)	1	1	-
CN (Base-Collector leakage emission coefficient)	2.42	2.42	-
VTO (Threshold voltage)	-	-	-2
BETA (Transconductance coefficient)	-	-	100.00E-06

Both the amplifiers are using voltage divider biasing methodology, similar to that is traditionally used in Common Emitter circuit configuration. Respective amplifier designs are not carrying any additional biasing resistance as were found essential in earlier Sziklai pair based small signal amplifiers [5],[9].

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Amplifier circuits under discussion are fed by +15V DC supply for biasing with 1V,1KHz AC input signal source but the qualitative performances of the respective circuits are observed at 1mV, 1KHz AC input signal.

III.RESULTS AND DISCUSSIONS

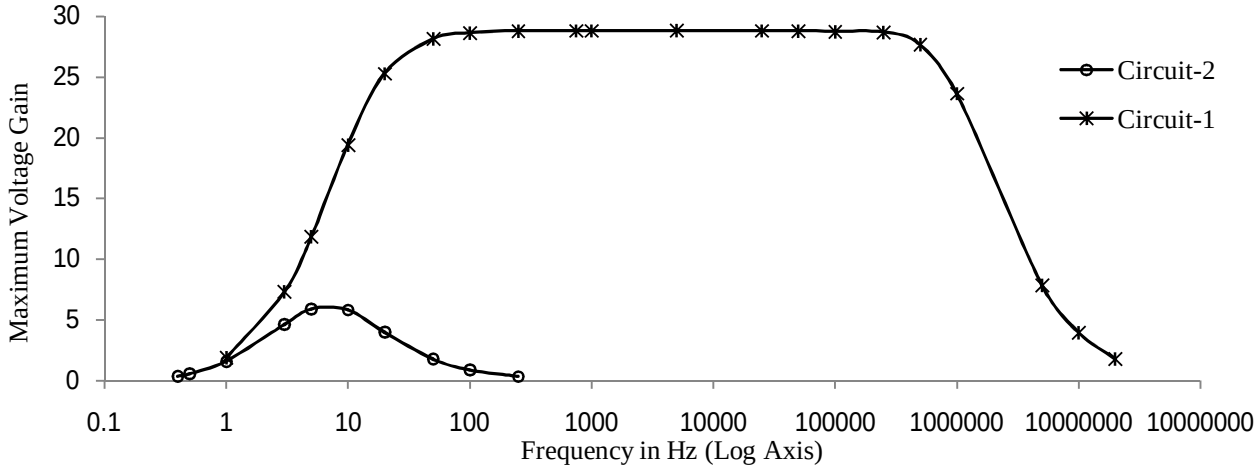

Fig.2. Frequency Response of the Amplifiers under Discussion

TABLE-II: PERFORMANCE PARAMETERS AT ROOM TEMPERATURE 27^{O}C

Performance Parameters	Circuit-1	Circuit-2
Biasing Voltage (DC)	+15V	+15V
Maximum Voltage Gain (A_{VG})	28.818	5.738
Maximum Current Gain (A_{IG})	40.965	5.517
Band Width (B_W)	1.43198MHz	13.418Hz
Lower Cut-off Frequency (f_L)	10.979Hz	2.058Hz
Higher Cut-off Frequency (f_H)	1.432MHz	15.476Hz
Input Signal Voltage used for present observations (V_I)	1.0 mV	1.0 mV
Input Signal Voltage range for purposeful amplification	10µV-9mV	1µV-2mV
Output Phase Difference θ^o	180	180
Total Harmonic Distortion (THD)	0.876%	6.30%

Observations corresponding to various performance parameters (at 27^{o}C) of the proposed amplifiers (described as Circuit-1 and Circuit-2) are listed in Table-II. The frequency response of the respective designs are depicted in Fig.2. Figure clearly indicates that both the circuits are free from the poor response problem at higher frequencies as usually obtained in Darlington pair based small signal amplifiers [5]-[7],[10]-[11].

It is evident from the Table-II (and Fig.2) that Circuit-1 amplifier holds high voltage and current gain (28.818 and 40.965 respectively), wider bandwidth (1.413198MHz) and low THD (0.876%) than Circuit-2 amplifier which produces 5.738 Voltage gain, 5.517 Current gain, 13.418Hz Bandwidth and 6.30%THD. Circuit-1 amplifier produces purposeful amplification in 10µV-9mV range of input signal voltage whereas this range for Circuit-2 amplifier is 1µV-2mV at 1KHz frequency. The outcomes corresponding to Circuit-1 and Circuit-2 suggests different kind of uses of respective designs that are listed in forthcoming lines.

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TABLE-IIIA: PERFORMANCE PARAMETERS OF CIRCUIT-1 AMPLIFIER WITH PRODUCTIVE RANGE OF BIASING RESISTANCES

Parameters	Circuit-1: Minimum and Maximum Permissible Range of Biasing Resistances for meaningful amplification									
	R_1		R_2		R_{SS}		R_S		R_D	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
	60KΩ	150KΩ	33KΩ	90KΩ	1Ω	350KΩ	300Ω	12KΩ	3KΩ	6KΩ
A_{VG}	1.1712	2.595	3.370	1.264	29.866	1.126	1.802	26.573	2.798	9.737
A_{IG}	0.853	9.168	8.06	0.092	40.965	40.965	2.668	23.019	0.900	22.45
B_W (MHz)	0.731245	0.747798	1.8899	0.731245	6.135	0.64923	6.511	1.066	0.709462	2.53
f_L (Hz)	24.551	1.661	1.99	24.454	11.221	5.007	11.18	10.42	25.01	4.03
f_H (MHz)	0.73127	0.74780	1.89	0.73127	6.136	0.64929	6.512	1.067	0.70948	2.531
THD%	2.041	0.75	0.72	2.12	0.90	2.49	0.89	0.76	3.41	0.81

TABLE-IIIB: PERFORMANCE PARAMETERS OF CIRCUIT-2 AMPLIFIER WITH PRODUCTIVE RANGE OF BIASING RESISTANCES

Parameters	Circuit-2: Minimum and Maximum Permissible Range of Biasing Resistances for meaningful amplification									
	R_1		R_2		R_{SS}		R_S		R_D	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
	50KΩ	100KΩ	30KΩ	80KΩ	10Ω	10KΩ	1KΩ	15KΩ	4KΩ	10KΩ
A_{VG}	6.197	1.480	1.890	1.854	5.764	3.815	1.828	1.481	6.737	1.175
A_{IG}	3.432	2.157	2.016	0.58	5.516	5.509	1.275	0.386	3.705	1.572
B_W (Hz)	40.80	5.71	6.117	177.81	13.081	10.841	40.78	119.481	52.097	5.435
f_L (Hz)	3.564	0.97	1.195	48.34	2.557	2.236	5.98	33.440	3.824	0.906
f_H (Hz)	44.36	6.68	7.312	226.15	15.638	13.077	46.76	152.921	55.921	6.359
THD%	5.56	6.34	5.41	2.76	6.51	6.56	4.28	3.96	4.16	5.37

As usual biasing resistances play an important role in amplifier performance of respective amplifiers [10]. Table-IIIA and IIIB show the variation of performance parameters of Circuit-1 and Circuit-2 amplifiers respectively with permissible resistance range corresponding to R_1, R_2, R_{SS}, R_S, and R_D for meaningful amplification. Indicators MIN and MAX in Tables IIIA and IIIB show the minimum and maximum permissible values of biasing resistances for meaningful amplification. It is evident from respective Tables that both the amplifier designs respond positively for wider range of variations in biasing resistances. This provides a flexible range of application to respective amplifier designs to be used in communication electronics as well as in bio-medical instruments.

TABLE-IV: VARIATION OF A_{VG} A_{IG} B_W AND THD VALUES WITH LOAD CAPACITANCE C_L FOR CIRCUIT-2 AMPLIFIER

Load Capacitance C_L (μF)	Performance Parameters			
	Voltage Gain (A_{VG})	Current Gain (A_{IG})	Bandwidth (B_W)	THD (%)
50	1.3526	1.457	11.015Hz	2.39
10	5.738	5.517	13.418Hz	6.30
1	19.739	13.882	37.724Hz	5.17
0	25.842	16.613	-	2.54
0.1	25.912	16.296	288.12Hz	5.68
0.01	26.746	16.579	2.786KHz	3.11
0.001	26.832	16.609	27.77KHz	2.59
0.0001	26.841	16.612	277.940KHz	2.49

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Load capacitance C_L plays an important role in the amplification performance of Circuit-2 [9],[12]. Variation of maximum voltage gain, current gain, bandwidth and THD with different values of C_L are depicted in Table-IV. The RC network at load position in Circuit-2 provides variation in tuning frequency by changing C_L values. This results increase in maximum voltage gain, current gain and bandwidth with the downfall of C_L values. When C_L is removed (C_L=0) from Circuit-2, apart from rise in voltage and current gain, the circuit starts behaving as high pass filter with a lower cutoff frequency 8.626Hz. It is clearly evident from the table that C_L values ranging in 1 µF to 50 µF brings amplifiers applicability in amplification of seismic waves or the waves released by human brain whereas C_L values ranging in 0.0001 µF to 0.1 µF suggests that this amplifier can be used as analog front end amplifier for biopotential measurement. However with C_L=0 the similar design can be used for processing of low amplitude signals ranging above 8.626Hz.

TABLE-V: VARIATION OF A_{VG} A_{IG} B_W AND THD VALUES WITH DC BIASING VOLTAGE

DC Biasing Voltage Vcc (Volts)	Performance Parameters							
	Circuit-1 Amplifier				Circuit-2 Amplifier			
	Voltage Gain (A_{VG})	Current Gain (A_{IG})	Bandwidth (B_W)	THD (%)	Voltage Gain (A_{VG})	Current Gain (A_{IG})	Bandwidth (B_W)	THD (%)
+10	1.562	5.066	22.198	0.65	1.290	1.707	5.561	2.86
+15	28.818	40.695	1431.98	0.87	5.738	5.517	13.418	6.30
+20	74.952	57.966	773.722	0.86	7.602	6.592	30.931	6.77
+25	118.462	64.836	557.196	0.84	8.108	6.843	49.255	2.80
+30	158.658	68.546	452.308	0.81	8.353	6.940	67.185	3.88
+40	229.908	72.325	349.171	0.80	8.563	7.038	102.576	3.19

Variation of Maximum voltage gain, current gain, bandwidth and THD with different values of DC biasing supply V_{CC} is depicted in Table-V. It is evident that minimum 10 Volts of DC biasing supply is required to switch ON the respective circuits under discussion. However, at 10V V_{CC}, Circuit-1 amplifier shows poor response beyond 30KHz frequency similar to that of small-signal Darlington pair amplifier [6],[10].

For both amplifiers Voltage and Current gains are found to be increasing with V_{CC}. Bandwidth corresponding to Circuit-2 amplifier gradually increases with V_{CC} but for Circuit-1 amplifier bandwidth increases up to 15V and thereafter it decreases with increasing values of V_{CC}. Thus for the optimum performance of respective amplifiers, the suggested DC biasing voltage for Circuit-1 is +15V whereas this for Circuit-2 is +25V at which THD is found minimum.

The values of performance parameters of respective amplifiers as depicted in Tables II, IIIA, IIIB, IV and V suggest that Circuit-1 amplifier may find wide applicability in various analog communication circuits e.g. radio/TV receivers, low frequency power sources, analog front end amplifier for biopotential measurement and other audible range communication equipments whereas Circuit-2 amplifier can be used to amplify fluctuations of low frequency and low magnitude such as low frequency waves released by human brain and seismic waves produced during earthquake or heavy explosion.

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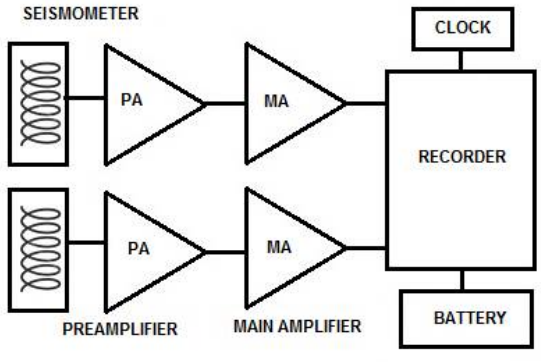

Fig.3. Seismograph

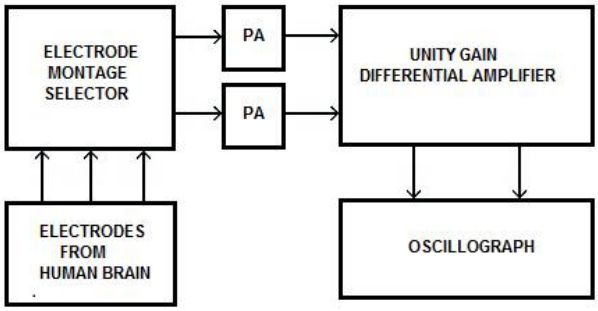

Fig.4. Electroencephalogram

Fig.3 and Fig.4 show the architectural idea of Seismograph (block diagram of a high performance field station for explosion seismology work) and Electroencephalogram (EEG a biomedical instrument used to track and record brain wave pattern) respectively with possible positions of Circuit-2 amplifier design (indicated as Preamplifier) [13]-[14]. Low bandwidth (ranging below 100 Hz) with low f_L and f_H values, low AC input amplifying signal range (1μv-2mv) and moderate THD of the Circuit-2 amplifier for various combinations of biasing resistances leads to a favourable environment for such application. It is noteworthy that waves released by human brain and the seismic waves normally holds frequency range of 1-100Hz with 1μV to few mV amplitude strength. Therefore, varying various biasing resistances of Circuit-2 amplifier, as depicted in Tables - IIIA, IIIB, IV and V, can lead very low frequency signals to be scaled-up at desired level for seismograph and EEG with moderate level of THD.

TABLE-VI: VARIATION OF A_{VG} A_{IG} B_W AND THD VALUES WITH TEMPERATURE (^OC)

Temp (^OC)	Performance Parameters							
	Circuit-1 Amplifier				Circuit-2 Amplifier			
	Voltage Gain (A_{VG})	Current Gain (A_{IG})	Bandwidth (B_W)	THD (%)	Voltage Gain (A_{VG})	Current Gain (A_{IG})	Bandwidth (B_W)	THD (%)
-27	20.877	29.772	1.763	0.96	4.787	4.886	9.991	2.94
-10	23.672	33.387	1.636	0.93	5.159	5.172	11.144	2.38
0	25.183	34.472	1.577	0.91	5.333	5.292	11.721	5.39
10	26.601	37.529	1.517	0.90	5.509	5.392	12.187	2.25
27	28.818	40.695	1.432	0.87	5.738	5.517	13.418	6.30
40	30.363	43.541	1.376	0.85	5.873	5.606	13.591	2.78
50	31.470	45.494	1.340	0.84	5.962	5.658	14.013	6.56

Variation of Maximum voltage gain, current gain, bandwidth and THD with temperature variation is depicted in Table-VI. Voltage and Current gain increases with rising temperature for both the amplifiers under discussion. Bandwidth corresponding to Fig.1 amplifier decreases whereas it increases for amplifier of Fig.2 with temperature elevation. Total Harmonic Distortion decreases with temperature elevation for Fig.1 amplifier whereas it alternatively decreases and increases for Fig.2 amplifier with increasing temperature.

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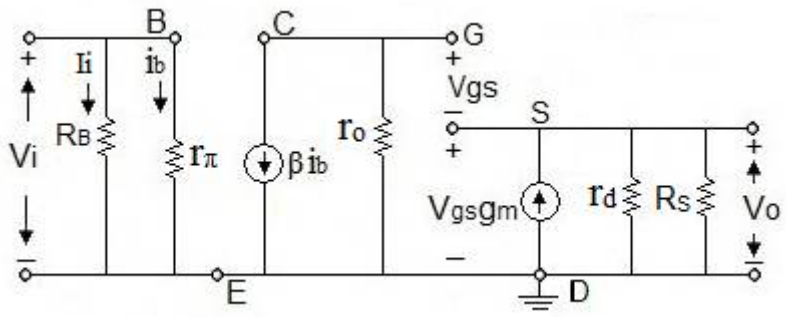

Fig.5. Small-signal AC equivalent of the Proposed amplifier Design

Small-signal AC equivalent circuit of the amplifiers under discussion is depicted in Fig.5 whereas observed values of various Small signal AC parameters corresponding to BJT and JFET used in Sziklai pair topology based hybrid unit models of respective amplifiers are listed in Table-VII.

Based on simulation results as depicted in Table-VI, BJT of the Sziklai unit in Circuit-1 consists base-emitter resistance r_π=24KΩ whereas for Circuit-2 it is r_π=18.4KΩ. Collector-emitter resistance of Circuit-1 BJT is r_o=503KΩ whereas for Circuit-2 it is r_o=1.00TΩ. DC current gain factor for Circuit-1 BJT is β=141 and for Circuit-2 BJT it is β=100. However P-JFET of Circuit-1 and Circuit-2 consists g_m=0.52mA/V and g_m=0.50mA/V respectively. Drain-source resistance for Circuit-1 P JFET is r_d=5.40KΩ and that for Circuit-2 P JFET r_d=6.19KΩ.

Mathematical analysis of the equivalent circuit suggests the following expression for small-signal AC voltage gain of the proposed amplifier design-

$$A_V = \frac{V_O}{V_i} = \frac{\beta r_o}{r_\pi\left(\frac{1}{g_m R_Y} - 1\right)}$$

Similarly, the small-signal AC current gain of the proposed amplifier design may be obtained as-

$$A_I = \frac{i_O}{I_i} = \frac{-\beta r_o}{R_Y\left(\frac{1}{g_m R_Y} - 1\right)\left(1 + \frac{r_\pi}{R_B}\right)}$$

TABLE-VII: SMALL SIGNAL AC PARAMETERS FOR THE MODELED DEVICES USING BJT-JFET HYBRID UNIT UNDER SZIKLAI PAIR TOPOLOGY

Small signal AC parameters for BJT-JFET Hybrid Unit Models under Sziklai Pair Topology	BJT-JFET Hybrid Unit Models under Sziklai Pair Topology			
	Device Model (Circuit-1)		Device Model (Circuit-2)	
	NPN BJT (Q2N2222)	P JFET (Jbreakp)	NPN BJT (Qbreakn)	P JFET (Jbreakp)
IB (Current flowing into Base)	1.23µA	-	1.65 µA	-
IC / ID (Current flowing into Collector/Drain)	0.152mA	-0.679mA	0.165 mA	-0.628mA
VBE / VGS (Voltage across Base-Emitter Junction / Gate-Source)	0.596V	-0.606V	0.645V	-0.505V
VBC (Voltage across Base-Collector Junction, Showing junction is reverse biased)	-2.16V	-	-2.74V	-

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VCE (Voltage across Collector-Emitter Region, indicate forward active operating region) / VDS (Voltage across Drain-Source)	2.76V	-3.36V	3.38V	-3.89V
BETADC (Small signal DC current gain)	123	-	100	-
GM (Small signal transconductance)	5.85 mA/V	0.52mA/V	5.43mA/V	0.50 mA/V
RPI (Small signal AC base emitter resistance)	24KΩ	-	18.4KΩ	-
RX (The base spreading resistance, the ohmic resistance of the base contact in BJT)	10Ω	-	00Ω	-
RO (Small signal AC collector emitter resistance)	503KΩ	-	1.00TΩ	-
CBE (Zero-Bias Junction Capacitance across Base-Emitter Junction)	0.373pF	-	00F	-
CBC (Zero-Bias Junction Capacitance across Base-Collector Junction)	4.60pF	-	00F	-
CJS (Zero-Bias Junction Capacitance across Collector-substrate) / CGD (Gate-Drain Capacitance)	00F	00F	00F	00F
BETAAC (Small signal AC current gain)	141	-	100	-
CBX/CBX2 (Extrinsic-base to intrinsic-collectorCapacitance)	0.00E+00	-	0.00E+00	-
FT/FT2 (Gain-Bandwidth product) / GDS (Channel Length Modulation)	2.22E+07	0.00E+00	8.65E+16	0.00E+00

IV.CONCLUSION

It can be concluded that Circuit-1 amplifier holds higher voltage and current gain with wider bandwidth and lower THD than Circuit 2. Circuit-1 amplifier produces purposeful amplification in 10µV-9mV range of input signal voltage whereas this range for Circuit-2 amplifier is 1µV-2mV at 1KHz frequency. Circuit-2 is suitable for applications with higher sensitivity requirements and best suited for measurement of bio potentials like human EEG measurement that ranges from 10µV to 100 µV for adult human in the frequency range of 10 to 50 Hz.

The high Bandwidth at µV range of circuit-2, makes it a suitable candidate for high sensitivity ultrasonic transducers and it can also be used in ultrasonic hydrophone design.

Both the designs of Circuit-1 and Circuit-2 are observed to be free from the poor response problem at higher frequencies as usually obtained in Darlington pair based small signal amplifiers. Respective amplifier designs produce meaningful amplification for 10-40 Volts of DC biasing voltage in -27 to 50 oC temperature range and respond positively for wider range of variations in biasing resistances. Use of load capacitance C_L is necessary to obtain reported results for Circuit-2 design.

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Vol. 8, Issue 5, May 2019

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