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Design of Comparator Using Reversible Logic

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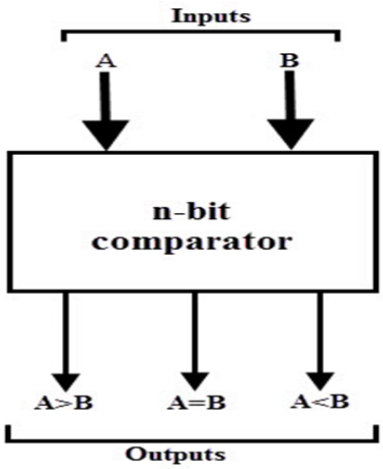
ABSTRACT: Digital comparator is an important part of ALU for comparison operations .In this method,4 bit digital comparator is designed using 2 bit comparator with reversible logic. Reversible logic is less heat dissipating characteristics.The main purpose of designing reversible logic are to decrease quantum cost , depth of the circuits and the number of garbage output.It has found its applications in several technologies such as low power CMOS,nanotechnology and optical computing.It can simulated on LT SPICE software.

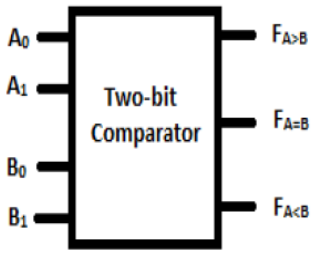
KEYWORDS: Reversible logic gate,low power,2 bit comparator,4 bit comparator .

I. INTRODUCTION

Digital Comparator

A digital comparator is a logic circuit that is used to compare the magnitude of two binary numbers say A and B. The result of comparison is specified by three binary variables that indicate whether A<B, A=B or A>B.The XNOR gate is a basic comparator because its output is a 1 only if its two input bits are equal.





2 bit Comparator

It compares two binary numbers , each of two bits and produce their relation such as one number is equal or greater than or less thanthe other. It has four input and three output.

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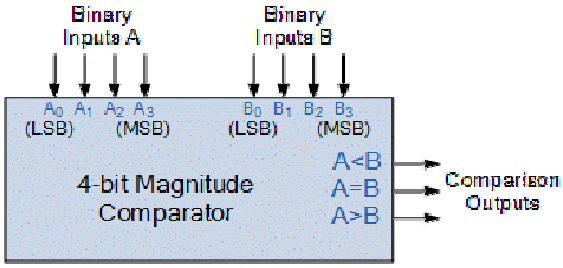
4 bit Comparator

A 4 bit comparator is a hardware electronic device that takes two number of

4 binary bits each has input and determines whether one number is greater than, less than or equal to the other number.



It can compares two 4 bit binary number Aand B and the outcome of comparator has been specified by three binary variables G(A>B),E(A=B),L(A<B).

II. REVERSIBLE LOGIC

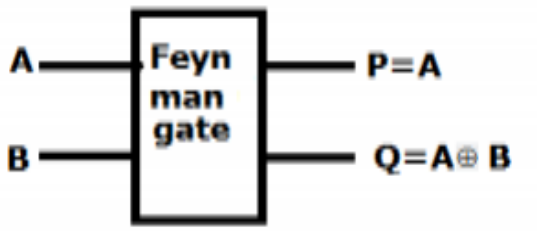
Reversible Gates are circuits in which number of outputs is equal to the number of inputs .And there is a one to one mapping between the vector of inputsand outputs.

Reversible Logic Gates

1. BJN Gate
2. UR Gate
3. Feynman Gate
4. TR Gate

FG Gate

Feynman gate, which realises XOR gate with a garbage output ‘A’. If B=‘0’ it duplicates the input ‘A’ and if B=‘1’, then it inverts the input ‘A’ to the output Q.



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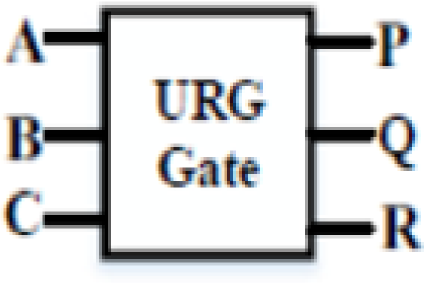
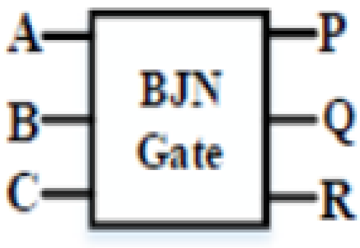
UR Gate



$$P = (A + B) \oplus C$$
$$Q = B$$
$$R = AB \oplus C$$

BJN Gate



$$P = A$$
$$Q = B$$
$$R = (A + B) \oplus C$$

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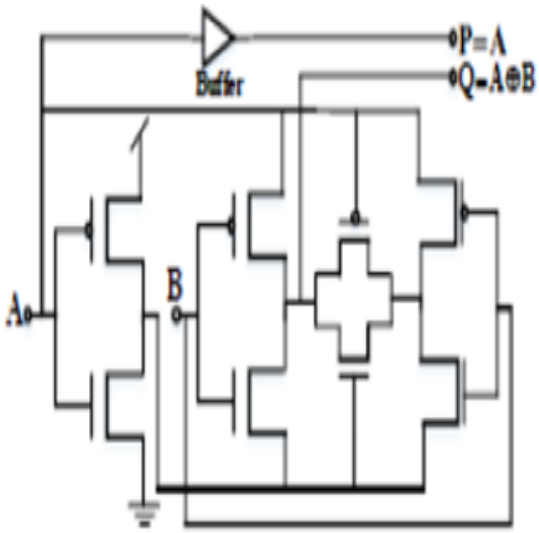
TR Gate

The gate has 3 inputs and 3 outputs having inputs (A, B, C) mapped to the outputs (P=A, Q=A⊕ B, R= (A.B1) ⊕ C).

Transistor Diagaram for Logic Gates

Feynman Gate



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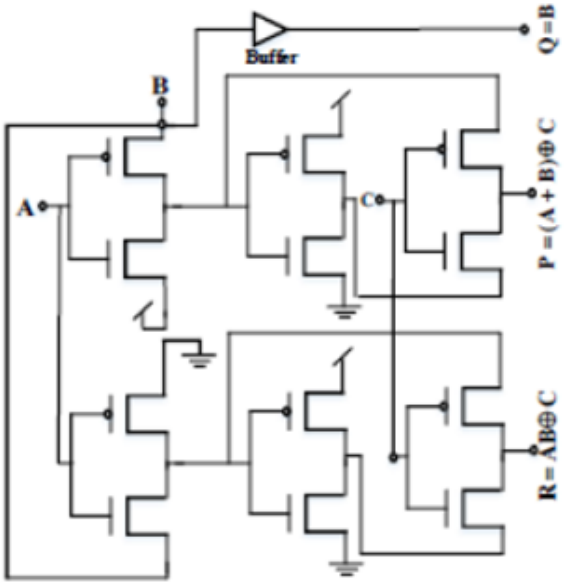
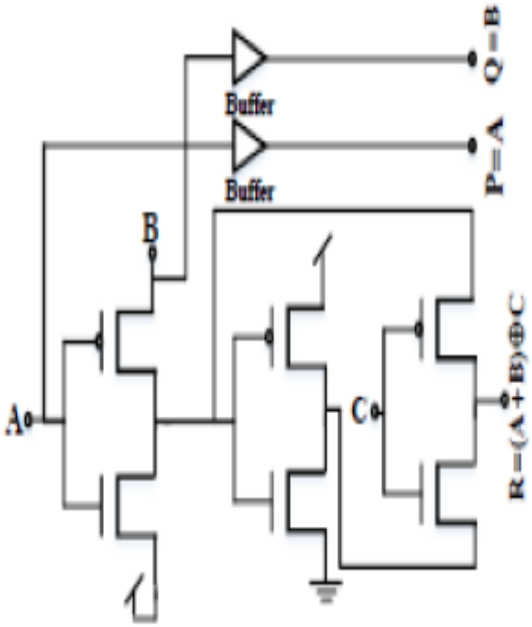
Universal Reversible Gate



BJN Gate



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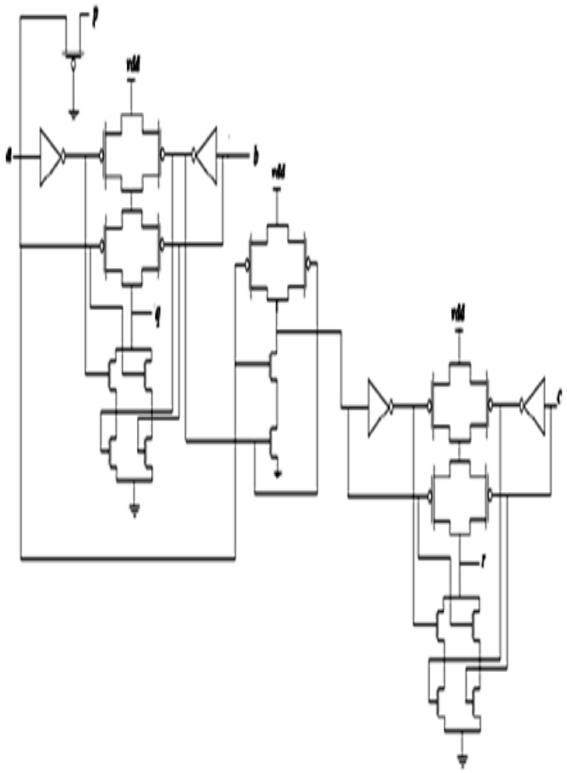
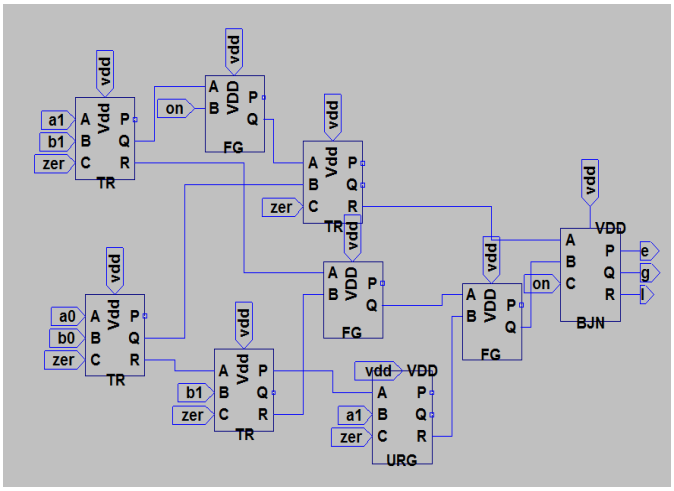
TR Gate



2 bit Comparator circuit diagram



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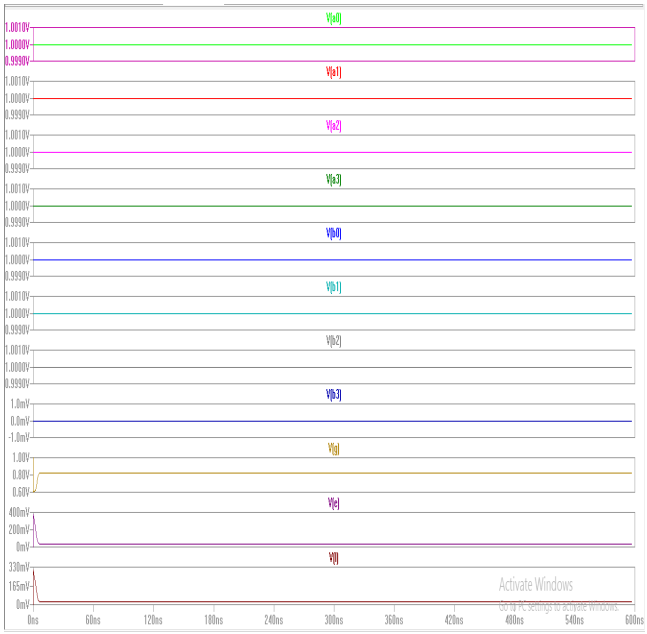
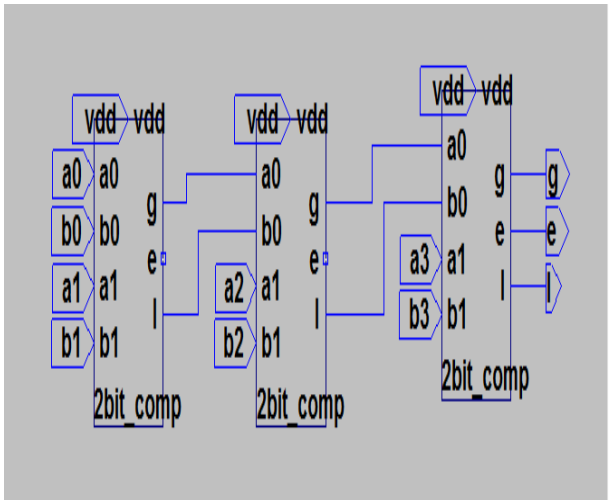
2 bit comparator output



4 bit comparator circuit diagram



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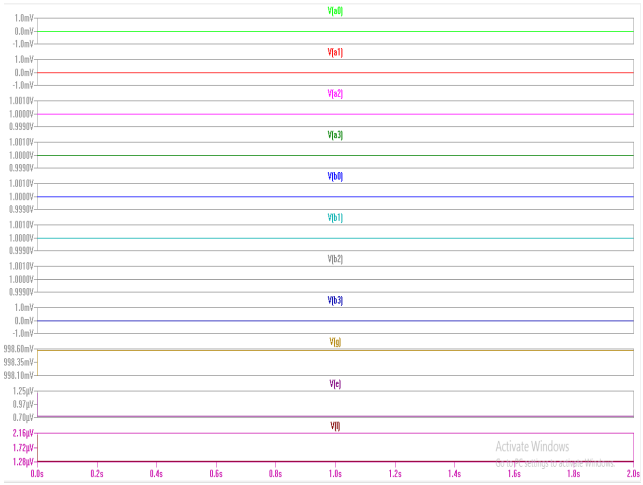
4 bit comparator output



IV. CONCLUSION

Reversible logic gates are used to reduce number of gate ,garbage output and constant inputs . Reversible logic gates are reduce the power consumption . So the designing of comparator by using the reversible logic gates .

REFERENCES

1 P. K. Lala, J. P. Parkerson, P. Chakraborty, “Adder Designs using Reversible Logic Gates” WSEAS Transactions. on Circuits and Systems, 2017.

2 Diganta Sengupta, Mahamuda Sultana, Atal Chaudhuri, “Realization of a Novel Reversible SCG Gate and its Application for Designing Parallel Adder/Subtractor and Match Logic”, International Journal of Computer Applications (0975-8887), Vol. 31, No. 9,pp. 30-35, October 2016.

3 B. Raghu kanth, B. Murali Krishna, M. Sridhar, V. G. Santhi Swaroop, “A Distinguish between Reversible and Conventional Logic Gates”, International Journal of Engineering Research and Applications (IJERA), Vol. 2, Issue 2, pp. 148-151, Mar-Apr 2015.

4 H. P. Sinha, Nidhi Syal, “Design of Fault Tolerant Reversible Multiplier”, International Journal of Soft Computing and Engineering (IJSCE), Vol. 1, Issue 6, pp. 120-124, January 2014.

5 D. Krishnaveni, M. Geetha Priya, “A Novel Design of Reversible Universal Shift Register with Reduced Delay and Quantum Cost”,Journal of Computing, Vol. 4, Issue 2, pp. 164-173, February 2012.