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Self-Powered IoT Node High Efficiency Solar Power Management System

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ABSTRACT: An efficient micro-scale solar power management architecture for self-powered Internet-of-Things node is presented in this paper. The proposed architecture avoids the linear regulator and presents a complete on-chip switched capacitorbased power converter in order to achieve higher end-to-end efficiency. Unlike traditional architectures, where the harvested energy processes twice, the proposed architecture processes the harvested energy only once before it reaches to the load circuit, irrespective of the ambient conditions. The system efficiency has been improved by 12% over the traditional architecture. The entire power management system has been designed using 0.18-μm CMOS technology node, and the circuit simulations demonstrate that the proposed architectural changes bring in a system efficiency of 82.4% under different light conditions. In addition to that, a hardware setup is created using commercially available ICs and photovoltaic cells, to validate that the proposed power management system is practically realizable. *Index Terms*—DC-DC converter, energy processing, energy scavenging, Internet of Things (IoT), maximum power point tracking, photovoltaic cell, wireless sensor nodes

I. INTRODUCTION

THERE is a great interest in powering IoT nodes by scavenging ambient energy, such as solar radiation [1], thermal gradient [2], mechanical vibration [3], or radio frequency (RF) waves [4]. Based on the applications and area of deployment, appropriate energy source/sources is/are utilized for powering the IoT node [5], [6]. As the ambient conditions are changing, one can not directly connect a harvester to the load as it is not regulated. Moreover, the available scavenged energy may not be sufficient for powering the sensor nodes all the time. Apart from that, unlike a battery, a harvester has a continuous source of power without depletion, but if it is not extracted continuously, the same would be unutilized and lost. Therefore, an interface circuit in between the load and the harvester is needed, in order to maintain regulation both at the input and the output.A typical power management architecture for IoT node is shown in Fig. 1.

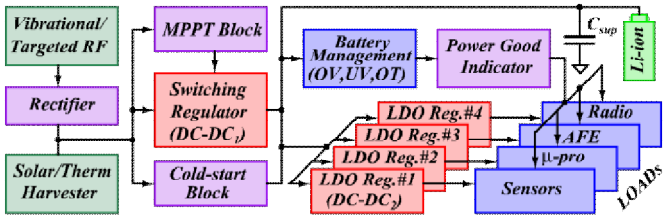

Fig. 1. Typical power management architecture of an IoT node.

DC-DC converters between harvesters and loads. The first converter (DC-DC1) is used to present an optimal impedance to the harvester for transferring maximum power as well as converting the input voltage to a level such that it meets the load requirements. Whereas, the second converter (DC-DC2) is used to provide a clean regulated supply to the noise sensitive analog/RF blocks. Therefore, both the input and output voltages of these converters are set differently by the system requirements. In order to implement DC-DC1, generally switched capacitor based DC-DC converters are preferred over inductive DC-DC converters, because, the integration of high-quality inductors in advance technology node is quite difficult. Moreover, in a typical mixed-signal SoC, there could be 30 isolated power domains for combined analog and RF blocks [7]. Therefore, integration of such a huge number of inductors in a single chip is quite impossible and costly. On the other hand, in some application linear regulators (low-dropout (LDO) regulators) are preferred over switching regulator for powering noise sensitive analog blocks as shown in Fig. 1. In

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this architecture, as the energy is processed twice before it reaches the load circuits, the overall efficiency expected is $\eta DC{-}DC,1{\times}\eta DC{-}DC,2$ and its typical values lies between 65−75%. This includes power transfer losses of associated interface circuits [8], [9]. One of the key issues with this architecture is that the
overall efficiency varies with ambient condition. Because the first switched capacitor DC-DC converter has a fixed voltage up-conversion ratio and its output voltage varies with ambient condition. As a result, the drop across LDO varies with ambient condition and much of the extracted power may simply be dissipated within the LDO, and hence, the overall efficiency will degrade accordingly. Another key issue is that often it utilizes two DC-DC converters even if there is sufficient ambient energy to power the load circuit. In order to address these issues, an efficient architecture has been proposed with following silent features: 1) the overall efficiency
varies minimally with ambient condition, 2) unlike

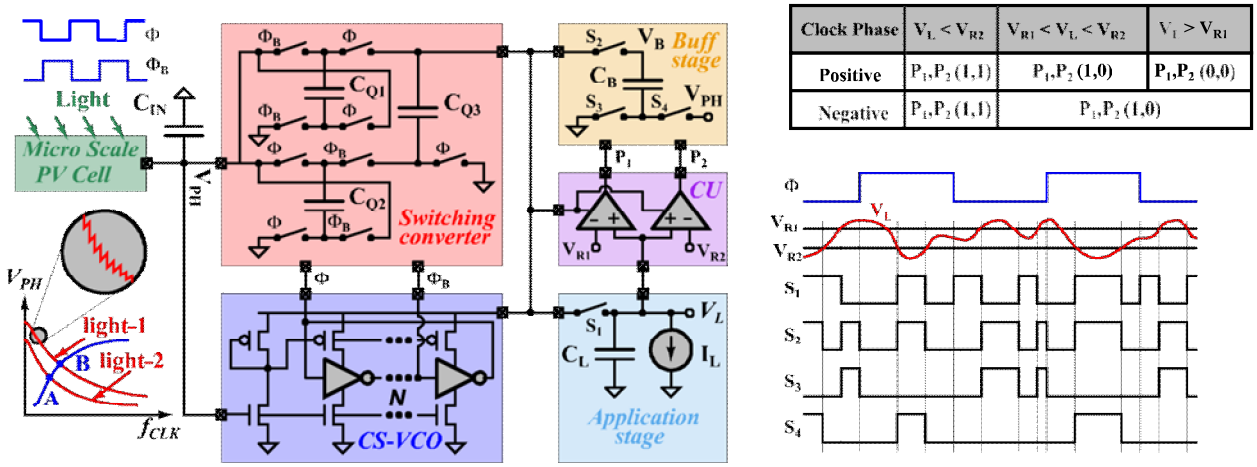

Fig. 2. Proposed power management architecture and the associated control signals for maintaining regulation at the load. *VPH* represents the PV cell terminal voltage and *fCLK* represents the frequency of the switching converter.

traditional architecture, input energy processes once before it reaches to the load circuit, and hence, overall efficiency has been improved by 12%, and 3) avoid inductive and linear converters, but presents a completely on-chip switched capacitor based architecture.
The rest of the paper is organized as follows: Section II discusses the proposed system architecture and its operation. Section III describes the circuit implementation of the proposed architecture. Section IV presents the hardware setup, measurement and simulation results to validate the proposed idea, and finally, Section V concludes the paper.

II. PROPOSED POWER MANAGEMENT ARCHITECTURE

The proposed power management architecture and the associated control signals are shown in Fig. 2. It comprises a switched capacitor boost converter to bring the output voltage several times higher than the input voltage, a current-starved voltage control oscillator (CS-VCO) to generate switching frequencies for the boost converter, a control unit (CU) to regulate the load voltage, a buffer stage to store the excess energy for future references, and an application stage to deliver the load. Due to the high power density and ubiquitous nature of light, a PV cell has been chosen as an energy source for powering the IoT node. The buffer stage has two modes: one is storage mode and other is converter (DC-DC) mode. The storage mode will be activated once there is more than enough ambient energy to supply the load and converter mode will be activated once there is insufficient ambient energy to supply the load. During the storage mode, it will store the excess energy into the buffer capacitor *CB* and during the converter mode, it will act as a linear charge pump circuit, which will pump the stored energy into the application stage. The CU comprises a reference generator associated with a start-up circuit, analog comparators, and few logic gates to generate the required control signals for the system. The reference generator generates two reference voltages *VR*1 and *VR*2, where *VR*1 is greater than *VR*2 by few tens of *m*V. Their difference should be higher than the op-amp offset voltage, in order to avoid unwarranted triggering of the comparator. Apart from that, a start-up circuit is needed to bring up the system

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from the sleep state to an active state if the input voltage is lower than the MOSFET threshold voltage. It will generate an auxiliary voltage higher than the MOSFET threshold voltage, which will eventually turn on the switches of the DC-DC_1 converter and starts transferring charges from the harvester to the load circuit. Previous works report solutions for start-up issue [10], [11] and therefore, this implementation does not focus the startup issues but assumes that the supercapacitor, C_B , is initially charged to bring up the system from the sleep state to an active state.

In order to maintain regulation at the load, V_L is compared with the internal reference voltages V_{R1} and V_{R2}, for generating control signals, P_1 and P_2, and associated switching signals, S_1, S_2, S_3 and S_4, as shown in Fig. 2. Initially, V_L is less than V_{R1} and V_{R2}, and the corresponding control signals are $P_1 = 1$ and $P_2 = 1$, and associated switching signals are $S_1 = 1$, $S_2 = 1$, $S_3 = 0$ and $S_4 = 1$, which will eventually activate the buffer stage as a converter mode and start delivering charges from buffer stage to the application stage to meet the charge deficiency. Once the load regulation is achieved during the negative half cycle of clock, and if the solar energy is more than enough to supply the load, then the corresponding control signals will be $P_1 = 0$ and $P_2 = 0$, and the associated switching signals will be $S_1 = 0$, $S_2 = 1$, $S_3 = 1$ and $S_4 = 0$, which will eventually enable the buffer stage as a storage mode for recharging the supercapacitor C_B . On the contrary, during the positive half cycle, if there is insufficient ambient energy to supply the load, i.e., $V_L < V_{R2}$, control signals, $P_1 = 1$ and $P_2 = 1$, and associated switching signals, $S_1 = 1$, $S_2 = 1$, $S_3 = 0$ and $S_4 = 1$, will activate buffer stage as converter mode, in order to maintain regulation at the load. Therefore, due to the involvement of complementary switching between the buffer stage and the application stage, one could expect few tens of *m*V supply ripple along with the regulated power supply. The magnitude of this ripple depends on the op-amp offset voltage and the delay in the feedback loop. In comparison with the classic architecture shown in Fig. 1, the proposed architecture consists of single stage of DC-DC converter instead of two stages of DC-DC converter in between the harvester and the load. That means, the input energy is processed only once before it reaches to the load. Therefore, due to having two stages of DC-DC converters in series, the classic architecture will be limiting with respect to the overall efficiency compared to the proposed architecture. In addition to that, the proposed architecture avoids power inefficient linear regulators (i.e.,LDOs) and presents an efficient on-chip switched capacitor based architecture.

Generally, the conversion efficiency of a solar cell varies 10% − 40% and degrades further when the ambient light intensities are varying continuously. The conversion efficiency of a PV cell can be improved by tracking and offering optimal impedances dynamically and such a process is known as maximum power point tracking (MPPT). This paper adopted

a low-overhead adaptive MPPT scheme based on the negative feedback control loop [12], which eliminates power hungry micro-controller, current/voltage sensor, analog/digital comparator, and bulky capacitors and resistors. In order to adjust the input impedance of the switching converter for matching with harvester impedance, switching frequencies are varied from few *M*Hz to tens of *M*Hz. The frequency at which the maximum power transfer take place is known as maximum power point (MPP) frequency, *fMPP*. In order to track MPP adaptively with respect to the changes in ambient condition, inherent negative feedback control loop is utilized. This concept is illustrated in Fig. 2, the *VPH* vs. *fCLK* plot.

There are two independent relationships between the same physical variables, *fCLK* and *VPH*, that arise from different sources: i) change in converter input impedance and hence *VPH* with *fCLK* (the red lines) under two different light conditions, and ii) the change in oscillation frequency *fCLK* with CS-VCO control voltage (the blue line). It is to be noted that, for a given light intensity there is only one intersection point (either *A* or *B*) between these two curves and the system will settle at that operating point. In other words, at zero switching frequency, there will be no charge transfer takes place through the switching converter and thus *VPH* will be the open circuit voltage, *VOC*. As the switching frequency increases, the charge transfer take place and *VPH* will begin to reduce the input impedance of the switching converter.

On the contrary, the oscillator frequency reduces as *VPH* starts decreasing. This brings the possibility of an equilibrium point (either point A or B), where both curves will intersect each other and the circuit will lock on that particular switching frequency.

To illustrate the concept a simplified block diagram of the inherent negative feedback control loop is shown in Fig. 3, which comprises of a PV cell, switching converter, and CS-VCO. Let us assume, in absence of light, the current through the PV cell is zero, and hence *IPH* and *VPH* are equals to zero. Once the light impinges on the PV cell, a nonzero photocurrent begins to flow in the capacitor *CI N* and gradually increases the PV cell terminal voltage *VPH*. Once, the *VPH* crosses a certain limit, say 200 *m*V, CS-VCO starts oscillating and forcing the switching converter for

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transferring charges either to the load capacitor/supercapacitor. As the part of *IPH*, begins to flow through the switching converter,

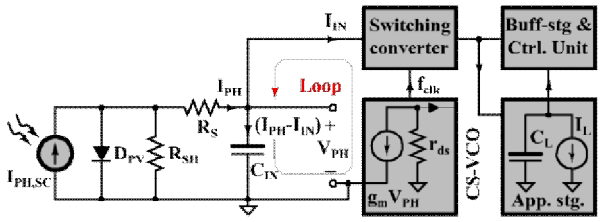

Fig. 3. Simplified block diagram of the proposed architecture for understanding the inherent negative feedback loop for tracking maximum power points.

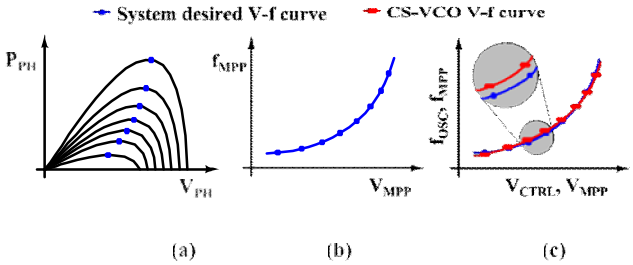

Fig. 4. (a) PV cell output power voltage characteristics, (b) System desired V-f characteristic, and (c) CS-VCO and system desired V-f characteristics.

charging current of *CI N* , i.e., *IPH − II N* , starts reducing and eventually becomes zero when *IPH = II N* . On this point, oscillator locks its frequency and remains in its state until
there is any alteration in ambient light intensities. Now, if there is a change in ambient light intensity, immediately the *IPH* will goes either up or down, however, *II N* will not change imminently due to the delay involved in the feedback loop and therefore, the error current, *IPH −II N* , either goes up or down which eventually reflects on *VPH*. Once *VPH* is changed, *fclk* will change the input impedance of the switching converter accordingly, which will change *II N* and reduces the error current and eventually becomes zero after few iteration.
Now, in order to make sure that the locking frequency is the maximum power point (MPP) frequency, CS-VCO has been trained in such a way that it passes through all the system desired MPP points as shown in Fig. 4. Fig. 4(a) shows the PV cell power voltage characteristics and maximum power points under different light intensities. To extract maximum power from this harvester, switching converter input voltage has to be the maximum power point (MPP) voltages, which are marked as a blue dots. In order to get these *VMPPs*, CS-VCO has been disconnected from the loop and plotted the combined characteristics of PV cell and switching converter in Fig. 4(b), which is nothing but system desired $V - f$ characteristic.
Therefore, one has to design a CS-VCO, which will approximate the desired $V - f$ curve well enough such that the disparity between them is negligible as shown in Fig. 4(c). Therefore, every stable point will be the MPP point of this feedback control loop.

III. CIRCUIT IMPLEMENTATION

Fig. 5 shows the complete circuit diagram of the proposed power management architecture. A tree-topology charge pump[13] is adopted as switching converter for better charge transfer capability, compared to a linear charge pump

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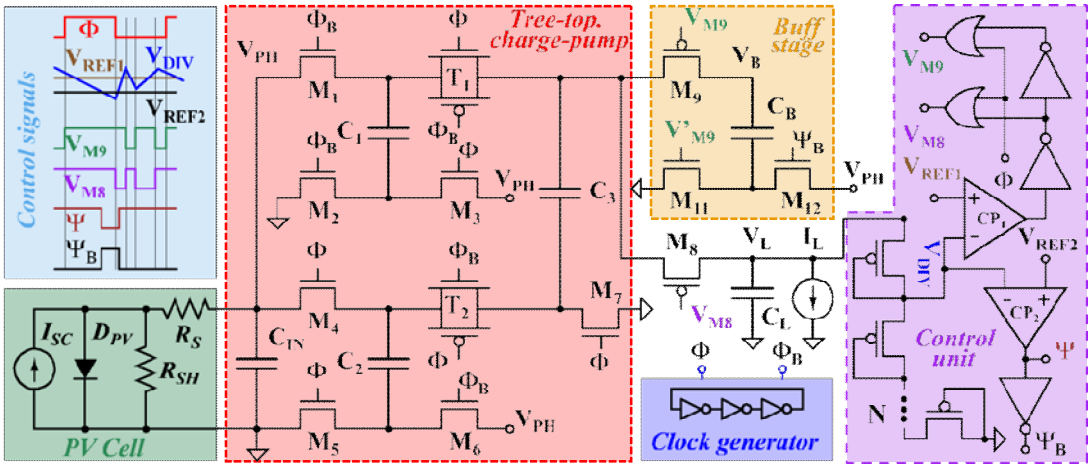

Fig. 5. Circuit diagram of the proposed power management architecture.

topology. To realize charge transfer switches (CTSs), n-MOS and p-MOS transistors and transmission gates are employed. Placement of respective CTSs are made based on their terminal voltages in order to get lower on resistance [14]. Pumping capacitors are realized by on-chip MOS gate capacitors to achieve compact chip area. Due to the presence of a switching converter in between the harvester and load, harvester voltage will experience some ripple, and one can suppress it by placing a capacitor, *CI N* , in between the harvester and switching converter. In control unit, in order to get a scaled version

of load voltage with low power consumption and small area, a voltage divider is formed by cascading PMOS transistors in subthreshold regime instead of a traditional resistor divider circuit. Two analog comparators are used to compare the scaled load voltage, *VDIV* , with two reference voltages, *VREF*1 and *VREF*2. A two-stage open loop transconductance amplifier with push-pull inverters in a cascade is used to realize the comparator circuit, as described by Allen and Holberg [15]. However, special care has been taken into consideration to realize high speed (> 50 *M*Hz) as well as low voltage (*VDD* = 1 V) operations. CMOS inverters and logic gates are used

for generating complementary switching signals for utilizing the buffer stage either as a storage mode or as a converter mode. Current starved inverters are employed to make the ring oscillator and phase shifter circuits are used to generate nonoverlapping clock signals as shown in Fig. 6. In order to get 50% duty cycle, *D*−flip flops are employed after the phase shifter circuits. In order to drive a heavy load (gate capacitor of the CTSs) with least propagation delay, buffer stages are added after the phase shifter. The buffer stage consists of a series of progressively sized inverters and its propagation delay will be minimized when each stage bears the same effort [16]. During the positive half cycle of clock _, capacitor *C*2 will be charged from the harvester and capacitor *C*1 will be discharged to the capacitor *C*3. While, in negative half cycle of clock _, capacitor *C*1 is getting charged from the harvester and capacitors *C*2 and *C*3 along with *VPH* will discharge either capacitor *CL* or *CB*, depending on the control signals *VM*8 and *VM*9. In order to generate these control signals, *CP*1 compares *VDIV* with *VREF*1 and triggers either control signals, CP_1 compares V_{DIV} with V_{REF1} and triggers either

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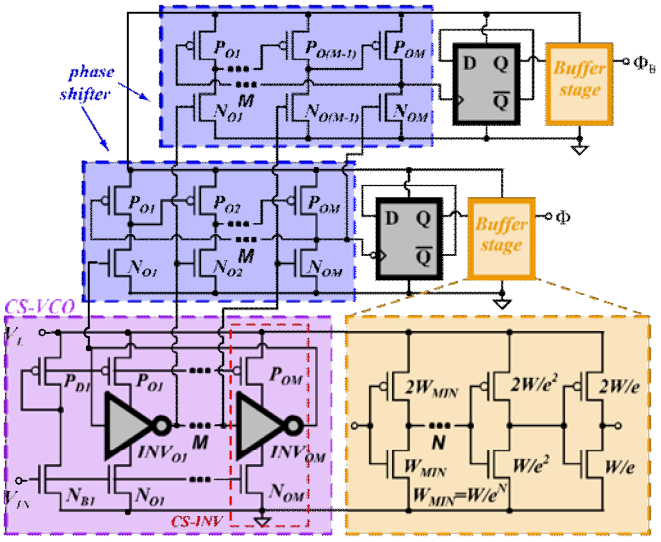

Fig. 6. Non-overlapping clock generator circuit.

V_{M8} or V_{M9} during the negative half cycle of , and their corresponding timing diagrams are shown in Fig. 5. Depending on comparator triggering, switching converter will connect either buffer stage or application stage. If $V_{DI\ V}$ is lower than $V_{RE\ F1}$ during the negative half cycle of , V_{M8} will trigger the M_8 transistor and V_{M9} will turn off both M_9 and M_{11} transistors, in order to maintain load regulation. Once the input energy meets the supply requirements, i.e., $V_{DI\ V} > V_{RE\ F1}$, M_8 will be turn off and $M_{9,11}$ will be turned on for storing the excess energy. Therefore, due to complementary switching between application stage and buffer stage, V_L is regulated and the remaining excess energy, is stored in the storage capacitor C_B , for future uses. Now, if $V_{DI\ V}$ is even lower than $V_{RE\ F2}$, that means, the scavenging energy is not sufficient to meet the load requirements, a control signal will trigger the M_{12} transistor, which will then allow the discharge of C_B to the C_L in order to mitigate any imbalances between available input energy and the output energy. In order to validate this idea, a system level simulation is carried out and a hardware setup

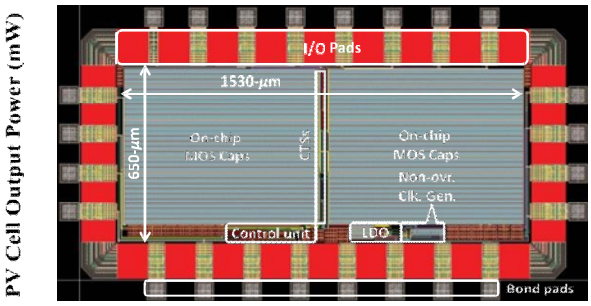

Fig. 7. Layout of the proposed power management interface circuit.

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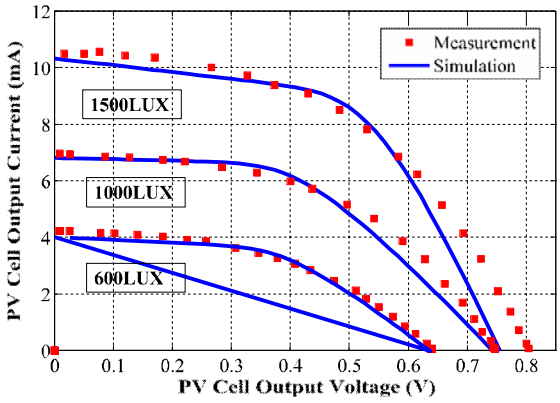

Fig. 8. Output current variation with respect to PV cell terminal voltage for three different light conditions.

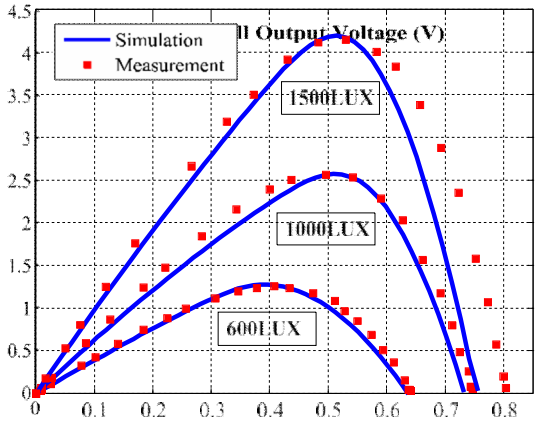

Fig. 9. Output power variation with respect to PV cell terminal voltage for three different light conditions.

is created using commercially available ICs, capacitors, and solar mini-panels and they are described in the next section.

IV. MEASUREMENT AND SIMULATION RESULTS

The proposed power management interface circuit is designed and simulated in 0.18-μm CMOS technology and its layout is shown in Fig. 7. The layout dimensions of the interface circuit is 1530 − μm×650 − μm and the major area of occupation is mainly due to the pumping capacitors. Post-layout simulations are carried out using standard foundry MOSFET models. The sizes of the power transistors (W/L) and pumping capacitors are chosen as 600μm/0.18μm and 500 pF, respectively. In order to suppress the input ripples, C_{IN} is chosen as 12 nF and to reduce the simulation time, buffer capacitor C_B and load capacitor C_L are chosen as 30 nF and 10 nF, respectively.

A. Photovoltaic Harvester

To emulate the PV cell in the simulation engine, an elec- trical equivalent model is used as an input energy source as shown in Fig. 5. To find the model parameters of this equivalent circuit, an experiment was conducted with two series-connected PV cells (Model 1-100, from Solar World Inc. [17]). A 40-Watt bulb is used as the light source and to emulate ambient variations, the position of the light bulb with respect the harvester is varied. In order to vary the load resistance, a standard potentiometer with the range of 0 − 10 K is used. Fig. 8 and 9 shows the output current and

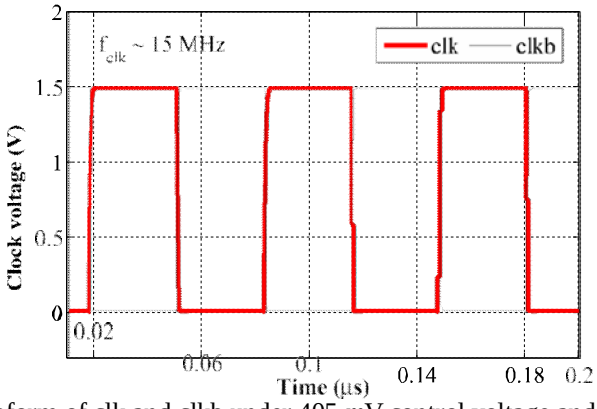

Fig. 10. Simulated waveform of clk and clkb under 405 mV control voltage and 1.5 V supply voltage.

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power variation with respect to PV cell terminal voltage for three different light conditions, 500 lx, 1000 lx, and 1500 lx, respectively. It may be noted that for a given light intensity, the output of solar cell behaves like a current source combined with a voltage limiter and at the transition point (where area under the curve is maximum), it offers maximum output power shown in Fig. 9. Now, from the slope of measured $I - V$ characteristic (dotted lines), one can calculate the equivalent series (R_S) and shunt (R_{SH}) resistances for the equivalent electrical model of a PV cell. The slope near to the open circuit voltage corresponds to the series resistance and the slope near to the short circuit current corresponds to shunt resistance. After fitting these parameters with appropriate short-circuit current, I_{SC} , and a number of diodes in the electrical model, simulation is carried out and the results are plotted in Fig. 8 and 9 (solid lines). There is a mismatch in the open circuit voltage at 1500 lx, but for an energy processing circuit, matching is important at the transition point, where the PV cell offers maximum power to the interface circuit.

B. Non-Overlapping Clock Generator

An array of five-stage (M = 5) current starved invert- ers (CS-INV) and two phase shifters are used to achieve the

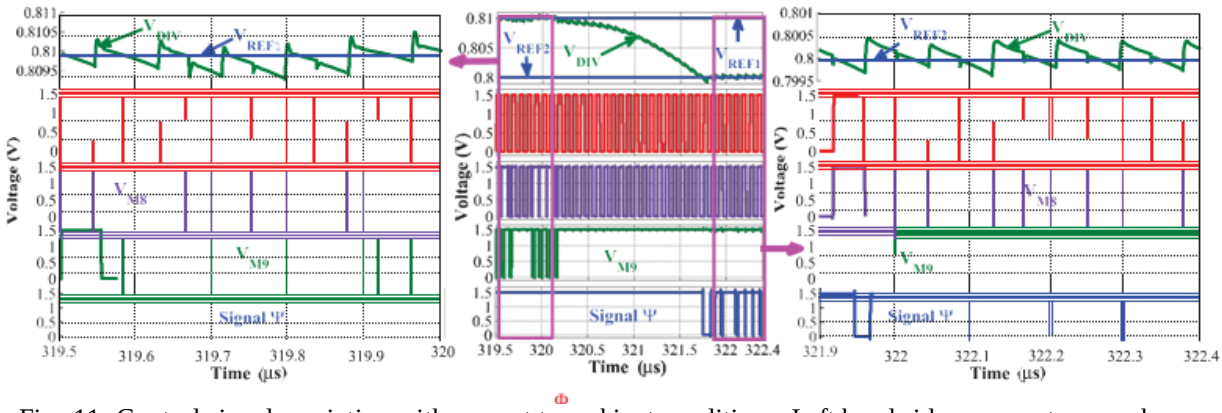

Fig. 11. Control signals variation with respect to ambient conditions. Left hand side represents enough ambient energy whereas right hand side represent insufficient ambient energy conditions [11].

desired clock frequencies for maximum power point. Voltages *VL* and *VI N* are used for power supply and for controlling the oscillation frequency, respectively. The (*W/L*) of *PD*1 and *NB*1 are kept at (0.36/0.18) μm and (*W/L*) of *PO*1 – *POM* and *NO*1 − *NOM* are kept at (1.80/0.18) μm and (0.90/0.18) μm, respectively. The (*W/L*) of PMOS and NMOS of CSINVs (*I NV*1− *I NVM*) are kept at (0.90/0.18) μm and (*W/L*) of *PP*1 − *PPM* and *NP*1 − *NPM* are kept at (0.72/0.18) μm and (0.36/0.18) μm, respectively, for this implementation. A reduced load clock load static master-slave register is used to realize *D* − *FF* [18]. To drive heavy loads, an array of progressively sized inverters are incorporated after the *D*− *FF* and their sizes are given in the figure itself, where, *W* represent the width of combined power transistors which are driven by the clock generator and *e* represents each stage efforts. A detailed discussion of progressive sizing inverters can be found in [16] and [19]. Fig. 10 shows the simulated waveform of the non-overlapping clock generator under supply voltage 1.5 V and control voltage 405 *m*V. The oscillation frequency achieved with this input condition is □ 15 *M*Hz, with a cost of 12.3 μW power consumption.

1 *C. Control Unit*

As the conventional bandgap reference circuit restricts its operation below 1.25 V, sub-threshold CMOS current reference circuit [20] has been chosen to generate reference voltages, *VREF*1 = 810 *m*V and *VREF*2 = 800 *m*V, for this implementation. The detailed operation of the reference generator and comparator circuits can be found in previous work [21]. Fig. 11 shows the output of the control unit under two different light conditions: when there is enough ambient energy to supply the load and when there is insufficient ambient energy to supply the load. During the negative half cycle of clock, if the sample voltage, *VDIV* , is higher than the reference voltage, *VREF*1, control signal *VM*9 will

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turn on *M*9 and *M*10 transistors, and *VM*8 control signal will turn off *M*8 transistor. On the other hand, if the voltage *VDIV* is lower than the reference voltage *VREF*1, control signal *VM*8 will turn on *M*8 transistor and turn off *M*9 and *M*10 transistors, respectively, to maintain the regulation. However, if the voltage

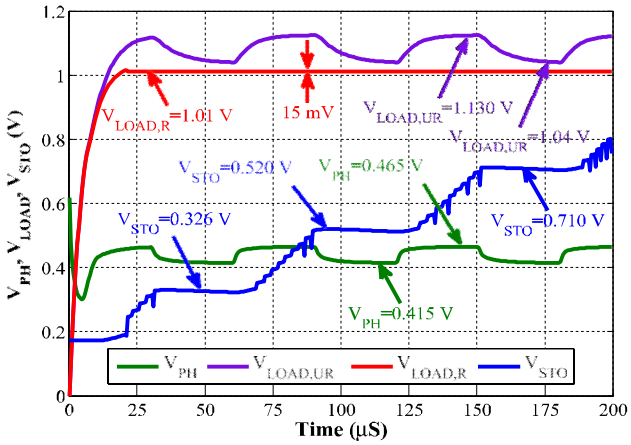

Fig. 12. Complete system simulation when there is enough ambient energy to supply the load.

VDIV is even lower than the second reference voltage *VREF*2, then the control signal will turn-on *M*11 and *M*9 transistors by the control signal _, to transfer the charges from *CB* to *CL* . Therefore, an appropriate triggering of the control signals are occurred to provide better load
regulation.

D. Complete System Simulation

After integrating all the individual components of energy processing circuit, a system level simulation is carried out to quantify its benefits. First, we have simulated the complete system under enough ambient energy and afterward have examined the behavior when there is insufficient ambient energy for a small period of time.

1) Under Enough Ambient Energy: In such a light condition, the system will utilize only a single DC-DC converter to maintain regulation at the load and the excess energy will be preserved in a storage capacitor *CB*. To emulate such varying light irradiance, the photocurrent, *ISC*, is varied fromemulate such varying light irradiance, the photocurrent, I_{SC}, is varied from 2.70 *m*A to 3.50 *m*A which corresponds light intensity 600 lx to 1000 lx, and corresponding variations of PV cell terminal voltage, energy storage voltage, and load voltage are presented

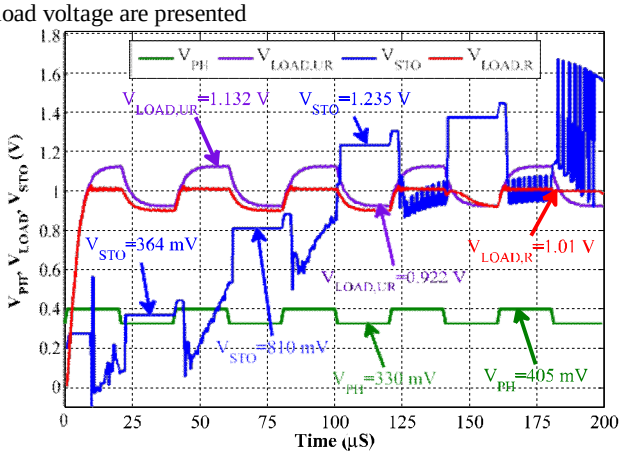

Fig. 13. Complete system simulation under sufficient and insufficient ambient energy to supply the load.

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Fig. 15. Conventional capacitor less low-dropout (CL-LDO) regulator.

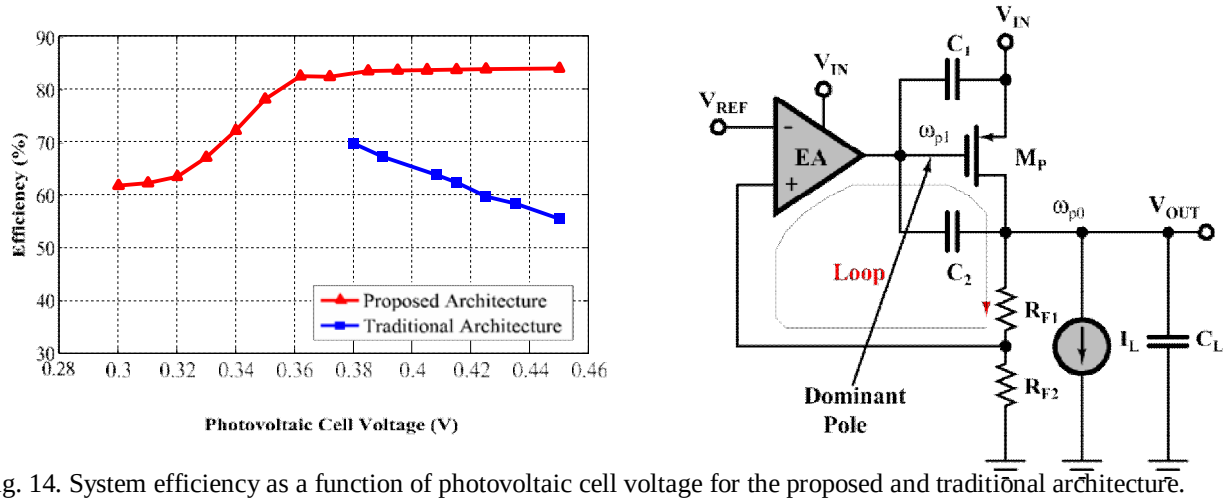

Fig. 14. System efficiency as a function of photovoltaic cell voltage for the proposed and traditional architecture.

in Fig. 12. For PV cell terminal voltages, (*VPH*), 415 *m*V and 465 *m*V, the unregulated load voltages (*VLOAD,UR*) reached are 1.04 V and 1.130 V, and regulated load voltage (*VLOAD,R*)
reached is 1.01 V, respectively. It took less than 20 μs to reach its steady state value for each light irradiance step. The proposed architecture will work properly once the photocurrent reached is above or equal to 2.70 *m*A, otherwise, the load voltage will goes below 1 V, and one may not be able to maintain the desired regulation at the load. Therefore, during this light condition, there will not be any excess energy that
can be stored in a rechargeable battery. On the contrary, when the photocurrent reaches 3.50 *m*A, which is more than enough to supply the load, and the excess energy will be stored in a storage unit for further use, as shown in Fig. 12.

2) Under Insufficient Ambient Energy: In this light condition, the proposed system will utilize the stored energy to maintain the load regulation. The variation of PV cell terminal voltage, energy storage voltage, and the regulated and unregulated load voltages are presented in Fig. 13. For PV cell terminal voltages 330 *m*V to 405 *m*V, the unregulated load voltage varies between 1.132 V to 0.922 V. Therefore, to maintain regulation at the load, one has to store the excess energy when *VPH* is 405 *m*V and utilize this energy when *VPH* is 330 *m*V. By doing so, one can achieve a regulated load

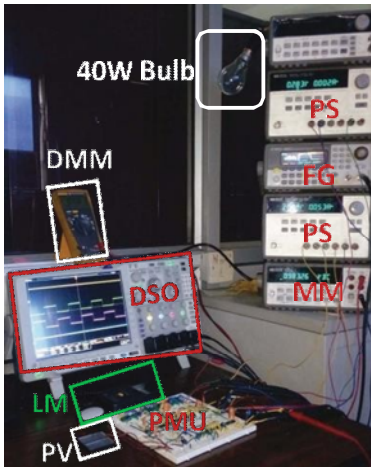

Fig. 16. Hardware setup for the proposed power management architecture. PV: Photovoltaic Cell; LM: Lux Meter; PMU: Power Management Unit; DSO: Digital Oscilloscope; DMM: Digital Multimeter; MM: Multimeter; PS: Power Supply; FG: Function

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generator.

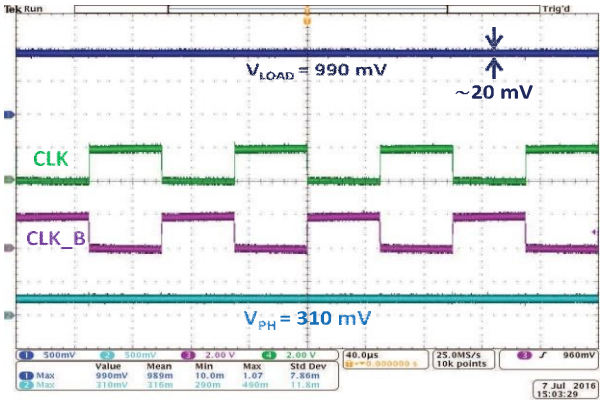
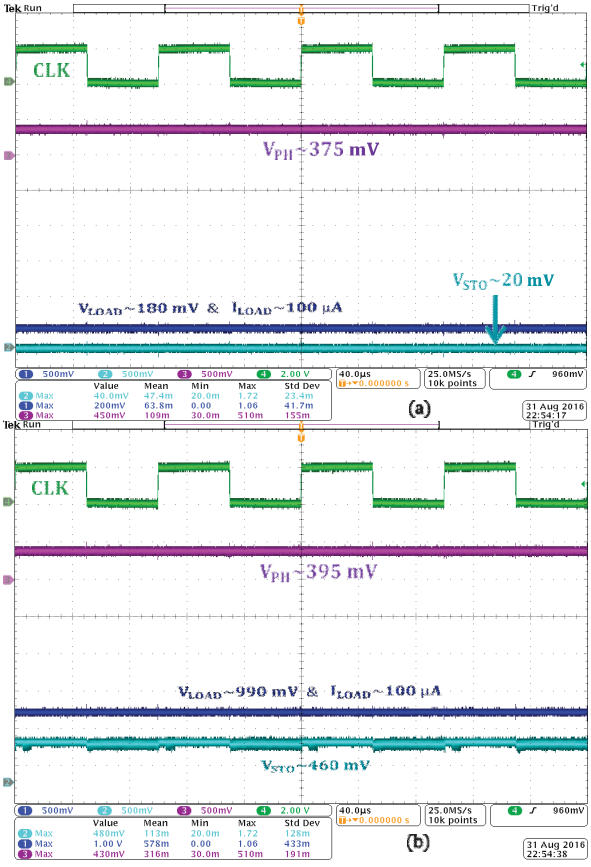


Fig. 17. Measurement results of PV cell terminal voltage (V_{PH}), non-overlapping clock signals (CLK and CLK_B), and no-load output voltage ($V_{LO\ AD}$) at 100 lx light intensity.

voltage, $V_{LO\ AD,R}$, of 1.01 V. The regulated voltage has only, 15 *m*V ripple, and one may reduce it further by minimizing opamp offset voltage.



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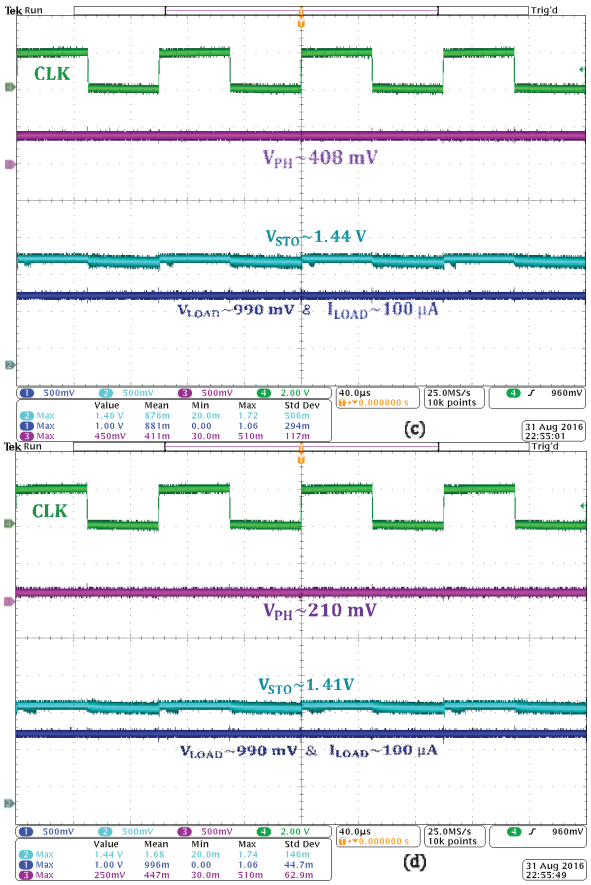

Fig. 18. Transient response when the light intensities varies from 100 lx to 330 lx: (a) initial stage, when the light intensity change from 100 lx to 330 lx, (b) after 21 sec, while maintained light intensity 330 lx, (c) after 44 sec, at 330 lx light intensity, and (d) when the light intensity changes from 330 lx to 100 lx.

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In order to calculate the effective system efficiency, one has to consider the power transfer loss due to both the control unit and the non-overlapping clock generator [22]. The power consumed by the clock generator at a supply voltage 1.5 V
is 12.3 μW, whereas, the control unit consume 18.3 μW at 15 *M*Hz clock frequency. Therefore, while calculating the net harvested power, one has to deduct these power from the output power. Fig. 14 shows the overall system efficiency as a function of PV cell terminal voltage of the proposed and traditional architecture. In order to calculate the overall system efficiency, average input power and average output power are taken into consideration as the ambient condition are changing with time [12]. Once the interface circuit provides regulation at the load, the overall efficiency of the system is calculated. The proposed architecture achieved a peak efficiency of 82.4% for input voltages higher than 365 *m*V. In order to compare with traditional power management architecture, a capacitor-less low-dropout regulator (CL-LDR) [23] has been incorporated (as shown in Fig. 15) in between the switching regulator and the load, and the buffer stage is eliminated from the architecture. The error amplifier (*EA*) is designed to achieve a voltage gain 40 dB and the W/L of the pass transistor (*MP*) is kept at (2000/1)μm to deliver a load of 1.01 *m*W with the supply voltage (*VI N*) of 1 V. The open loop AC response shows a voltage gain of 59.22 dB and a phase margin of 84°. The overall efficiency achieved after incorporating the CL-LDR is 69.7% as shown in Fig. 14, where, $\eta_{DC-DC,1}$ (switching regulator), $\eta_{DC-DC,2}$ (CL-LDR), and $V_{LO\ AD,UR}$ are 84%, 83.3%, and 1.01 V, respectively. As one move towards higher input voltage, the intermediate voltage ($V_{LO\ AD,UR}$) goes up and reaches 1.132 V for V_{PH} = 450 *m*V, and eventually the CL-LDR and overall system efficiency have degraded to 73% and 60%, respectively. Therefore, in comparison with proposed archi- tecture, the system efficiency has been improved by 12.7% for $V_{LO\ AD,UR}$= 1.01 V and 22.4% for $V_{LO\ AD,UR}$ = 1.132 V. Though the percentage of improvement depends on the ambient light intensities, one can expect at least 12% improvement for this implementation.

E. Experiment Results

In order to validate the proposed power management scheme, a hardware setup is created using commercially avail- able ICs, capacitors, and solar mini-panels as shown in Fig. 16. ICs ALD1103 [24], LM2903P [25], and HEF4071B [26] are used for MOSFETs, comparators, and OR gates, respectively. Three 1 μF capacitors and two 1000 μF capacitors are used for

TABLE I
PERFORMANCE COMPARISON AMONG STATE-OF-THE-ART POWER MANAGEMENT ARCHITECTURE FOR MICRO-SCALE ENERGY HARVESTING SYSTEMS

Parameters	Ghosh [29]	Dallago [30]	Shao [31]	Shih [32]	Sourav [33]	Chao [12]	This work
Technology node	0.50 μm	0.35 μm	0.35 μm	0.13 μm	0.35 μm	45 nm	0.18 μm
Energy source	solar	solar	solar	solar	solar	solar	solar
Light intensity	60 k-lx	600 W/m^2	1141 lx	60W bulb@12cm	1500 lx	2152 lx	600 lx
Input current and voltage to converter	I_{PH} = 50μA, V_{PH} = 550mV	I_{PH} = 8μA, V_{PH} = 560mV	I_{PH} = 286μA, V_{PH} = 2.74V	I_{PH} = 40μA, V_{PH} = 480mV	I_{PH} = 1.58mA, V_{PH} = 410mV	I_{PH} = 1.34mA, V_{PH} = 330mV	I_{PH} = 3.06mA, V_{PH} = 408mV
Load condition	2.81V@6.85μW	3.0V@2.9μW	4.4V@528μW	1.4V@11μW	1.88V@564μW	1.0V@170μW	1.0V @1.01mW
Converter type	IBC	IBC	CBC	CBC	IBC	CBC	CBC
Architecture	charger	two-stage	charger	charger	dual-path	charger	dual-path
MPP Voltage	not discussed	–	2.74V@ f_{MPP}=2.1MHz	–	0.410V@t_{CH},t_{DCH} =1.86μs,470ns	0.364V@ f_{MPP}=11MHz	0.408V@ f_{MPP}=15MHz
MPPT scheme	HC method	no scheme	HC method	no scheme	P&O method	NFC method	Inherent NFC
System efficiency	59%	65%	67%	58%	83%	40%	82.4%

IBC: Inductive boost converter; CBC: Capacitive boost converter; P&O: Perturb and observe; HC: Hill Climbing; NFC: Negative Feedback Control; t_{CH}: inductor charging time; t_{DCH}: inductor discharge time.

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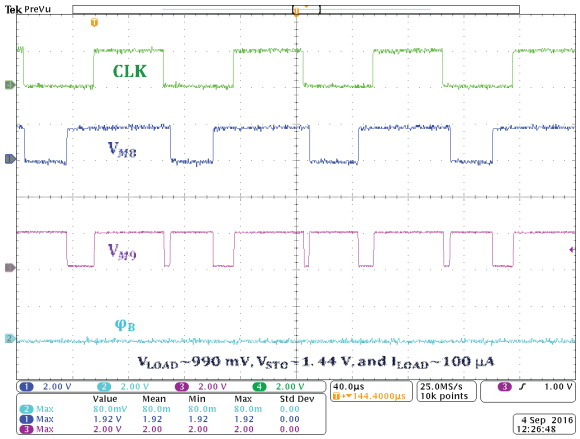

Fig. 19. Measurement of control signals at 330 lx light intensity.

charge transfer and storage, respectively. Two series connected mini solar panels (Model 1-100, from Solar World Inc. [17]) are used to convert light energy to electrical energy. A digital lux meter (Mastech MS6610 [27]) is used to measure the light intensity. For system clock, Agilent-33250A function genera- tor [28] is used and to generate non-overlapping clock signals phase shifter circuits are implemented using ALD1103 ICs. To represent ambient light energy, 40W light bulb is used for conducting the experiment. In order to vary the light intensity, the distance between the light bulb and solar panels are varied.

Fig. 17 shows the measurement results of PV cell termi-nal voltage (V_{PH}), non-overlapping clock signals (CLK and CLK_B), and no-load output voltage ($V_{LO\ AD}$) at 100 lx light intensity. Under this light intensity, V_{PH} offers 310 mV to the interface circuit and with the help of non-overlapping clock signals, the load voltage reached is 990 mV with ±

20 mV ripple. Once the load is connected (I_L □ 100μA), under this light intensity, $V_{LO\ AD}$ is settled down to zero because of the insufficient light intensity for powering the load. Fig. 18 captures four images when the light intensity varies back and forth between 100 and 330 lxes. Fig 18(a) shows the initial stage waveforms where the light intensity changes from 100 lx to 330 lx. As soon as the light intensity increases, V_{PH} reaches

□ 375 mV and the load voltage starts increasing from the 0 V.

Once the load voltage reaches □ 1 V, buffer voltage $V_{ST}\ O$ starts increasing as shown in Fig 18(b). The PV cell terminal voltage is increasing once the load voltage and buffer voltage approaches the final value as shown in Fig. 18(b) and (c). Because, initially the load capacitor was empty and the charge pump draws more current from the harvester, which eventually lowers the PV cell terminal voltage. Once the capacitor is charged, the load demand is reduced and eventually PV cell terminal current is reduced and the voltage is increased. After storing sufficient energy in the C_B , light intensity was changed from 330 lx to less than 100 lx. Under such a condition, V_{PH} has come down to □ 210 mV, which is not enough to maintain regulation at the load. In such a condition, the stored energy is utilized and the regulation is maintained at the load as shown in Fig. 18(d). Therefore, it is apparent from the measurement results that the proposed technique can maintain regulation at the load, irrespective of whether there is enough or not enough ambient energies to supply the load.

The measurement results of control signals at 330 lx and 100 lx light intensities are shown in Fig. 19 and 20, respectively. The 330 lx light intensity case represents enough ambient energy, whereas 100 lx light intensity represents a case in which ambient energy is insufficient to supply the load. At 330 lx light intensity, during the negative phase of clock, control signals V_{M8} and V_{M9} are generated alternatively to transfer the charge either to the load or to the storage unit, whereas the control signal $_B$ remains at logic zero states, which means that the ambient energy is enough to maintain regulation at the load. On the contrary, at 100 lx light intensity, during the negative phase of the clock, the control signals V_{M8} and V_{M9} are in logic zero and logic one state, respectively, whereas the control signal $_B$ changes its state alternatively during the phases of the clock. It indicates that the

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ambient energy is insufficient to supply the load and to maintain regulation it utilizes the stored energy.

Table I shows the performance comparison among the state-of-the-art power management architectures for micro-scale

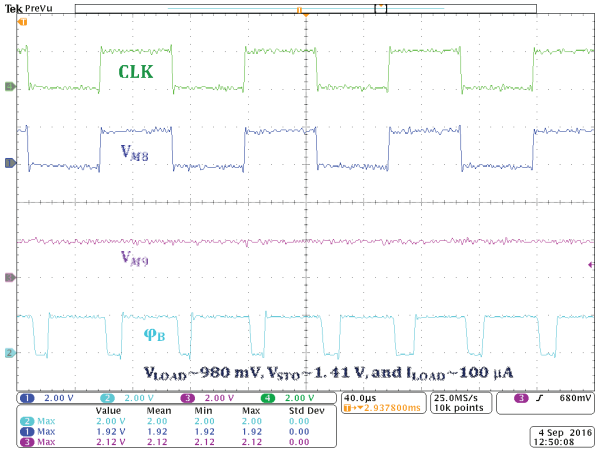

Fig. 20. Measurement of control signals at 100 lx light intensity.

solar energy harvesting systems. Among the capacitive boost converter, the proposed one has higher conversion efficiency and higher power delivery capability. Moreover, the proposed one has highest switching frequency which allows smaller component size and compact chip-area. Further, the proposed one has lower MPPT overhead as it utilizes inherent negative feedback loop for maximum power point tracking.

V. CONCLUSION

An efficient on-chip power management architecture for solar energy harvesting system is presented, which utilizes a single stage DC-DC converter when there is enough ambient energy for maintaining regulation at both the input and load. The proposed architecture utilized the stored energy to main- tain regulation when there is insufficient ambient energy to supply the load requirement. The proposed architecture avoids linear regulator and utilizes simple charge pump concept in order to maintain regulation. By utilizing a switching converter instead of a linear regulator, the proposed scheme achieved higher end-to-end efficiency. Simulation, as well as experi- mental result, are reported to validate the proposed idea.

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