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Positive Feedback Based Enhanced Gain Operational Amplifier in 45nm Technology

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ABSTRACT*:* A gain boosted operational amplifier designed using positive feedback technique is presented in this paper. In this design, a differential output differential amplifier merged with a single output differential amplifier is used so that positive feedback can be applied appropriately. The proposed Op-Amp is designed in 45nm CMOS process using 45nm spice library in HSpice tool. The simulation of proposed circuit results in 86dB gain, 268MHz UGB, 62 degree phase margin and 510µW power consumption.

KEYWORDS*:* CMOS Op-Amp; Positive Feedback; High Gain; 45nm Technology.

I. INTRODUCTION

Over the past years there had been a significant development in portable consumer electronic products. For ensuring portability of electronic devices the power consumption of the device should be low. Due to this reason in the modern world, there is an increasing need of circuit designs with low power consumption. But most of the times for low power consuming circuits the performance of the circuits also degrades. Hence, new improved designing techniques are required which can improve the performance of the circuit effecting the power dissipation of the circuit as little as possible.

In analog/mixed signal designs, Op-Amps are the fundamental cells. Operational Amplifiers are most commonly used for providing gain, but large bandwidth and low power dissipation are also desirable [1]. For analog circuits to be used in high precision application ultra high gain Op-Amps are required. As the MOS transistors are scaled down and the channel length reaches the sub micron levels, the low power consuming circuit designing becomes easy, but at the same time it becomes difficult to achieve high gain [2]. There are two main reasons for the difficulty in achieving high gain in submicron levels. First, the decrease in output resistance (ro) of MOSFET and second is the short channel effect [3]. However, many design techniques have been already reported for gain enhancement in submicron levels. There are four main ways to enhance the gain of an Op-Amp. First is to employ additional gain stages. But this method makes the designing and compensation process lengthy and complex. The second method use self-cascode or composite cascade structures. This method degrades the gain-bandwidth product and slew-rate of Op-Amp and most importantly limits the output swing. The third way to increase gain of an Op-Amp is to employ positive feedback technique. However, in order to achieve high gain using positive feedback, high level of transistor matching is required. The fourth way to boost the gain is cascading. But this method creates difficulty in frequency compensation of amplifier [4].

II. POSITIVE FEEDBACK

Adding positive feedback circuit in the differential amplifier of Op-Amp boosts the DC gain of the amplifier. Recently, as MOSFETs are being significantly scaled down, positive feedback circuits give a solution to enhance the small signal gain. One major problem associated with the application of positive feedback internally in Op-Amp is the possibility of instability and uncontrollability. However, an Op-Amp using positive feedback can be stabilized if it is designed properly while assuming that the open loop gain of the amplifier is small. The decrease in the maximum intrinsic gain (gmro) of a MOSFET due to its scaling helps maintaining stability when positive feedback is applied. Another problem associated with implementation of positive feedback is the strong dependence of gain of the Op-Amp on transistor matching. All of these problems are dealt with by properly selecting the W/L ratio and the compensation capacitor.

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When positive feedback is used internally for designing, a compensating conductance which is negative in nature is generated that boosts the amplifier gain [5, 6]. In most of the previously proposed structures a negative resistance is being generated from the feedback at output node of the amplifier that helps generating high open loop gain by compensating for some positive resistance at the output [7-9]. The initial implementation of the positive feedback in differential pair was implemented into a comparator [10]. Then this technique was used in a positive-feedback transconductance amplifier which was designed for applications in high-frequency range [11]. Several new designs for CMOS amplifiers were presented with very high open loop gain that used positive feedback techniques [12, 13]. A novel topology for differential pair positive feedback with improved transconductance gain was introduced [14] whose further improvement resulted in higher small signal gain [15]. But mostly these circuits were implemented as differential output circuits.

III.DIFFERENTIAL INPUT DIFFERENTIAL OUTPUT AMPLIFIER WITH POSITIVE FEEDBACK

The circuit in Fig. 1 uses positive feedback strategy. This circuit is a simple differential input differential output amplifier with positive feedback provided by the crosscoupled MOSFETs M3 and M4. The cross-coupled MOSFETs generate a negative conductance which is subtracted from the positive conductance, which in turn produces high open loop gain. The small signal model of the negative input side of the circuit is given in Fig. 2. From the small signal model, we can observe that the transconductance due to M4 opposes the transconductance of M1. Equivalently the variable current source in the model for M4 can be treated as a resistance with conductance G_m.

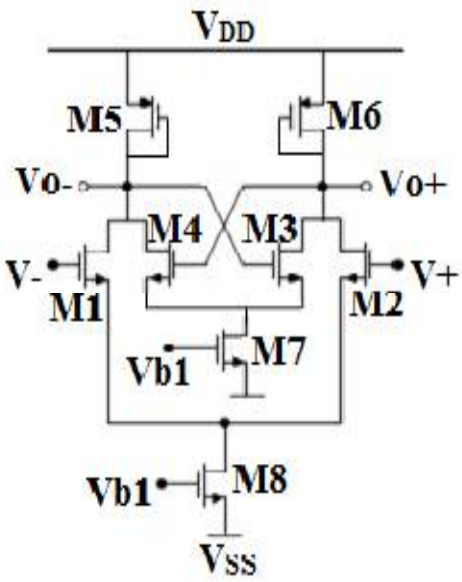

Fig. 1. Differential input differential output amplifier with positive feedback

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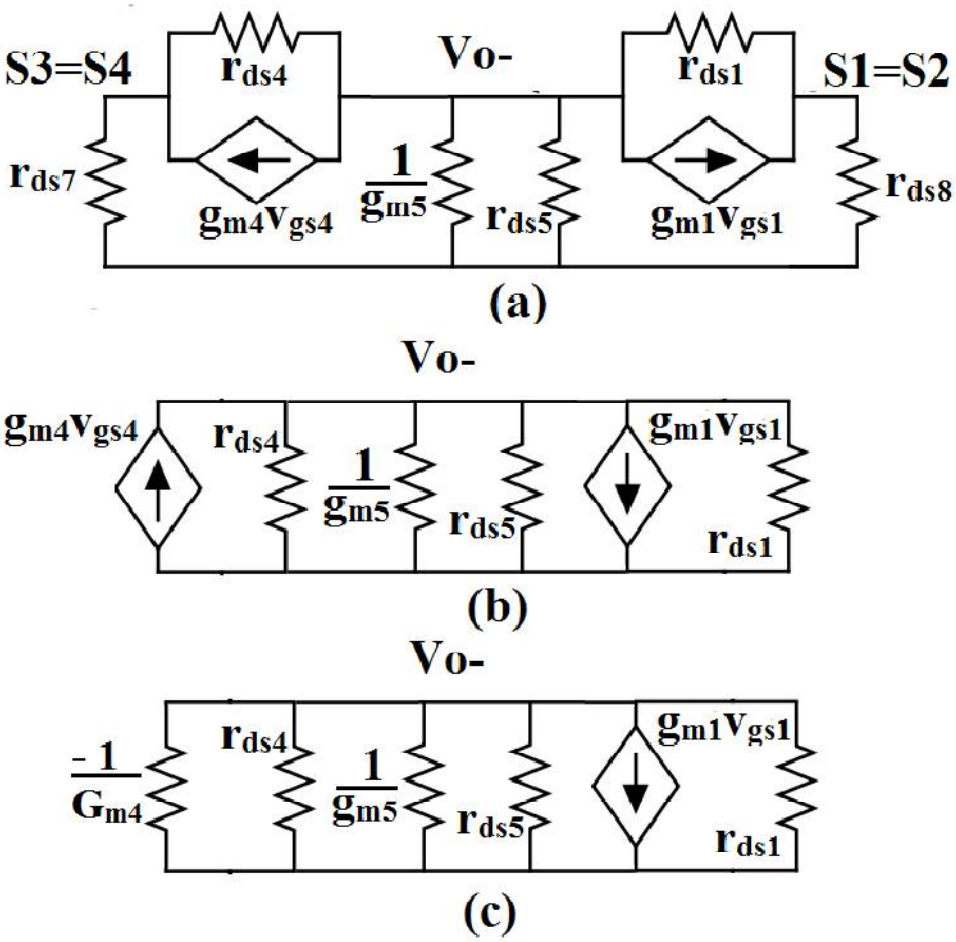

Fig. 2. Small signal model of the differential input differential output amplifier with positive feedback

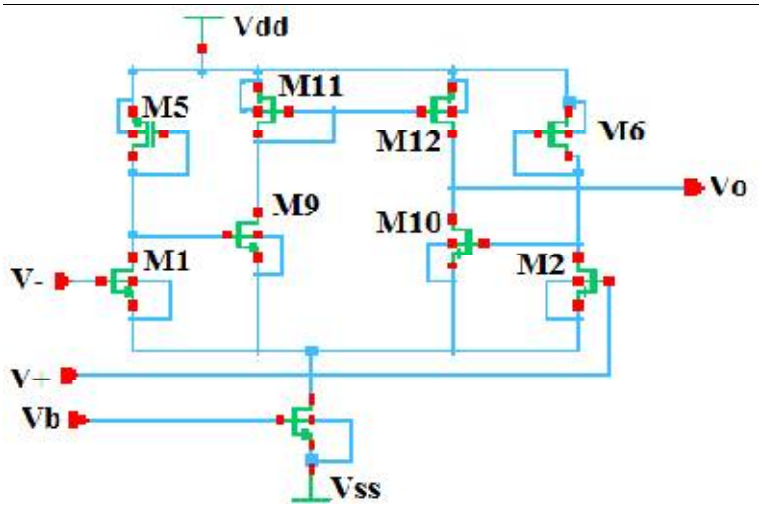

Fig. 3. Differential Output Amplifier Merged with Single Output Differential Amplifier

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IV. DIFFERENTIAL OUTPUT AMPLIFIER MERGED WITH UNBALACED DIFFERENTIAL AMP.

The circuit shown in Fig. 3 is a differential output amplifier merged with single output differential amplifier. In this amplifier the output from differential output differential amplifier is fed into a single output differential amplifier. This strategy not only converts the differential output into single output but also increases the gain of the differential amplifier. When applying positive feedback it is not possible to implement it directly in a single output differential amplifier as it may unbalance the amplifier output. So, a different approach is necessary to get a single differential output. The differential output amplifier merged with single output differential amplifier can be a solution to this problem.

V. PROPOSED CIRCUIT

The proposed Op-Amp circuit is designed using differential output amplifier merged with single output differential amplifier with positive feedback implemented within it as the differential stage. The schematic of the circuit is given in Fig. 4. In the circuit the positive feedback is provided using the transistors M3 and M4 along with the help of M7. It can be observed that the positive feedback is applied only in the differential output part of the differential amplifier.
The feedback is sensed from the node Vo- and Vo+, and with respect to these voltages current is drawn from the opposite node, which draws extra current from the circuit and increases the output voltage at these nodes.

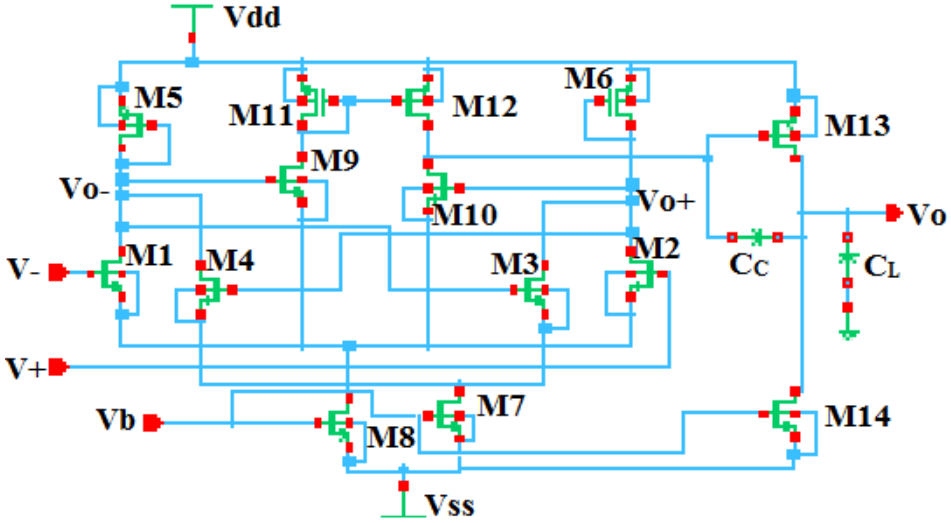

Fig. 4. Proposed circuit

VI. SIMULATION RESULT

The proposed Op-Amp given in Fig. 4 is designed in 45 nm CMOS technology and then simulated 45 nm spice library in HSpice tool. A power supply of ±1V, compensating capacitor (CC) of 150fF and load capacitor (CL) of 1pF was used for simulation purpose. The simulation of the circuit resulted in 86 dB DC gain, 268MHz bandwidth and 62 degree phase margin. The gain and phase plot of the proposed circuit is shown in Fig. 3. The power consumed by the circuit was 510Mw.
The proposed circuit has been compared with some of the previously reported circuits. It is quite easy to note that the proposed Op-Amp produces superior results in terms of gain and power consumption while maintaining the bandwidth in moderate levels. The DC gain and the UGB of the circuit are quite high considering the technology used and the power consumed by the circuit.

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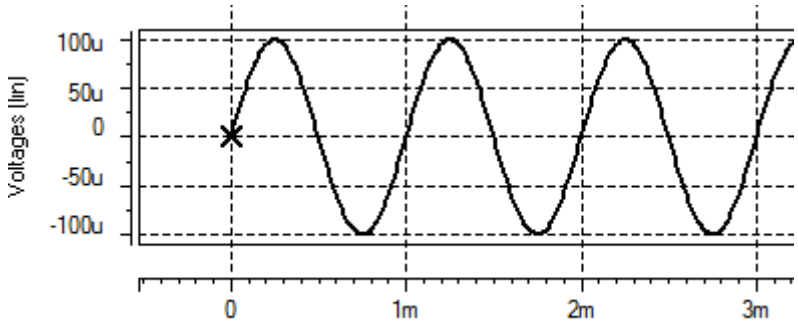

Fig. 1 Waveform of sinusoidal input signal

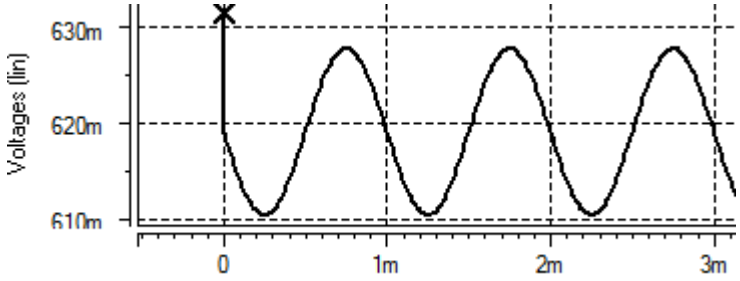

Fig. 2 Waveform of sinusoidal output signal

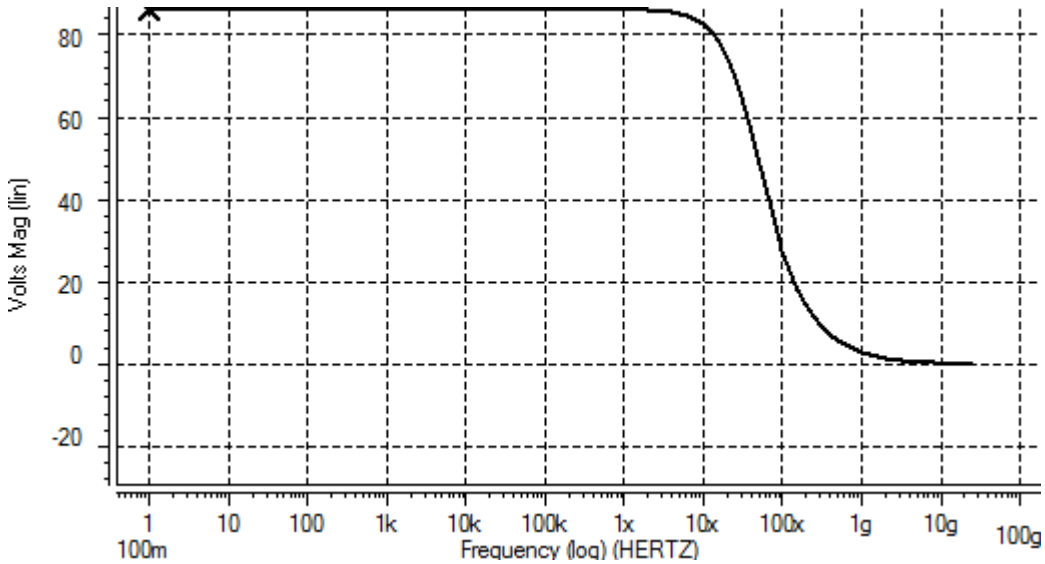

Fig. 2 Gain Vs Frequency plot of the proposed Opamp.

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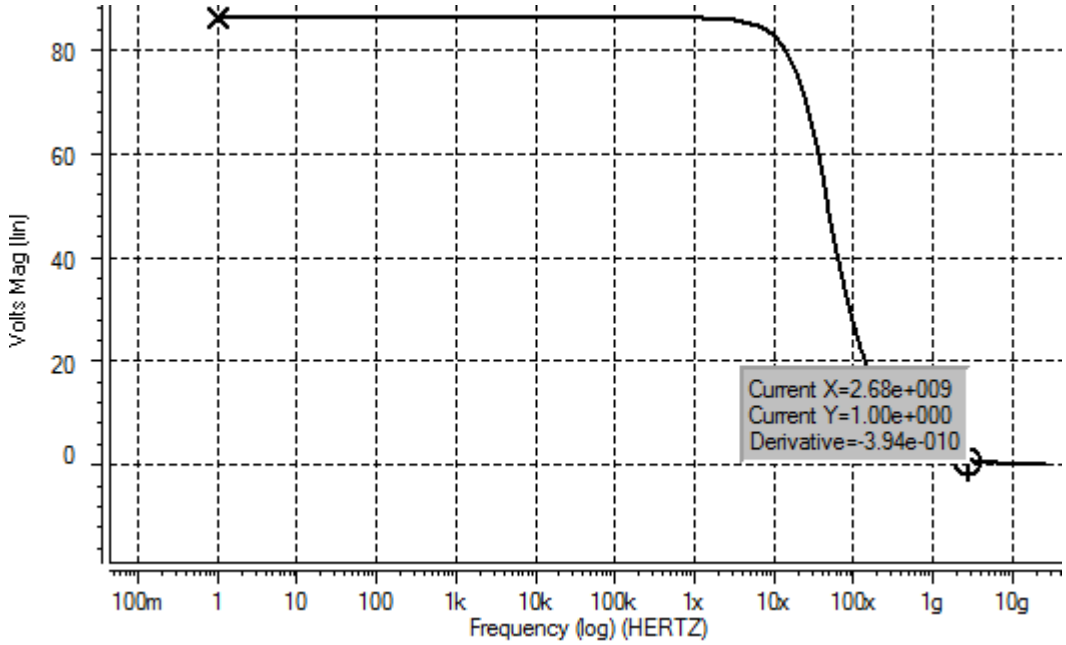

Fig .4 Unity Gain Bandwidth of the proposed Amplifier

VII. CONCLUSION

In this paper, a new approach has been presented for designing high gain amplifiers. The differential stage of the Op-Amp has been modified and the positive feedback strategy was successfully implemented for achieving this substantially high gain. An improved performance in terms of open loop gain is exhibited by the proposed circuit, which is evident from the comparison. On the down side of it, a high level of transistor matching is necessary for implementing positive.

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