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Design of Finfet Based 1-Bit Full Adder

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ABSTRACT: This paper proposes a 1-bit Full adder using Fin type Field Effect Transistor (FinFETs) at 250nm CMOS technology. The paper is intended to reduce leakage current and leakage power, chip area, and to increase the switching speed of 1-bit Full Adder while maintaining the competitive performance with few transistors are used. In this paper, we are designed a double-gate (DG) FinFETs and extracting their transfer characteristics by using Synopsys TANNER-EDA simulation tool. We investigate the use of Double Gate FinFET technology which provides low leakage and high-performance operation by utilizing high speed and low threshold voltage transistors for logic cells. Which show that it is particularly effective in sub threshold circuits and can eliminate performance variations with Low power. A 22ns access time and frequency 0.045GHz provide 250nm CMOS process technology with 5V power supply is employed to carry out 1-bit Full Adder of speed, power and reliability compared to Metal Oxide Semiconductor Field Effect Transistor (MOSFET) based full adder designs. Hence FinFET is a promising candidate and is a better replacement for MOSFET.

KEYWORDS: FinFET, Full Adder, Logic Styles, Tanner-EDA.

1. INTRODUCTION

In today's trend, any portable electronic devices like Laptops, mobiles, etc. should be smaller and smarter. Smaller device context in terms of cost and area, smarter device means, it should respond fast. there is an escalating number of portable applications with a limited amount of power available, requiring small area, low-power, and high throughput circuitry. Therefore circuits which consume low power become the major concern factor for the design of microprocessors and system components. The research effort in low power microelectronics has been intensified and low power VLSI systems have emerged as exceedingly in demand. The working principle is the same as that of planner MOSFET. The conventional bulk MOSFETs suffer from short channel effects at lower technology nodes due to the fact that as the source and drain regions are brought closer together, the drain region is better able to control the carriers in the channel than the gate.

Adder is one of the most important components of a central processing unit, Arithmetic logic unit (ALU), and floating point unit and address generation like cache or memory access unit. Low-power and high-speed adder cells are used in battery-operation based devices. As a result, the design of a high-performance full-adder is very useful and vital[1]. One of the most well known full adders is the standard CMOS full adder that uses 28 transistors as shown in Figure-1.

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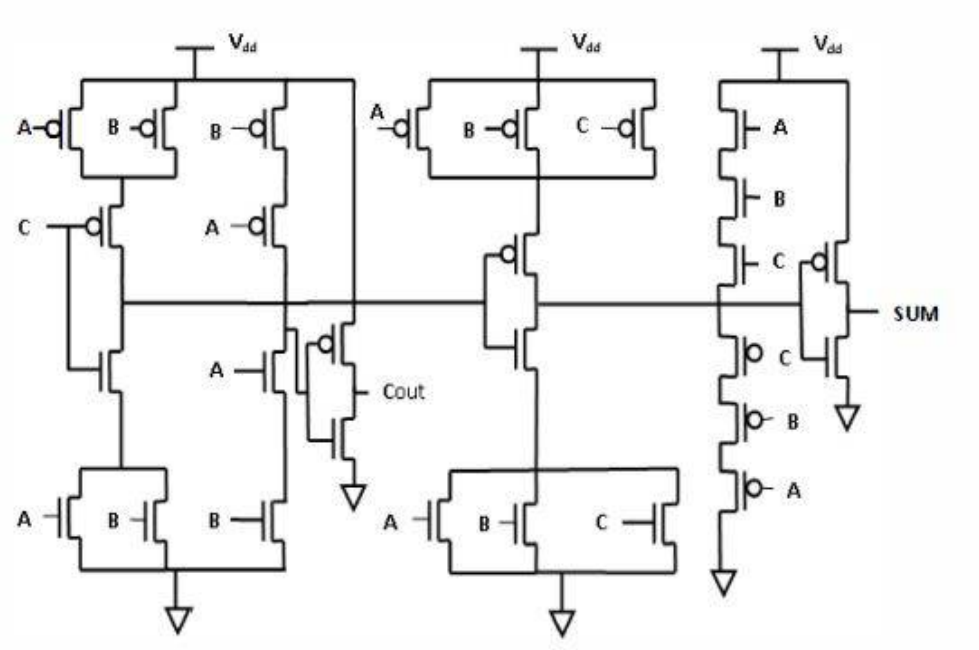

Figure 1.Schematic of conventional Full Adder

In this paper, we present a 1-bit full-adder circuit, which uses 10 transistors with suitable power consumption and delay performance. The basic advantage of 10 transistors full adders are-low area compared to higher gate count full adders, lower power consumption, and lower operating voltage[2]-[3]. It becomes more and more difficult and even outmoded to keep full voltage move backward and forward operation as the designs with fewer transistor count and lower power consumption are pursued. The basic disadvantage of the 10 transistors full adders are suffering from the threshold-voltage loss of the pass transistors. They all have double threshold losses in full adder output terminals. These drawbacks were overcome in this paper by applying Double gate FINFET technique to 10 Transistor 1-Bit full adder design. Double Gate FINFET has two electrically independent gates, which gives the circuit designer more flexibility in design[1]. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where the average power is in microwatts[5].

Full Adder Circuit Design

The addition is the most basic arithmetic operation and usually used in any digital electronic devices and arithmetic logic unit (ALU) to add any value of numbers. The commonly used adder cell is full adder where three inputs i.e. A, B and C_{in} will be added together to calculate the output of Sum and C_{out} [7]. The expression for Sum and C_{out} is given by:

$$\boldsymbol{Sum = A\ XOR\ B\ XOR\ Cin} \quad \text{..... (1)}$$
$$\boldsymbol{Cout = A.B + Cin\ .\ (A\ XOR\ B)} \quad \text{..... (2)}$$

Where the above Equations are generated from the truth table of 1-bit full adder as shown in Table 1

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Table-1: Truth Table of 1-bit full Adder

INPUTS			OUTPUTS	
A	B	CIN	SUM	OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FinFET

In a parallel transistor, there are two transistors with their source and drain terminals tied together. FinFETs were first introduced by Profs. Chenming Hu,Tsu-Jae King-Liu and Jeffrey Bokor at the University of California in 1999. Most chipmakers are currently developing technologies based on FinFET. These include IBM, Intel, TSMC, GlobalFoundries, SMIC, Qualcomm AMD, and Motorola. FinFETs are 3d structures that rise above the substrate and resemble a fin. The 'fins' form the source and drain, effectively and in this way, they enable more volume than a traditional planar transistor for the same area. The gate wraps around the fin, and this gives more control of the channel as there is sufficient length for the control. Also as the channel has been extended there is very little current to leak through the body when the device is in the 'off' state. This also allows the use of lower threshold voltages and it results in better performance and lower power dissipation. The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three sides of the fin or channel.

FinFET Structure

FinFET is non planar double gate transistor built on Silicon on Insulator (SOI) substrate. The important characteristics of the FinFET are that the conducting channel is enfolding by the thin silicon fin, which creates the gate device. The effective channel length of the device is determined by the thickness of the fin. It is called FinFET because the thin channel region stands vertically similar to the fin of a sandwich between the source and the drain regions. The gate covers around the body from three sides and therefore reduces the short channel effect (SCE). A parallel transistor pair consists of two transistors with their source and drain terminals tied together. The second gate which is added opposite to the traditional gate. Due to problems in aligning the front and back gates, as well as in buildings a low resistance to the back gate, DGFETs are difficult to fabricate.

The FinFET has been developed to overcome the problem faced by DGFET. Double gates for FinFETs provide effective control of the short channel effects. It can also be exploited to reduce the number of transistors for implementing logic functions [6].

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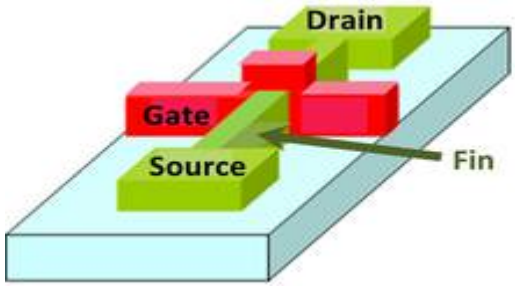

Figure. 2: FinFET Structure

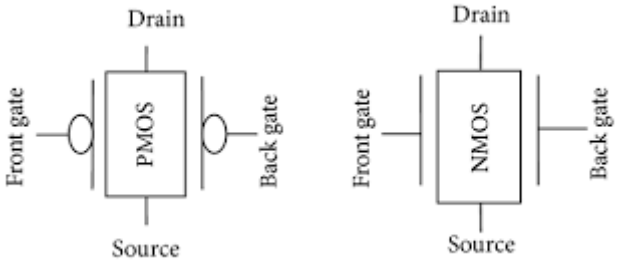

Figure. 3: FinFET Symbol

Complementary MOS Logic Style (CMOS)

Complementary MOS logic style is a combination of two networks; the Pull-up Network (PUN) and the Pull-down Network (PDN). The Pull-up Network consists of PMOS transistors and Pull down Network consists of NMOS devices. The function of Pull up Network is to provide a connection between gate output and Vdd, anytime the output of the gate is meant to be high. Similarly, the function of Pull down Network is to provide a connection between gate output and GND anytime the output of the gate is meant to be low. The Pull-up Network and Pull down Network are mutually exclusive to each other. The noise margin and propagation delay depends on the input patterns.

1-Bit Complementary MOS (CMOS) Full Adder

The CMOS full adder has 28 transistors in the design and it is the simplest implementation based on the above equations. The circuit of CMOS 1-bit full adder is as shown in Figure 4. This design has its advantages and disadvantages. The advantages include high noise margin is very reliable to low voltage. However, a high number of transistors may result in large power consumption, high input loads and requires larger Silicon area in a wafer. It also stated that this design may introduce more delay because Sum is generated from C_{out} as input as can be observed from Figure 4 and Figure 5.
Figure 4 shows a symmetric design which is called as CMOS-Bridge. This design generated Carry and Sum with 20 transistors, here using two inverters for improving the driving capability and produce Carry and Sum. The design uses 24 transistors. The output waveforms are following the truth table 1 of a full adder. Figure 6 shows a proposed symmetric design and implementation of Double-Gate Circuit with shorted gate mode which is called as FinFET Bridge. Full adder is a logical circuit with the three inputs (A, B and C_{in}) and two outputs that are called Sum and Carry. Full adder is one of the core for the arithmetic processors, Full adder is one of the cores for the arithmetic processors, therefore by increasing the performance of full adder thereby the performance of processors is also increased. The improvement in performance which thereby decreases propagation delay. This design generates $C_{\text{out}}$and Sum with 20 transistors, the use of two inverters is to improve the driving capability and produce Carry and Sum. Here also the design uses 24 transistors.

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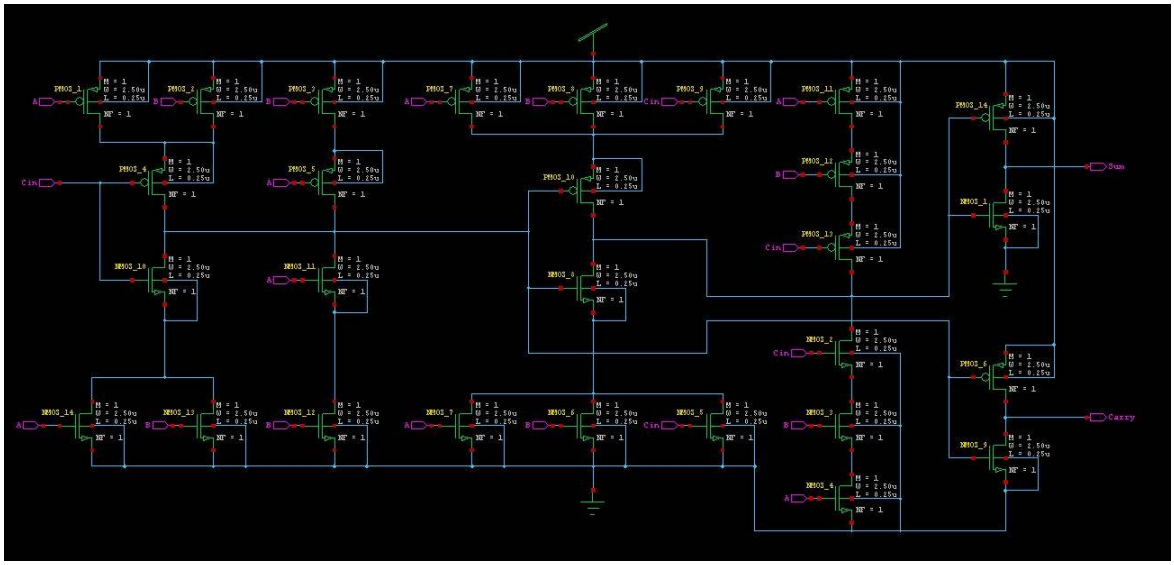

Figure-4 Schematic Diagram CMOS Full adder

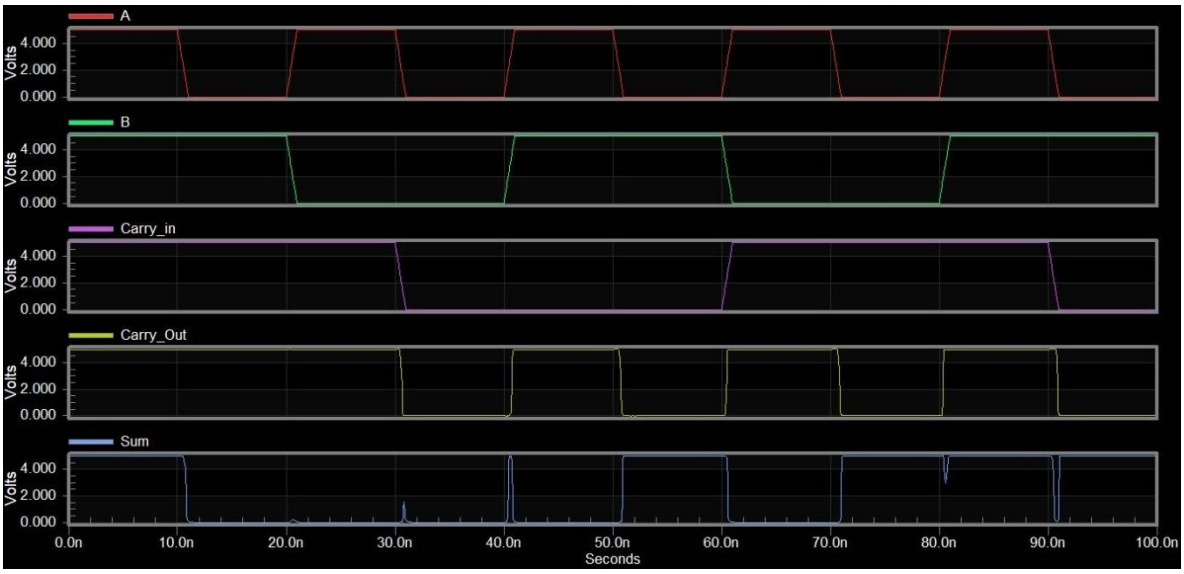

Figure 5. Simulation Result of CMOS Full adder

1-BIT FULL ADDER USING DOUBLE GATE FinFET

Double gate FINFET technique is applied on 1-Bit Full Adder cell. Here self-determining control of the front and back gate in Double-Gate (DG) can be efficiently used to develop performance and reduce power consumption. In non-critical paths, self-determining gate control can be used to join together parallel transistors. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. The second gate is added opposite to the conventional gate in Double-Gate (DG) FINFETS, which has been predictable for their prospective to superior control short channel effects, as well as to control leakage current. The operations of FINFET is recognized as short gate (SG) mode with transistor gates attached together, the independent gate (IG) mode, were self-determining digital signals are

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used to drive the two device gates, the low power and optimum power mode where the back gate is attached to a reverse-bias voltage to reduce leakage power and the hybrid mode, which employs an arrangement of low power and self-determining gate modes. In due to its base material the uninterrupted down in scaling of bulk CMOS creates key issues. The crucial obstacles to the scaling of bulk CMOS to 250nm gate lengths include short channel effects, optimum current, gate-dielectric leakage, and device to device variations. But FINFET based designs offer the superior control over short channel effects, low leakage and better yield in 250nm helps to overcome the obstacles in scaling The schematic of DG FINFET applied on 1-Bit Full Adder is shown in Figure 6.

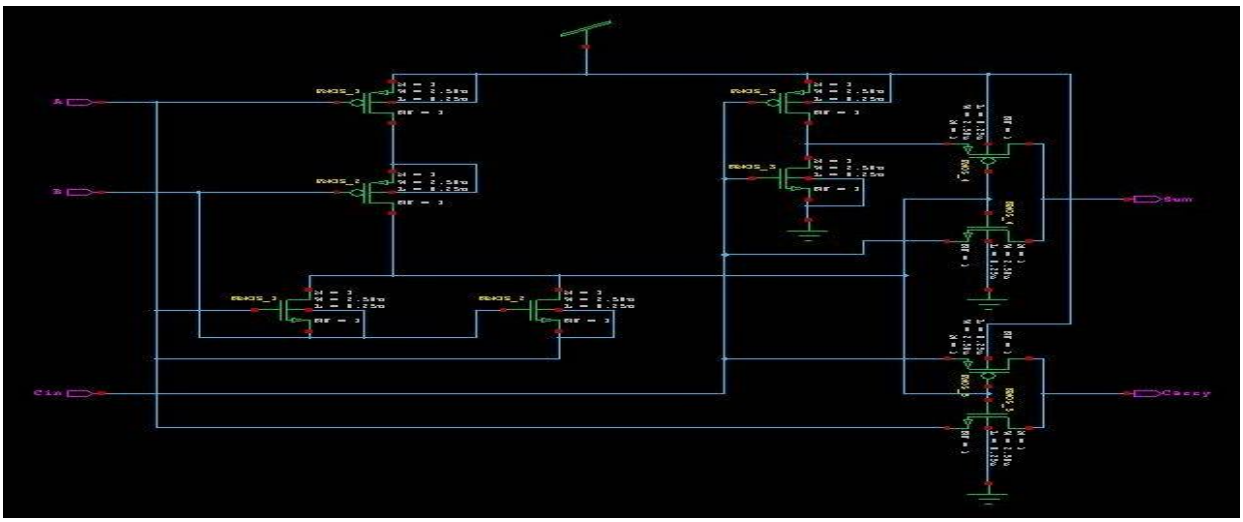

Figure 6. 1-Bit Full Adder using DG Finfet

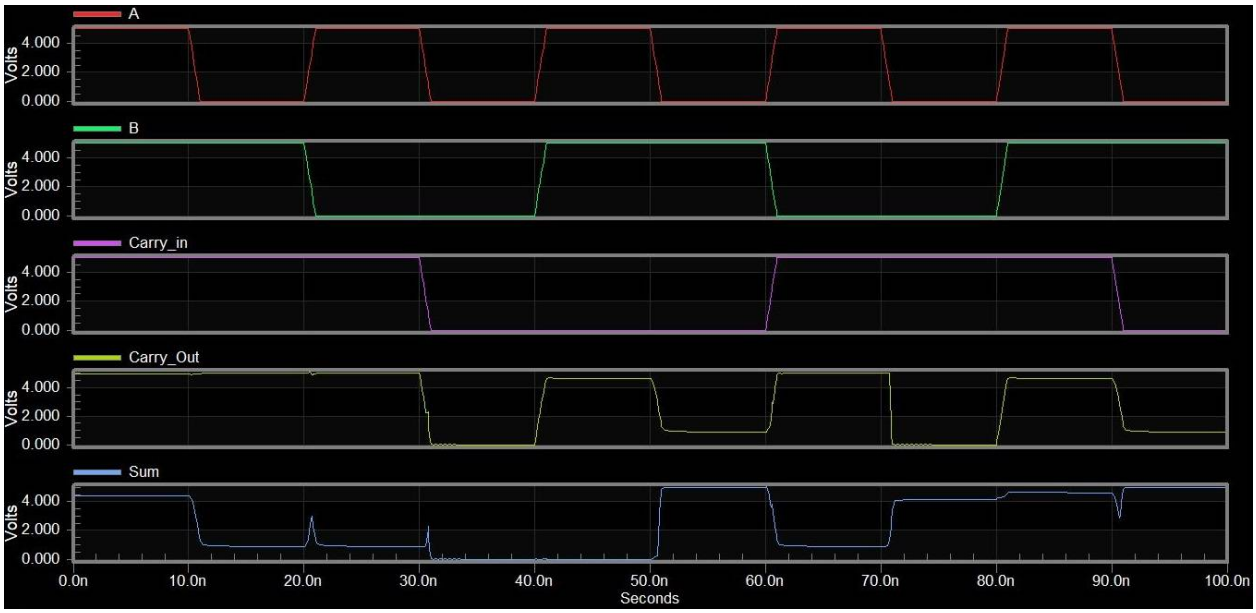

Figure7. Simulation Result of 1-Bit Full Adder using DG Finfet

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The output waveform of 1-Bit Full Adder using DG FinFET technique is shown in figure 7. Digital CMOS circuit may have three major sources of power dissipation namely dynamic, short and leakage power. Hence the total power consumed by every Adder can be evaluated using the following equation:

$$P_{tot} = P_{dyn} + P_{SC} + P_{leak}$$
$$= CLV_{dd}Vf_{clk} + I_{SC}V_{dd} + I_{leak}V_{dd} \quad \ldots\ldots\ldots\ldots (3)$$

Thus for low-power design, the important task is to minimize $CLV_{dd}Vf_{clk}$ while retaining the required functionality. The first term P_{dyn} represents the switching component of power, the next component P_{SC} is the short circuit power and P_{leak} is the leakage power. Whereas CL is the loading capacitance, Vf_{clk} is the clock frequency which is actually the probability of logic 0 to 1 transition occurs (the activity factor). V_{dd} is the supply voltage, V is the output voltage swing which is equal to V_{dd} but, in some logic circuits, the voltage swing on some internal nodes may be slightly less.
The current I_{SC} in the second term is due to the direct path short circuit current which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{leak} which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

II. SIMULATION RESULTS

A 1-Bit Full Adder based on DG FinFET technique has been proposed. The analysis of the simulated results confirms the feasibility of the DG FinFET technique in full adder design and shows that there is a reduction of 25 to 30 percent in the value of power dissipation parameter as
compared to CMOS technique at a supply voltage of 5V. DG FinFET adders have a marginal increase in area compared to the CMOS adders, we achieved the lowest power dissipation. The simulation result is measured by TANNER EDA Tool. The Simulation result is summarized in Table 2.

Table 2: Simulation Results Summary

Parameters	1-bit Full Adder	FinFET based Full Adder
Technology Used	250nm	250nm
Supply Voltage	5v	5v
Frequency Used	0.045GHz	0.045GHz
Access Time	22ns	22ns
Delay	10.31ns	9.73ns
Efficiency	52.3%	96.56%
Leakage Power	2.30nW	0.31nW
Leakage Current	52.1Pa	34.5pA
Optimum Current	8.21uA	3.16uA
Optimum Power	0.55Mw	0.15mW
Dynamic Current	0.05Na	0.03nA
Dynamic Power	3.30nW	0.61nW
Operating Power	1.84Mw	9.76mW
Operating Current	0.28Ma	0.23mA

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III. CONCLUSIONS

We have experimentally investigated the device performance and parameters such as operating current, operating power, leakage current, leakage power, optimum current and optimum power transistor count. The previous techniques have a disadvantage of the transistor count and the power dissipation. The current work progresses the design of a 10T full adder using FinFET in which extremely low power dissipation is observed and also the transistor count is low. In this paper 1-Bit, Full Adder using FinFETs has been proposed. The simulations were carried out using Tanner EDA At 250nm technology. The simulation results are shown in Table 2, and can be seen that the proposed adder offers improved result. Thus the different types of full adders have been studied and comparison of different full adders in terms of power and number of transistors in various technologies were done. Based on this comparison, 10T full adder is the best power consuming adder. The transistor count is also very low compared to others. This adder is suitable for VLSI applications with very low power consumption. Due to the reduction in a number of transistors, switching activity is reduced. We have also calculated Duty cycle is 96.56 % which is about 2 times greater than CMOS 1-Bit full adder cell.

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