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An Ultra-low power Subthreshold Bandgap Reference without using Resistors

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ABSTRACT: This paper proposes an ultra-low power Bandgap Reference (BGR) operating in the subthreshold region. The proposed design contains no resistors and operates at a supply voltage below 1V. The BGR circuit consists of a biasing circuit, a Proportional to Absolute Temperature (PTAT) generator and a Complementary to Absolute Temperature (CTAT) generator based on diode-connected MOSFET. The PTAT generator is based on the Self-Cascode MOSFET (SCM) structure. The circuit was designed and simulated in a standard 90nm CMOS process. The circuit produces an output reference of 397.6mV at 27°C with a supply voltage of 0.9V. The BGR operates over a temperature range of -50°C to 80°C with a temperature coefficient(TC) of 16ppm/°C. The circuit consumes a power of 20.781nW.

KEYWORDS: Subthreshold, Bandgap Reference (BGR), Low power, Resistor-less, low temperature coefficient

I. INTRODUCTION

The need for low power design has increased tremendously owing to the decrease in chip size and increasing complexity. Power dissipation has become a crucial deciding factor in the design process. As the technology size decreases, the chip density increases and the power consumption increases. The supply voltage and current should be scaled down to reduce the power dissipation. Low power circuits are widely used in portable and battery-operated systems, wireless sensors, energy harvesting systems etc.

A voltage reference circuit is an important component of analog and mixed-signal circuits, like comparators, Opamp, Linear Dropout Regulators, Phase Locked Loop, Analog to Digital Converters etc. A Bandgap Reference is an example of a most widely used voltage reference circuit. The reference output should be stable with respect to temperature, process, supply variations and circuit loading. Low power applications make use of BGR operating in the subthreshold region.

A Bandgap Reference circuit is designed by summing a PTAT voltage with a CTAT voltage in the appropriate ratios. A PTAT source has a Positive Temperature Coefficient (PTC) and its output increases with increase in temperature. A CTAT source has a Negative Temperature Coefficient (NTC) and its output decreases with increase in temperature. A Bandgap Reference works by cancelling the PTC and the NTC resulting in an average value of zero TC. Thus, the BGR circuit works by cancelling the opposing variations in temperature.

II. LITERATURE SURVEY

A voltage reference has multiple consideration factors, including power consumption, area, temperature coefficient, line sensitivity and power supply rejection ratio (PSRR). A standard BGR circuit consists of an Opamp circuit, which will however produce an offset voltage and affect the output. An offset insensitive, low power BGR is presented in [1]. It achieves a PSRR of -43dB by using a current-buffer based compensation technique.

A BGR with inherent curvature compensation and low TC of 10ppm/°C is proposed in [3], which however has a power consumption of 576nW at room temperature. A high precision BGR with second order curvature compensation and a TC of 10ppm/°C is proposed in [6]. However, it operates at a high supply voltage of 5V, with a current consumption of 5uA. A sub-1V, low power, high PSRR BGR is proposed in [7], which uses self-supply regulated feedback to achieve

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better Line sensitivity. An all-in-one bandgap voltage and current reference is proposed in [8] with a low power consumption of 9.3nW. However, the current reference has a high TC of 283 ppm/°C as opposed to voltage reference TC of 26 ppm/°C.

Resistors are normally used in BGRs to generate the bias current and set the operating point, and to control the temperature coefficient of the output voltage. However, large resistors must be used to achieve a low bias current in the order of nano-amperes. This leads to increased power dissipation, noise and chip area. Hence resistor-less BGRs are preferred for ultra-low power applications. A resistor-less BGR with improved PTAT generator is proposed in [2], which adds two Bipolar Junction Transistors (BJT) in the input stage to improve the TC. A sub-1V low power BGR based on SCM is proposed in [4], which uses a nano-ampere current reference circuit and has a low TC of 13 ppm/°C. In [5], a temperature compensated, self-biased reference with native NMOS is proposed, which has a TC of 105 ppm/°C. A MOSFET-only BGR with TC of 34ppm/°C is proposed in [9]. A picowatt, subthreshold voltage reference based on SCM is proposed in [10].

This paper proposes a sub-1V low power BGR based on the SCM structure. The circuit consists of no resistors and a single Bipolar Junction Transistor (BJT) in the biasing circuit, thereby reducing power dissipation and area.

III. METHODOLOGY

A transistor is said to operate in the subthreshold or weak inversion region when its Gate-to-Source voltage V_{GS} is less than the Threshold voltage V_{TH}. The corresponding current between the source and drain terminals is called the subthreshold drain current or the subthreshold leakage current. This region of operation is widely used in design of low power analog circuits, unlike in digital circuits where it is considered an off state.

The current in a MOSFET mainly consists of two components: drift current and diffusion current. The drift current mainly flows in the strong inversion region, due to the lateral electric field. In the subthreshold region, the current flow is due to the diffusion of minority charge carriers. The subthreshold current has an exponential dependence on V_{GS}.
The drain current of a MOSFET in subthreshold region is given by

$$I_D = \mu C_{ox} K(\eta - 1) {V_T}^2 \, exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

where K is the aspect ratio of the MOSFET, μ is the carrier mobility, Cox is the gate-oxide capacitance, V_T = kT/q is the thermal voltage, (K is the Boltzmann constant, T is the absolute temperature, and q is the electron charge) and η is the subthreshold slope factor.
For $V_{DS} > 4V_T$, the last term becomes nearly equal to 1. The current I_D is almost independent of V_{DS}, and is given by

$$I_D = \mu C_{ox} K(\eta - 1) {V_T}^2 exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right)$$

The value of slope factor η is given by

$$\eta = 1 + \left(\frac{C_D}{C_{ox}}\right)$$

where C_D and C_{OX} are the depletion-layer and gate-oxide capacitances respectively.

$$\eta = 1 + \left(\frac{C_D}{C_{ox}}\right) \text{ and } \eta = 1 + \left(\frac{C_D}{C_{ox}}\right)$$

where ε_{si} and ε_{ox} denote the dielectric constants of silicon and oxide respectively, W_d is the width of the depletion layer and t_{ox} is the thickness of the gate-oxide layer. The value of η lies between 1 to 2, depending on the process and biasing.

The block diagram of a generic BGR circuit is shown in Fig. 1. The BGR circuit consists of a biasing circuit, a PTAT generator, a CTAT generator and a summing block. The biasing circuit provides the necessary voltage/current bias and helps in establishing the operating point. The PTAT generator produces a PTAT voltage, which is then summed with the CTAT voltage from the CTAT generator in the appropriate ratio. This results in a low TC output voltage, which is independent of temperature variations.

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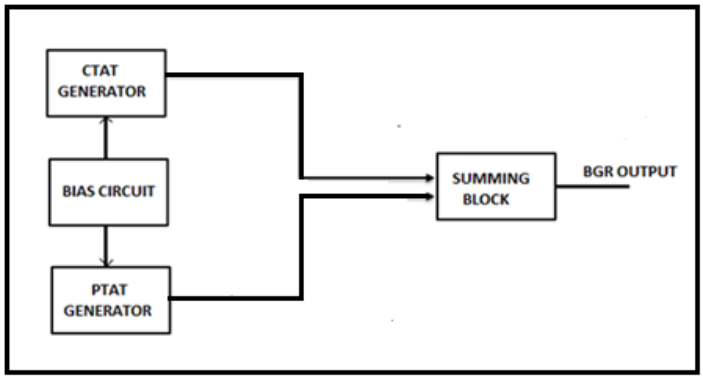

Fig 1 Block Diagram of a Generic BGR circuit

The biasing circuit provides a suitable voltage or current bias to the PTAT and CTAT generators. The biasing circuit helps in setting the operating point of the circuit. In a traditional BGR circuit, resistors are used to generate the bias current. However, the bias current of subthreshold circuits ranges in the order of nano-amperes and requires large value of resistors, which in turn increases the power dissipation and chip area. Thus resistor-less BGRs are used with self/external biasing.

The biasing circuit with a single bipolar transistor is shown in Fig. 2. The voltage across the diode-connected PNP transistor is divided among the transistors M3-M5 [4]. The V_{DS} of M5 is provided as the bias voltage to the core circuit.

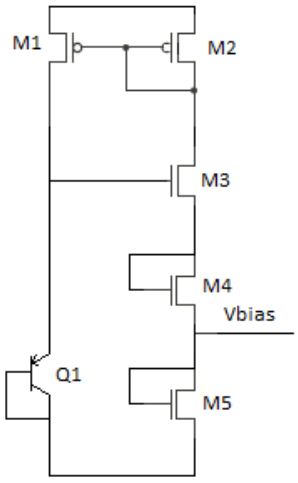

Fig 2 Biasing Circuit

A PTAT voltage is normally generated by taking the voltage difference between two PN junctions. The standard Self-Cascode MOSFET structure is used for the generation of the PTAT voltage[4,11,12]. The SCM PTAT generator used in the proposed BGR is shown in Fig.3.

In the SCM structure, both the transistors operate in the subthreshold region. The output voltage of this circuit is taken across the drain-to-source voltage of the bottom transistor and is given by the difference in gate-to-source voltages of the two transistors.

$$V_{OUT} = V_{GS2} - V_{GS1} = \frac{nkT}{q} ln\left(\frac{I_2}{I_s}\left(\frac{L}{W}\right)_2\right) - \frac{nkT}{q} ln\left(\frac{I_1}{I_s}\left(\frac{L}{W}\right)_1\right)$$

$$V_{OUT} = nV_T \ln\left(\frac{I_2}{I_1} * \frac{K_1}{K_2}\right),$$

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where K1 and K2 are the aspect ratios of M1 and M2 respectively, and V_T is the thermal voltage. The output voltage is directly proportional to the absolute temperature and behaves like a PTAT voltage.

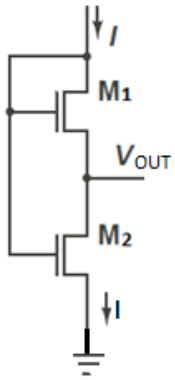


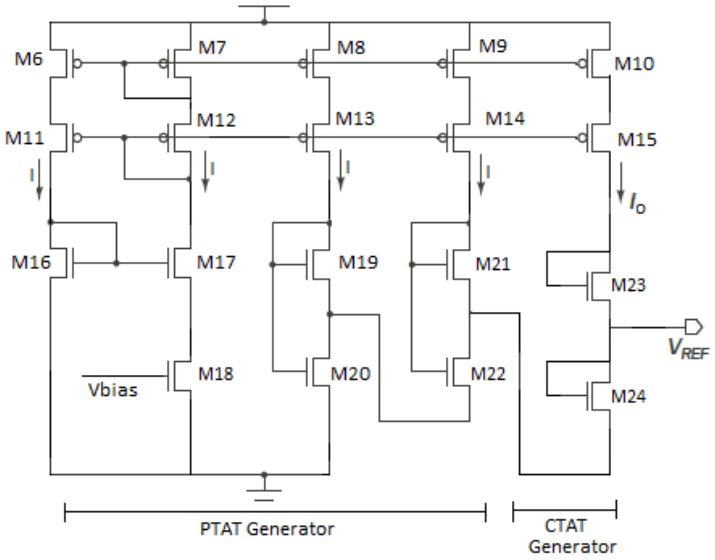
Fig 3 SCM PTAT Generator

The CTAT voltage is normally generated from the gate-to-source voltage V_{GS} or base-to-emitter voltage V_{BE} (in case of a bipolar transistor). The V_{GS} of a MOSFET operating in the subthreshold region is given by

$$V_{GS} = \eta V_T \, ln\left(\frac{I_D}{\mu C_{ox} K(\eta - 1){V_T}^2}\right) + V_{TH}$$

Differentiating V_{GS} with respect to temperature gives a voltage with negative temperature coefficient. This is due to the negative dependence of threshold voltage w.r.t temperature. A diode-connected MOSFET is used as the CTAT generator in the proposed circuit.

The schematic of the proposed subthreshold BGR is shown in Fig. 4. The circuit mainly consists of a PTAT and a CTAT generator. The resistors in the traditional BGR are replaced by MOS-resistors M18 and M23. The MOSFET M18 is biased to produce a bias current of 3nA. The reference current is mirrored to the other branches using PMOS current mirrors M6–M15.
The PTAT voltage is generated by cascading two SCM structures, comprising of MOSFETs M19–M22. The CTAT voltage is generated by the diode-connected MOSFET M24.



- Fig 4. Schematic of the Proposed BGR

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The temperature compensated output voltage is given by

$$V_{REF} = V_{GS20} - V_{GS19} + V_{GS22} - V_{GS21} + V_{GS24}$$

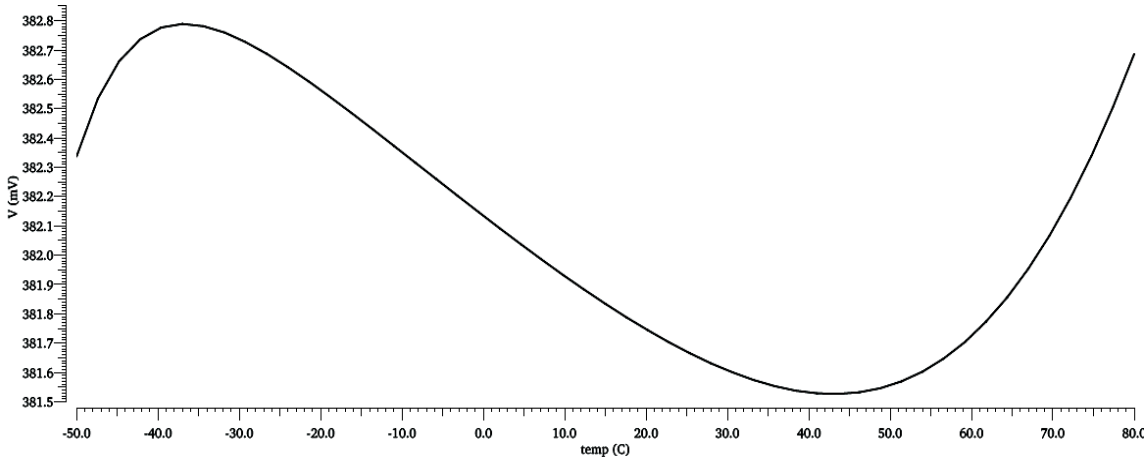
$$V_{REF} = nV_T ln\left(\frac{I_{20}}{I_{19}} * \frac{K_{19}}{K_{20}}\right) + nV_T ln\left(\frac{I_{22}}{I_{21}} * \frac{K_{21}}{K_{22}}\right) + V_{GS24}$$

$$V_{REF} = nV_T ln\left(\frac{I_{20}}{I_{19}} * \frac{I_{22}}{I_{21}} * \frac{K_{19}}{K_{20}} * \frac{K_{21}}{K_{22}}\right) + V_{GS24}$$

The negative temperature coefficient of CTAT voltage is compensated by choosing appropriate aspect ratios of MOSFETs M19–M22.

IV. RESULT AND DISCUSSION

The circuit was simulated in a standard 90nm CMOS process. The circuit produces an output reference of 381.63mV at room temperature. The BGR operates over a temperature range of -50°C to 80°C, with maximum variation of 1.23mV. The plot of output voltage versus temperature is shown in Fig. 5.



- Fig 5 Variation of BGR output w.r.t Temperature

The value of Temperature Coefficient is calculated[12] as

$$T.C. = \frac{\Delta V_{REF}}{\Delta T * V_{REFNOM}}$$

where ΔV_{REF} is the change in V_{REF}over a temperature difference of ΔT, and V_{REFNOM} is the nominal V_{REF} at room temperature.

The circuit draws a current of 12nA from a 0.8V supply. This leads to a power consumption of 9.624nW at 0.8V supply at room temperature. The variation of output voltage over supply voltage range is shown in Fig. 6.

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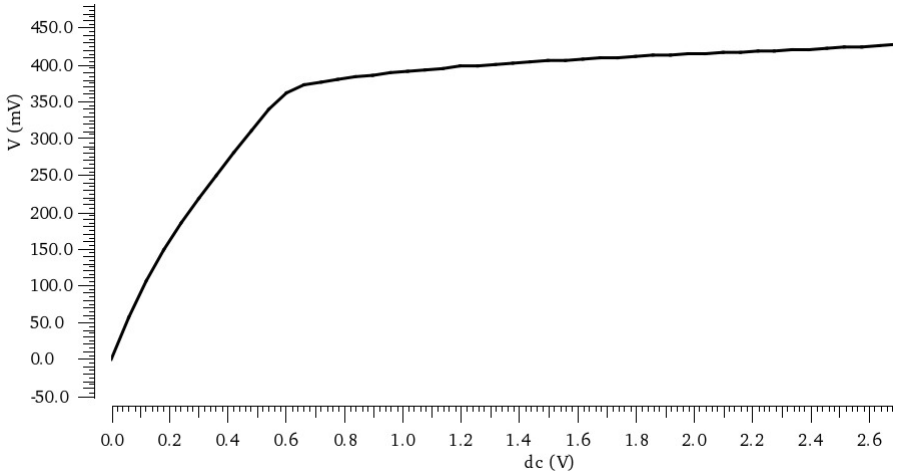

Fig. 6. Variation of BGR Output w.r.t Supply Voltage

V. CONCLUSION

A low power, resistor-less Bandgap Reference circuit has been proposed in this paper. The design consists of subthreshold MOSFETs and a single bipolar transistor, thereby reducing power consumption and chip area. The circuit produces an output voltage of 381.63mV at room temperature with a current consumption of 12 nA. The BGR operates over a temperature range of -50°C to 80°C with a temperature coefficient(TC) of 25ppm/°C. The BGR has a power dissipation of 9.63nW at a supply voltage of 0.8V and can be used for low power applications.

REFERENCES

[1] Lidan Wang, Chenahang Zhan and Guofeng Li, “An Ultra-Low Power and Offset-Insensitive CMOS Subthreshold Voltage Reference”, IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2016.
[2] Hong Zhang, Dong Li, Qing Wang, Jie Zhang, Chong Li2 Ruizhi Zhang, “A Resistor-less Bandgap Reference with Improved PTAT Generator for Ultra-low-power LSIs”, Faible Tension Faible Consommation (FTFC), IEEE, 2014.
[3] Kin Keung Lee, Tor Sverre Lande, Philipp Dominik Häfliger, “A Sub-µW Bandgap Reference Circuit with an Inherent Curvature-Compensation Property”, IEEE Transactions on Circuits and Systems, vol. 62, no. 1, pp. 1-9, Jan. 2015.
[4] Iman Fakharyan, Mehdi Ehsanian, “A Sub-1V Nanowatt CMOS Bandgap Voltage Reference with Temperature Coefficient of 13 ppm/℃”, Iranian Conference on Electrical Engineering (ICEE), IEEE, 2015.
[5] Ting-Chou Lu1, Ming-Dou Ker, Hsiao-Wen Zan, “A 70nW, 0.3V Temperature Compensation Voltage Reference Consisting of Subthreshold MOSFETs in 65nm CMOS Technology”, International Symposium on VLSI Design, Automation and Test (VLSI-DAT), IEEE, 2016.
[6] Qingping Li, Menglian Zhao, Xiaobo Wu, “Design of High Precision Bandgap Voltage Reference with Second-Order Curvature Correction in Bi-CMOS Process”, IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2016.
[7] Myungjun Kim, SeongHwan Cho, “A 0.8V, 37nW, 42ppm/°C Sub-Bandgap Voltage Reference with PSRR of -81dB and Line Sensitivity of 51ppm/V in 0.18um CMOS”, Symposium on VLSI Circuits, IEEE, 2017.
[8] Youngwoo Ji, Cheonhoo Jeon, Hyunwoo Son, Byungsub Kim, Hong-June Park, Jae-Yoon Sim, “A 9.3nW All-in-One Bandgap Voltage and Current Reference Circuit”, IEEE International Solid-State Circuits Conference (ISSCC), 2017.
[9] Yang Liu, Chenchang Zhan, Lidan Wang, “An Ultralow Power Subthreshold CMOS Voltage Reference Without Requiring Resistors or BJTs”,IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 1, pp. 201-205, Jan. 2018.
[10] Arthur Campos de Oliveira, David Cordova, Hamilton Klimach, Sergio Bampi, “Picowatt, 0.45–0.6 V Self-Biased Subthreshold CMOS Voltage Reference”, IEEE Transactions on Circuits and Systems, vol. 64, no. 12, pp. 3036-3046, Dec. 2017.
[11] T. Hirose, K. Ueno, “A CMOS Bandgap and Sub-Bandgap Reference voltage reference circuits for nanowatt power LSIs”, IEEE Asian Solid State Circuits Conference (A-SSCC), 2010.
[12] Oscar E. Mattia, Hamilton Klimach, Sergio Bampi, “0.9 V, 5 nW, 9 ppm/°C resistorless sub-bandgap voltage reference in 0.18µm CMOS”, IEEELatin American Symposium on Circuits and Systems, 2014.