ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

Homojunction TFET Device Design and Analysis for Low Power Applications

Sushmita Badiger[1], K.Sujatha[2] , Dr. Kiran Bailey[3]

PG Student [VLSI], Dept. of ECE, B.M.S College of Engineering, Bangalore, Karnataka, India[1]

Associate Professor, Dept. of ECE, B.M.S College of Engineering, Bangalore, Karnataka, India[2]

Associate Professor, Dept. of ECE, B.M.S College of Engineering, Bangalore, Karnataka, India[3]

ABSTRACT: As the scaling of the conventional MOSFET is increasing, the device is approaching the fundamental limits. Hence there is the need for the alternative device to substitute the conventional MOSFET. The TFET is the most promising device which shows convincing performance as it has high Ion and can achieve lower subthreshold swing than 60mV/dec as compared to MOSFET device. The main objective of this paper is provide the understanding of the two different configuration of DG-TFET devices such as Si-based TFET and InAs TFET to achieve better performance for low power applications. The design and analysis is performed on these devices using Sentaurus TCAD tool. The InAs homojunction TFET device shows the better result that conventional TFET device. This makes it more suitable for low power applications.

KEYWORDS: Tunnel field effect transistor, Indium- Arsenide, Subthreshold swing. low power.

I.INTRODUCTION

The need for faster and more energy efficient computing devices has been a constant motivation for scaling MOSFETs down. This is primarily a result of the short channel effects that emerge due the fundamental physics governing the operation of MOSFETs. These effects lead to major difficulties while implementing low-standby power MOSFET devices [1, 2]. Another problem with MOSFETs, is the limitation of SS of the device to a minimum of 60 mV/decade. Reduction of SS of the device below this fundamental limit becomes imperative for improved switching action of the transistor.

These limitations have inspired researchers to explore other transistor device structure to substitute the traditional MOSFETs. A promising candidate is the Tunnel Field Effect Transistor (TFET). A TFET is a gated p-i-n junction that is operated in reverse bias [3-5]. Majority carriers are injected from the source to the channel through quantum mechanical Band-to-Band Tunneling (BTBT).This improves the fundamental limitation of a minimum SS of 60 mV/decade, allowing TFETs to have SS as low as 20 mv/decade [6]. Although variety of TFET device models have been proposed and continued to develop fundamental parameters such as sub-threshold swing and threshold voltage(Vt), are still not properly defined for TFETs as they are for conventional inversion mode MOSFETs. This paper provides the comparative analysis of two different types of TFET devices such as Si based TFET and III-V semiconductor based TFET device.

II.SUBTHRESHOLD SWING

Subthreshold swing in TFETs is defined in the same way as it is done in MOSFETs which means that it is the gate voltage which must be applied with respect to source so as to increase the drain current by one decade. A formula for calculating the subthreshold swing of TFET is proposed in [7]. This formula shows that SS of TFET is not limited to 60mV/decade. Mathematically Subthreshold Swing (SS) can be expressed as-

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

$$Subthreshold\ Swing = \frac{dVg}{d(\log Id)} mV / dec.$$

The subthreshold swing of MOSFET is limited to 60 mV/dec at T=300K (room temperature) and this limitation can be overcome in TFETs which rely on interband tunneling via barrier width modulation rather than the formation of weak inversion channel between source and drain. Point sub threshold swing is the smallest value of the subthreshold swing on the ID-VG curve and on the other hand average subthreshold swing is calculated from the point where the device starts to turn on up to the threshold point (defined using constant current method [8,9]). The subthreshold swing in TFET is strongly dependent on the gate bias and for analyzing the switching performance it is better to consider average subthreshold swing rather than the point subthreshold swing. Literature indicates that the inherent issue of lower tunneling current that exists in silicon because of relatively higher energy band gap and lower effective tunneling mass has encouraged the designers to deploy lower band gap materials for the fabrication of TFET. Materials like Ge, InAs, GNRs, Heterojunction materials (SiGe/Si, AlGaSb/InAs, AlGaAsSb/InGaAs) etc. leads to a significant increase in the on current of TFET.[19,20,21]

III. TFET DEVICE STRUCTURE AND ITS OPERATION

The basic TFET consists of p-i-n diode structure where the gate is covered by intrinsic region. The figure 1 shows the double gate TFET structure where P+ source region, N+ drain region and intrinsic gate region. This p-i-n configuration helps in tunneling of the electrons between P+ source to intrinsic gate region.[15,17,18]

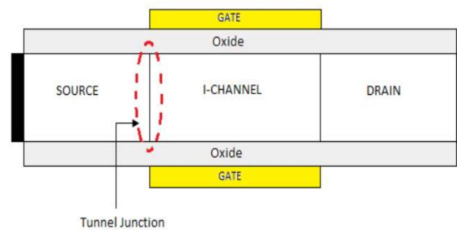

Fig 1. Basic DTFET device structure.

The functionality of the device is dependent on the gate voltage applied so as to buildup the electron near intrinsic region. The current flow in TFET is caused due to phenomenon called as Band to Band Tunnelling(BTBT).By applying gate bias the electrons move from valance band of P-type region to conduction band of intrinsic region by bringing the conduction band to the line of valance band as shown in Fig 2.[13,,16]

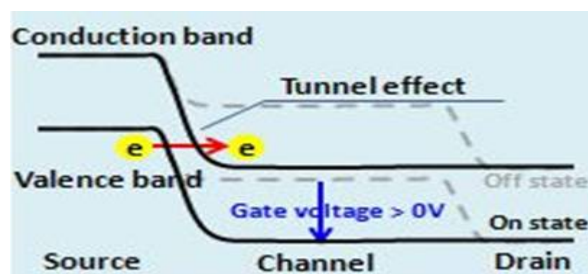

Fig 2. BTBT of TFET.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

IV. RESULT AND DISCUSSION

A. Si-based Double gate TFET Device:

Two-Dimensional Double gate TFET device is constructed and the simulations were performed using Synopsys Sentaurus TCAD[14]. The parameters used for constructing this device is as shown in table 1. and the Double gate TFET device construction is as show in Fig 3.

Parameters	*Values*
Gate length(L_g)	20nm
Source doping concentratio n	1e+20/cm^3
Drain doping concentration	5e+18/cm^3
EOT	0.4nmSiO2+0.6HfO2
Body Thickness	5nm

Table 1. Device Parameters.

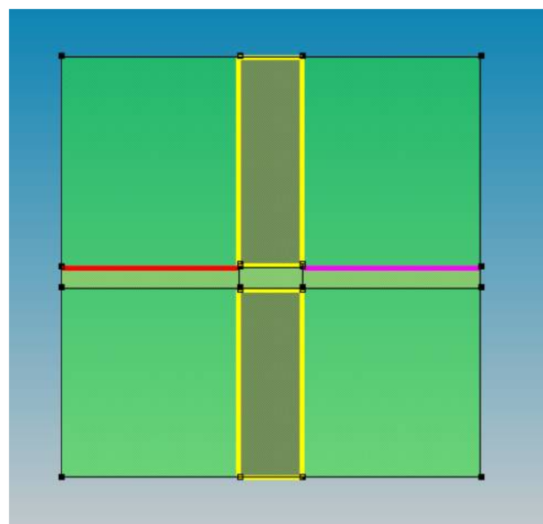

Fig 3. DTFET structure in Sentaurus TCAD.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

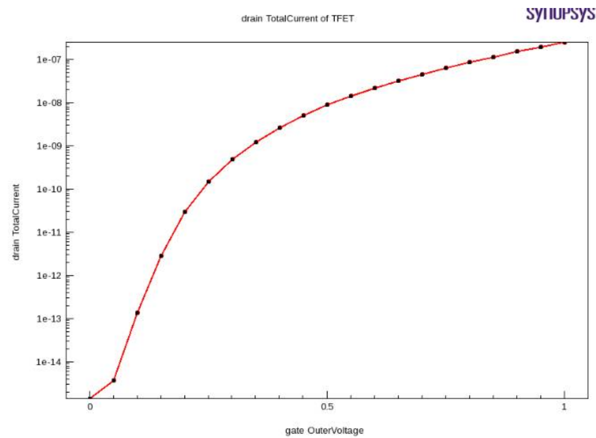

Fig 4. Id Vg characteristics of Si-based DTFET.

The Id Vg characterisctics of Si-based TFET device is shown in Fig 4. Where Ion=0.25uA/um, Ioff=1.42fA/um, Ion/Ioff= 10^8,Vt=0.747V and subthreshold swing= 48.45mV/dec.The performance of the TFET device depends on the different parameters such as source doping concentration, drain doping concentration and High-k dielectric materials used.

B. Effect of High-K dielectric:

As the gate oxide becomes thinner, the gate has better control over the channel. Hence, the high-k dielectric material helps to reduce the effective oxide thickness as it has the larger dielectric constants. Meanwhile, the high-k material increases the the ON-state current and lowers the SS.[11] Fig 5 .shows the Id-Vg characteristics of DTFET device with different dielectric materials such as SiO2, Si3N4 and HfO2.HfO2 shows the better ON current than two of them as it has higher dielectric constant.

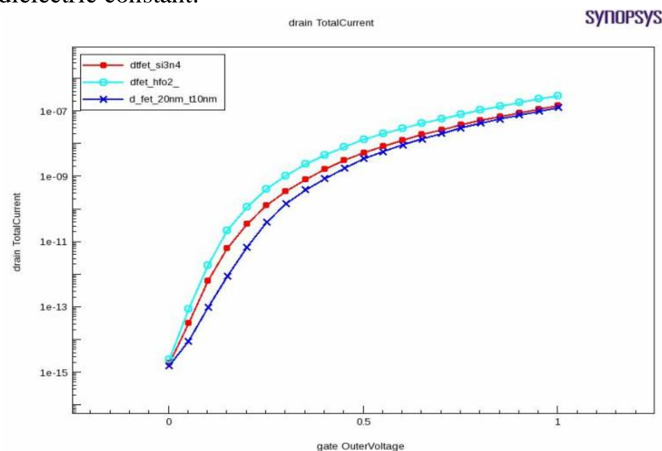

Fig 5.Id Vg curves of DTFET for different dielectric constants,

C. Effect of source and drain doping:

The source doping plays a very important role in increasing the ON current and lower SS of TFET device. As source doping increases the Ion also increases because the electric field at tunneling region is increased and subthreshold swing decreases.[11]

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

Though the drain doping has not much effect on ON current, but lower the drain doping reduces the OFF current. If drain doping level is same as that of source doping level, then there is an undesirable condition caused which is called as ambipolar current.[10,12] To overcome this condition relatively low drain doping level must be chosen.

D. InAs TFET Device:

The InAs TFET device is constructed using the same parameters as used for Si-based TFET device. This is a homojunction TFET device as it has InAs material in all source, gate and drain.To boost the ON current of the device the lower band gap materials can be used instead of Si-based TFET device. The lower band gap material such as InAs is used for Source, drain and channel which increases the tunneling hence, the ON current and subthreshold swing of TFET device is improved.

The Fig 6 shows Id Vg characteristics of InAs based DTFET device where Ion=0.128mA/um, Ioff=8.24e-10A/um. Table 2. Shows comparative results of Si-based TFET and InAs TFET device.

	Si-based TFET	InAs TFET
Ion	0.256uA/um	0.128mA/um
Ioff	1.425fA/um	8.24e-10Aum
Ion/Ioff	10^8	10^5
Vt	0.747V	0.684V
Subtreshold swing	48.457mV/dec	42.16mV/dec

Table 2. Comparison of results of Si-based TFET and InAs TFET.

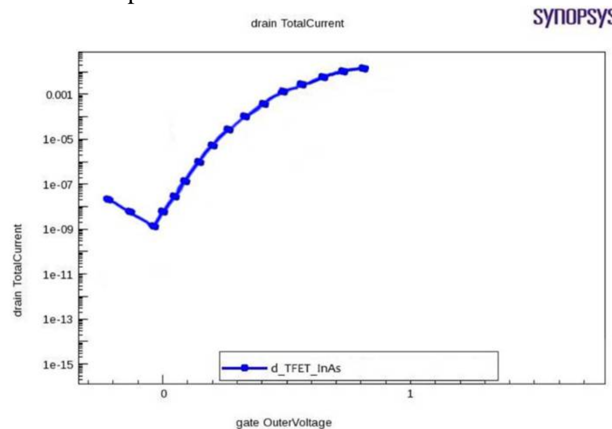

Fig 6. Id Vg Characteristics of InAs TFET device.

The InAs TFET device shows the improved ON current and subthreshold swing as compared to Si-based TFET. As the InAs material has lower energy band gap (0.45eV) as compared to silicon (1.1eV).This shows the significant improvement in subthreshold swing value of 42.16mV/dec.Hence this device configuration has promising performance which is idle candidate for low power high performance applications. The Fig 7. shows the combined curve of Si-based TFET device and InAs TFET device.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

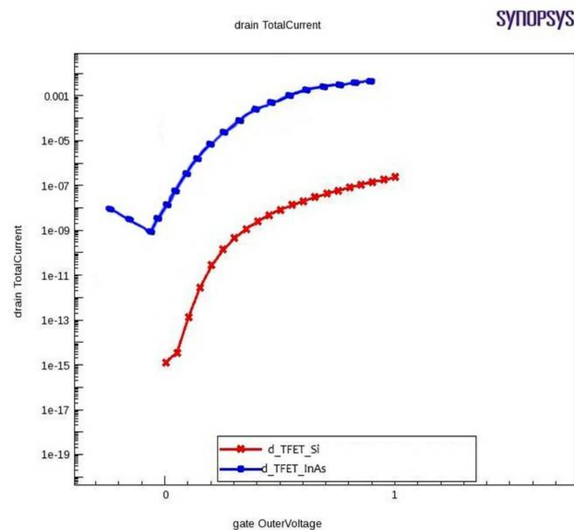

Fig 7. Combined curve for both Si-based TFET and InAs TFET configuration.

V.CONCLUSION

This paper investigate the device performance of the two different configuration i.e. Si-based TFET and InAs TFET device. According to the experimental results conducted InAs TFET device configuration shows the best performance on subthreshold swing as it can achieve the value of 42.16mV/dec and ON current as compared to Si-based TFET device. The TFET device shows tremendous improvement to become potential candidate to replace MOSFET for low power high performance applications.

REFERENCES

[1] K. Boucart and A. M. Ionescu, "Length scaling of the double gate tunnel FET with a high-k gate dielectric", *Solid-State Electronics,* vol. 51, pp.1500-1507, 2007.

[2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling fieldeffect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Letters,* vol. 28, pp. 743-745, 2007.

[3] A. C. Seabaugh, and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2095-2110, Dec. 2010.

[4] J. Madan and R. Chaujar, "Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability," *IEEE Transactions on Device and Materials Reliability,*vol. 16, pp. 227-234, 2016.

[5] J.Madan and R. Chaujar,"Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance", *Superlattices and Microstructures,* vol. 102, pp. 17-26, 2// 2017.

[6] J.Madan and R. Chaujar, "Numerical Simulation of N+ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature", *IEEE Transactions on Electron Devices,* vol. 64, pp. 1482-1488, 2017.

[7] Y. Khatami and K. Banerjee, "Steep subthreshold slope n-and p-type tunnel-FET devices for low-power and energy-efficient digital circuits", *IEEE Transactions on Electron Devices,* vol. 56, pp. 2752-2761, 2009.

[8] Z, Qin, W. Zhao, and A. Seabaugh, "Low-subthreshold swing tunnel transistors," *IEEE Electron Device Letters.,*vol. 2, no. 4, pp. 297-300, Apr. 2006

[9] M. K. Z. Ansari, S. Ahish, D. Sharma, M. H. Vasantha, and YB Nithin Kumar, "Performance analysis of a novel hetero-junction tunnel FET based SRAM at 0.3 V supply voltage," *IEEE Technology Symposium (TechSym),* pp.224-228, Sep. 2016.

[10] C. Anghel, Hraziia, A. Gupta, A. Amara and A. Vladimirescu,"30-nm Tunnel FET With Improved Performance and Reduced Ambipolar Current," *IEEE Trans. on Electron Devices*, vol. 58, no. 6, pp. 1649-1654,Jun. 2011.

[11] K. Boucart, and A. M. Ionescu,"Double-Gate Tunnel FET With High-k Gate Dielectric," *IEEE Trans. on Electron Devices,* vol. 54, no. 7,pp. 1725-1733, Jul. 2007.

[12] Ahmed Shaker, Mona El Sabbagh, and Mohammed M. El-Banna, "Influence of Drain Doping Engineering on the Ambipolar Conduction and High-Frequency Performance of TFETs", *IEEE Transactions on Electron Devices*, VOL. 64, NO. 9, SEPTEMBER 2017.

[13] Li Ying, Bu Jianhui, Luo Jiajun, Han Zhengsheng, **"**Analysis and optimization ofTunneling-FET based on Sol", 978-1-4673-9719-3/16/$31.00 ©2016 IEEE.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 9, September 2018

[14] Sentaurus User's Manual, Synopsys, Inc. Mountain View, CA, 2009.v. 2009.06.
[15] S. Dutta, H. Liu, and V. Naraynan,"Tunnel FET Technology: A reliability perspective," Microelectronics Reliability, vol. 54, no. 5, pp. 861-874, May 2014.
[16] Wieslaw Kuzmicz, "The Future of CMOS: More Moore or the Next Big Thing?" Proceedings of the 24th International Conference "Mixed Design of Integrated Circuits and Systems" , June 22-24, 2017.
[17] Thomas Nirschl, Peng-Fei Wang, Walter Hansch, Doris Schmitt-Landsiedel, " The Tunneling Field Effect Transistor (Tfet): The Temperature Dependence, The Simulation Model, And Its Application."0-7803-8251-X/04/$17.00, ISCAS 2004.
[18] C. Diaz Llorente, C. Le Royer, C-M. V. Lu, P. Batude, C. Fenouillet-Beranger, S. Martinie, F. Allain, and M. Vinet, S. Cristoloveanu and G. Ghibaudo, " First SOI Tunnel FETs with Low-Temperature Process", 978-1-5090-5313-1/17/$31.00 IEEE, 2017.
[19] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic", IEEE Proc., pp. 2095-2108, vol. 98, December 2010.
[20] S. Takagi, D. H. Ahn, T. Gotow, M. Noguchi, K. Nishi, S.-H. Kim, M. Yokoyama, C.-Y. Chang, S.-H. Yoon, C. Yokoyama and M. Takenaka," III-V-based low power CMOS devices on Si platform",2017.
[21] Umesh Dutta, M.K.Soni, Manisha Pattanaik, **"**Design and Analysis of Tunnel FET for Low Power High Performance Applications", *I.J. Modern Education and Computer Science,* 2018, 1, 65-73.