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Analysis of a Cascaded Modified Developed H-Bridgemultilevel Inverter with an Optimum Structure

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ABSTRACT:A general analysis of a cascaded multilevel inverter using developed H- bridge topology is proposed. In comparison with the various existing combined multilevel inverter topology, this topology of a One Twenty One level Multi-Level Inverter has been designed by using a lesser number of dc voltage sources and power switches. The proposed inverter can output more numbers of voltage levels by using this conversionhence, decreases the Total Harmonic Distortion. The voltage sources are sequentially connected in series in order to get different voltage levels at the output. The simple switching technique is implemented by dividing half of the fundamental sine wave with required number of output voltage levels. As the number of levels increases the Total Harmonic Distortion (THD) is reduced due to the increase in the fundamental frequency component of the output waveform. This multilevel inverter is simulated using MATLAB version 8.1.0 (R2013a).

KEYWORDS:H-bridge; Cascaded; Multilevel; Inverter; THD;

I.INTRODUCTION

Designing new topologyof a multilevel inverter is an important area of research in the field of power electronics due to its extensive application in renewable energy systems and machine drives, as a better quality of output waveform could be produced at a lower cost by using lesser number of required power electronic devices. A cascaded multilevel inverter with optimum structure is used in order to generate maximum numbers of output voltage levels by using a constant number of power switches and/or dc voltage sources [1],[4]-[6]. The proposed topology of multilevel inverter uses a transformer-less design in order to acquire higher efficiency by eliminating heat losses and eddy currents [2]. It is impossible to connect a power semiconductor switch to a high voltage network directly. Therefore multilevel inverter had been introduced and is being developed now. A single-phase cascaded multilevel inverter comprises a series connection of the proposed basic unit which consists of different arrays of power switches and dc voltage sources. It is able to only generate positive levels at the output. Therefore, an H-bridge is added to the proposed inverter. This inverter is called the developed cascaded multilevel inverter. The proposed inverter generates all voltage levels (even and odd). The inverter design consists of modular, simplicity of control, and reliability, and they require the lowest number of power semiconductor devices to generate a particular level. [3],[7],[8]. This type of multilevel inverter could be broadly classified into symmetric multilevel inverter which uses dc sources with same amplitude and asymmetric multilevel inverter which uses dc sources with different amplitude. Due to the usage of dc sources with different amplitude, the asymmetric multilevel inverter produces more output voltage levels when compared to symmetric multilevel inverter. Hence the asymmetric multilevel inverter is considered to be more efficient when compared to the symmetric structure as the number of level of output voltage increase; the fundamental sine wave tracking becomes more prominent and efficient thus producing better quality of output waveform. A multilevel inverter with asymmetric

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structure is the proposed design in focus [5]. The bidirectional power switches have been used in this topology. Asymmetric cascaded multilevel inverter has been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them. Two of thistopology has been presented in [9] and [10]. The switching losses in the multilevel inverter is considered to be one of the important factor the affects the overall efficiency of the multilevel inverter. Hence determining the switching losses is necessary to find out the efficiency of this design. The switching losses depend on the operating frequency of every switch. The peak current flowing through every semi-conductor switch in this topology of multilevel inverter remains same [11]. Multilevel inverter have found wide acceptance as they can achieve a low harmonic component with low switching frequency. The multilevel VSI enables to synthesize output voltages with reduced harmonic distortion. By increasing the number of levels in the multilevel inverter, the output voltages have more steps in generating a staircase waveform, reduced dv/dt stresses, operating with low switching frequency, as well as minimum harmonic distortion and switching losses. The reduction in the total harmonic distortion (THD) is one of the key factors that will be analysed and compared with total harmonic distortion of a lower level multilevel inverter and justify the efficiency of this topology [11]. The multilevel inverter has gained much attention in recent years due to its advantages in lower switching loss, better electromagnetic compatibility, higher voltage capability, and lower harmonics. The inverter generate a stepped voltage waveform by using a number of dc voltage sources as the input and an appropriate arrangement of the power-semiconductor-based devices.The number of switching devices used for the proposed inverter is reduced by using this scheme. The harmonics of the output voltage waveform are also reduced. Capacitors, batteries, and other dc voltage sources can be used as the voltage sources of the proposed inverter, considering that the peak current flows through every source. Hence used sources must be designed to withstand higher magnitude of currents. The performance of the proposed single phase 121-level inverter with reduced number of switches is observed. The application of this inverter is mainly used in industries and is used in FACTS devices to improve the quality of the power system. While these inverter are used there is no need of transformer and filters. Therefore installation cost and harmonic are reduced.

In this paper in the section II presents the 121 level inverter topology and their features and characteristics. The section III will deal with the simulation of the proposed topology of 121-level inverter. The section IV will deal with simulation result analysis.

II. CIRCUIT TOPOLOGY

The proposed topology is mainly aimed at increasing the number of output voltage level with lesser number of power switches. The proposed topology produces 121 levels at the output with 14 power switches and 6 voltage sources. The proposed topology consists of two identical units that are cascaded to give 121 levels at the output. Each unit is an 11 level circuit having 7 power switches each. Six voltage sources are $V_{L,L}$, $V_{L,R1}$, $V_{L,R2}$, $V_{R,L}$, $V_{R,R1}$ and $V_{R,R2}$. The sources are sequentially connected in both positive and negative sequence to get various levels at output. If the step voltage is taken as V_1 then, the sources are chosen such that $V_{L,L}$ should be equal to V_1 , $V_{L,R1}$ and $V_{L,R2}$ should be equal to twice of V_1, $V_{R,L}$ should be equal to $2(V_{L,L}+V_{L,R1}+V_{L,R2})+V_1$, $V_{R,R1}$ and $V_{R,R2}$ should be equal to twice of $V_{R,L}$. The switches in the left unit are denoted as S_{11}, S_{12}, S_{13}, S_{14}, S_{X1}, S_{Y1} and S_{P1}. In which S_{P1} is a bi-directional switch. Similarly there are 7 switches in right unit namely S_{21}, S_{22}, S_{23}, S_{24}, S_{X2}, S_{Y2} and S_{P2} where S_{P2} is a bi-directional switch. In this topology, equal area criteria switching technique is used for finding the best switching angles for the switches, by dividing the half of fundamental sine wave with step voltages. The circuit diagram of the developed topology is given in Fig. 1

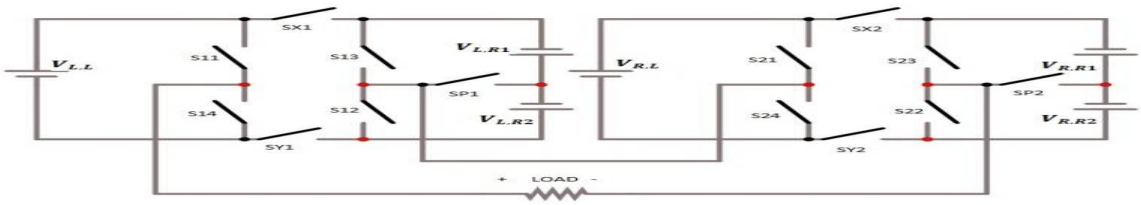

***Fig.1**: 121 level inverter*

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The output levels and various switching pattern of the switches used in the topology is given in the table 1. In this table the indicated switches are in ON state, whereas the non-indicate are in OFF state.

***Table 1**: Switching sequences and corresponding output voltage levels of the proposed 121-level inverter*

LEVEL	LEFT UNIT	RIGHT UNIT	OUTPUT VOLTAGE
1	S_{11}, S_{13}, S_{Y1}	S_{21}, S_{23}, S_{Y2}	$+60V_1$
2	S_{13}, S_{14}, S_{Y1}	S_{21}, S_{23}, S_{Y2}	$+59V_1$
. . .	. . .	. . .	. . .
55	S_{11}, S_{13}, S_{Y1}	S_{21}, S_{23}, S_{X2}	$+5V_1$
56	S_{13}, S_{14}, S_{Y1}	S_{21}, S_{23}, S_{X2}	$+4V_1$
57	S_{11}, S_{P1}, S_{Y1}	S_{21}, S_{23}, S_{X2}	$+3V_1$
58	S_{14}, S_{P1}, S_{Y1}	S_{21}, S_{23}, S_{X2}	$+2V_1$
59	S_{11}, S_{12}, S_{Y1}	S_{21}, S_{23}, S_{X2}	$+V_1$
60	S_{11}, S_{13}, S_{X1}	S_{21}, S_{23}, S_{X2}	0
61	S_{13}, S_{14}, S_{X1}	S_{21}, S_{23}, S_{X2}	$-V_1$
62	S_{11}, S_{P1}, S_{X1}	S_{21}, S_{23}, S_{X2}	$-2V_1$
63	S_{14}, S_{P1}, S_{X1}	S_{21}, S_{23}, S_{X2}	$-3\ V_1$
64	S_{11}, S_{12}, S_{X1}	S_{21}, S_{23}, S_{X2}	$-4V_1$
65	S_{12}, S_{14}, S_{X1}	S_{21}, S_{23}, S_{X2}	$-5V_1$
. . .	. . .	. . .	. . .
120	S_{11}, S_{12}, S_{X1}	S_{22}, S_{24}, S_{X2}	$-59V_1$
121	S_{12}, S_{14}, S_{X1}	S_{22}, S_{24}, S_{X2}	$-60V_1$

Based on switching table, the switches can be sequentially turned ON and turned OFF, in order to get various voltage levels at the output. Using switching table, the mode of operation of different voltage levels can be interpreted. Sample mode of operation for one negative voltage level and one positive voltage level is shown in Fig. 2 and Fig. 3 respectively. Taking experimental values such that $V_{L,L}$=5V, $V_{L,R1}$=$V_{L,R2}$=10V, $V_{R,L}$=55V and $V_{R,R1}$=$V_{R,R2}$=110V, Fig. 2 shows the mode of operation for -30V and Fig. 3 shows the mode of operation for +55V.

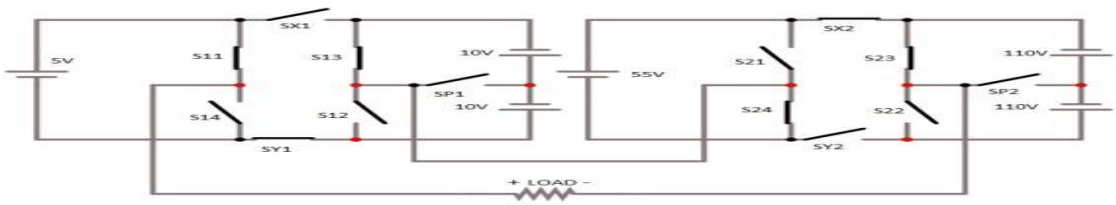

***Fig.2**: Mode of operation for -30V.*

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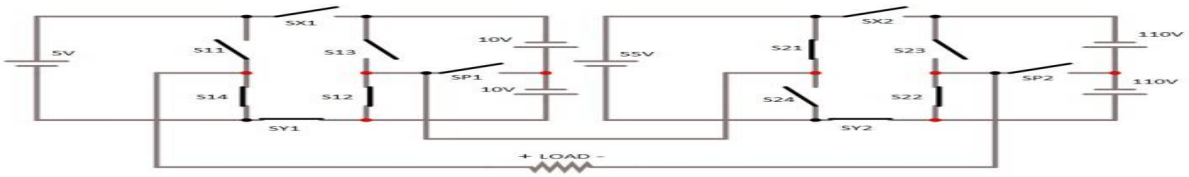

***Fig.3**: Mode of operation for +55V.*

Since the switches are connected in series, the peak voltage across each switch is different. However the switches on the same branch have same peak voltage. The voltages stress across each switch is given as,

$$V_{S11} = V_{S14} = V_{L,L} \quad (1)$$

$$V_{S12} = V_{S13} = V_{L,R1} + V_{L,R2} \quad (2)$$

$$V_{SX1} = V_{SY1} = V_{L,L} + V_{L,R1} + V_{L,R2} \quad (3)$$

$$V_{SP1} = V_{L,R1} \quad (4)$$

$$V_{S21} = V_{S24} = V_{R,L} \quad (5)$$

$$V_{S22} = V_{S23} = V_{R,R1} + V_{R,R2} \quad (6)$$

$$V_{SX2} = V_{SY2} = V_{R,L} + V_{R,R1} + V_{R,R2} \quad (7)$$

$$V_{SP2} = V_{R,R1} \quad (8)$$

Since the switches are connected in series for every mode of operation, the peak current passing through every switch is same. The peak current flowing in the circuit is given as,

$$I = \frac{V_{L,L} + V_{L,R1} + V_{L,R2} + V_{R,L} + V_{R,R1} + V_{R,R2}}{R_L} \quad (9)$$

III.SIMULATION

Fig. 4 shows 121 level inverter consisting two sub systems built using MATLAB version 8.1.0 (R2013). During simulation, sinusoidal waveform is taken as reference and compared with a constant comparator to generate the switching frequency for the switches. For simulation, the power switches used are IGBT switches. The simulated circuit is tested with resistive load.

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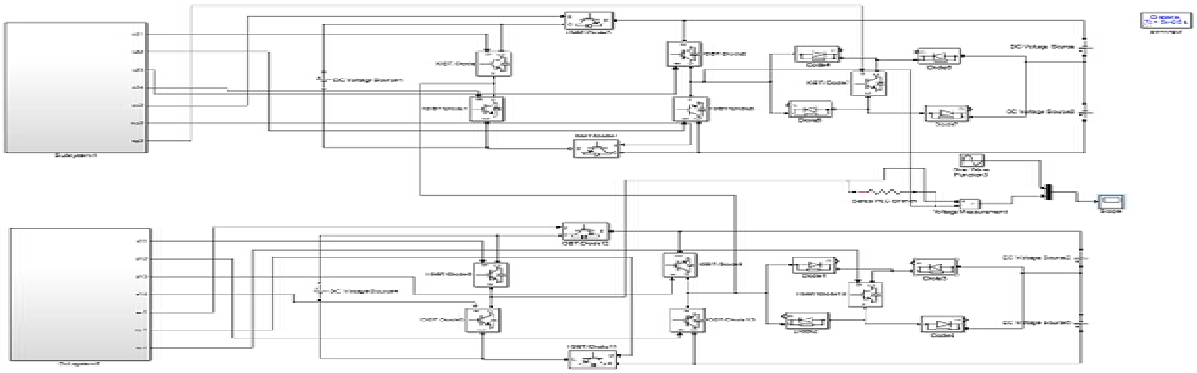

***Fig. 4**: Simulation diagram of 121-level inverter with resistive load.*

***Table 2**: Simulation Parameters*

$V_{L,L}$	5V
$V_{L,R1} = V_{L,R2}$	10V
$V_{R,L}$	55V
$V_{R,R1} = V_{R,R2}$	110V
S11,S12,S13,S14,S21,S22, S23,S24,SX1,SX2, SY1,SY2	Uni-directional switches
SP1,SP2	Bi-directional switches

IV.SIMULATION RESULTS

Fig. 5, shows the MATLAB simulation output voltage waveform with 60 positive voltage levels, 60 negative voltage levels and one zero voltage level, which constitutes a total of 121 levels. Here we can see that the waveform is having less distortion from ideal sine wave. This indicates least introduction of harmonics into the supply. Fig. 6 and Fig.7 shows the output waveform of the individual unit in the proposed cascaded topology. The FFT analysis for the 121 level inverter is carried out in the Simulink to study the Total Harmonic Distortion (THD) at the output of inverter. The THD of the proposed 121 level inverter is found to be 0.85%. THD for output voltages is shown in Fig. 8.

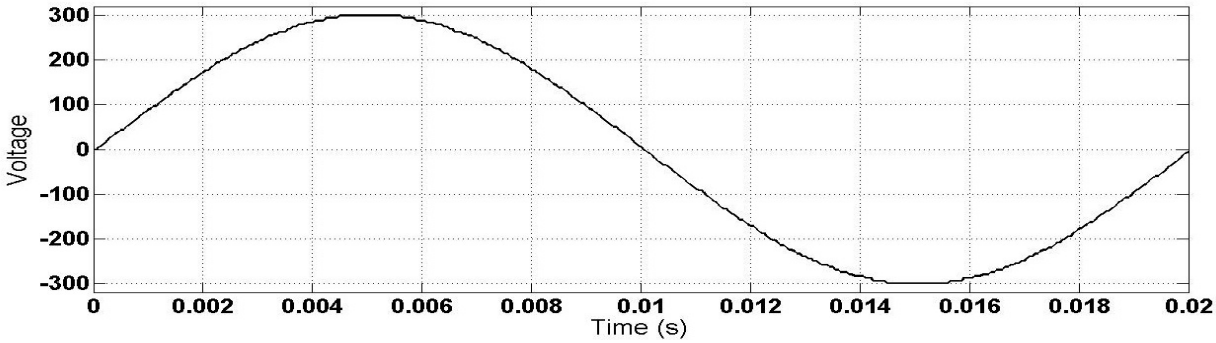

***Fig.5**: Voltage waveform of 121 level inverter*

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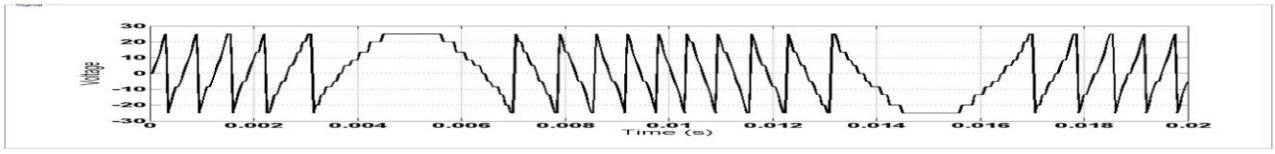
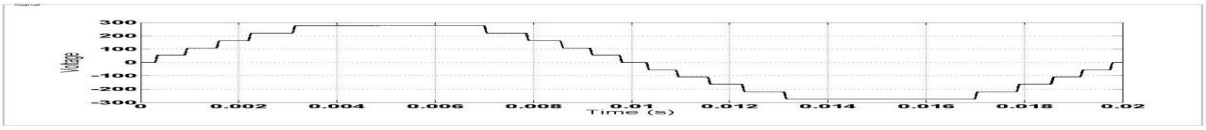


***Fig.6**: Voltage waveform of left unit*



*. **Fig.7**: Voltage waveform of right unit*

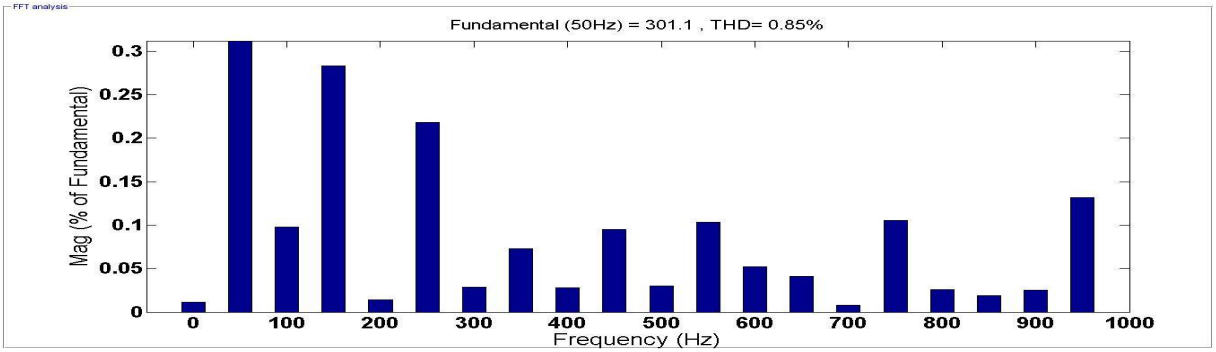


***Fig.8**: FFT Analysis of 121 level inverter with resistive load*

The voltage stress across switch S11 is shown in fig.9. As per equation (1) the voltage across the switch should be maximum of $V_{L,L}$ which is equal to 5V.

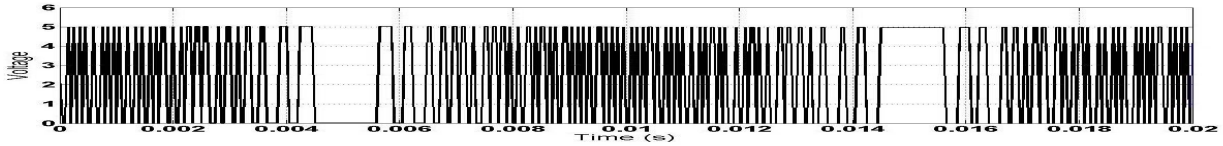


***Fig.9** : Voltage waveform across switch S11*

The voltage stress across switch S12 is shown in fig.10. As per equation (2) the voltage across the switch should be maximum of $V_{L,R1}, V_{L,R2}$ which is equal to 10V.

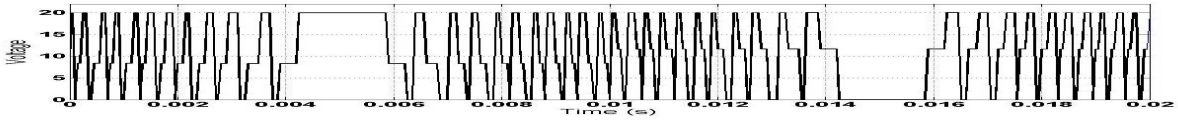


***Fig.10** : Voltage waveform across switch S12*

The voltage stress across switch S13 is shown in fig.11. As per equation (2) the voltage across the switch should be maximum of $V_{L,R1} + V_{L,R2}$ which is equal to 20V.

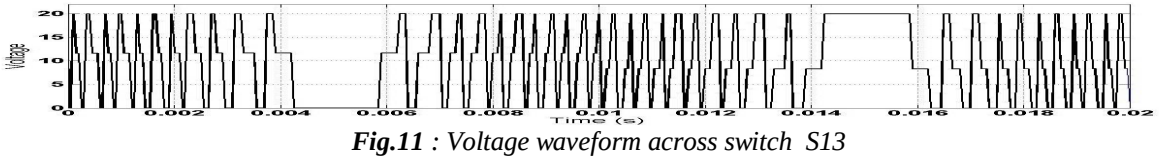


***Fig.11** : Voltage waveform across switch S13*

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The voltage stress across switch S14 is shown in fig.12. As per equation (1) the voltage across the switch should be maximum of $V_{L,L}$ which is equal to 5V.

***Fig.12**: Voltage waveform across switch S14*

The voltage stress across switch SP1 is shown in fig.13. As per equation (4) the voltage across the switch should bemaximumof $V_{L,R1}$ which is equal

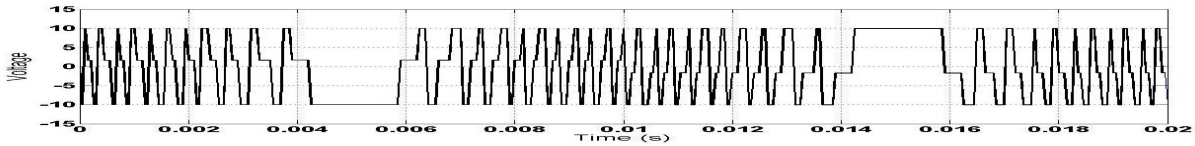

***Fig.13**: Voltage waveform across switch SP1*

The voltage stress across switch SX1 is shown in fig.14. As per equation (3) the voltage across the switch should be maximum of $V_{L,L}+V_{L,R1}+V_{L,R2}$ which is equal to 25V.

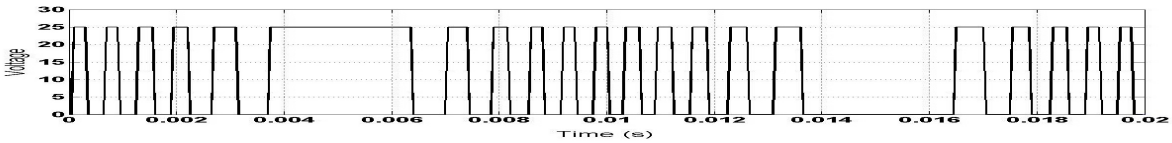

***Fig .14** : Voltage waveform across switch SX1*

The voltage stress across switch SY1 is shown in fig.15. As per equation (3) the voltage across the switch should be maximum of $V_{L,L}+V_{L,R1}+V_{L,R2}$ which is equal to 25V.

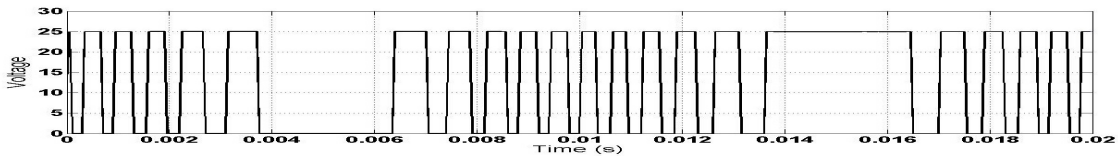

***Fig .15** : Voltage waveform across switch SY1*

The voltage stress across switch S21 is shown in fig.16. As per equation (5) the voltage across the switch should be maximum of $V_{R,L}$ which is equal to 55V.

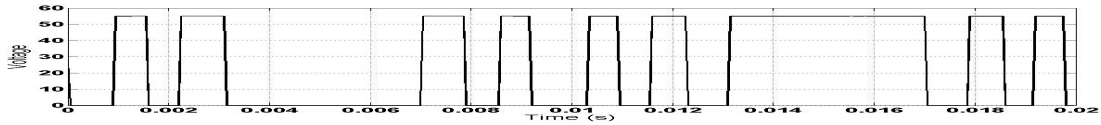

***Fig.16:** Voltage waveform across switch S21*

The voltage stress across switch S22 is shown in fig.17. As per equation (6) the voltage across the switch should be maximum of $V_{R,R1}+V_{R,R2}$ which is equal to 220V.

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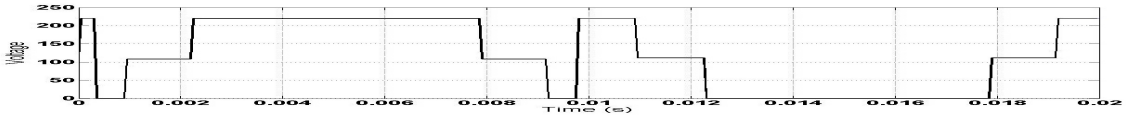

Fig.17*: Voltage waveform across switch S22*

The voltage stress across switch S23 is shown in fig.18. As per equation (6) the voltage across the switch should be maximum of $V_{R,R1}+V_{R,R2}$ which is equal to 220V

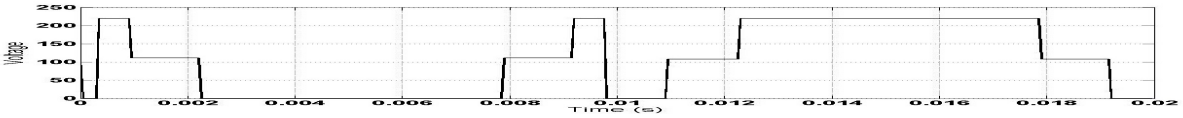

Fig.18 *: Voltage waveform across switch S23*

The voltage stress across switch S24 is shown in fig.19. As per equation (5) the voltage across the switch should be maximum of $V_{R,L}$ which is equal to 55V.

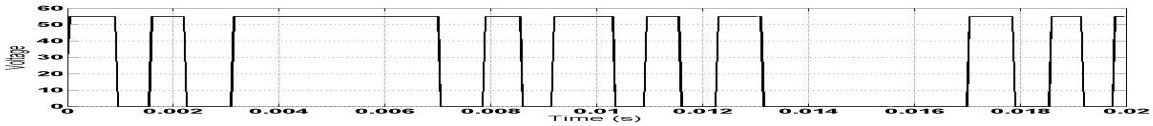

Fig.19*: Voltage waveform across switch S24*

The voltage stress across switch SP2 is shown in fig.20. As per equation (8) the voltage across the switch should be maximum of $V_{R,R1}$ which is equal to 110V.

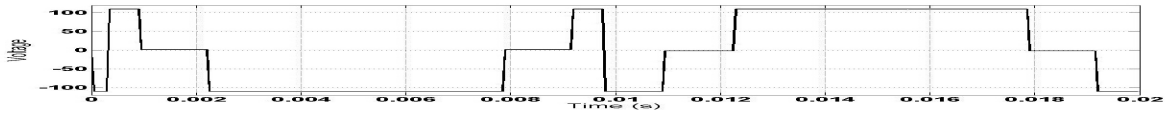

Fig.20*: Voltage waveform across switch SP2*

The voltage stress across switch SX2 is shown in fig.21. As per equation (7) the voltage across the switch should be maximum of $V_{R,L}+V_{R,R1}+V_{R,R2}$ which is equal to 275V.

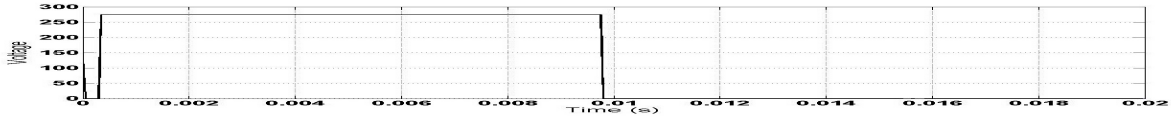

Fig.21*: Voltage waveform across switch SX2*

The voltage stress across switch SY2 is shown in fig.22. As per equation (7) the voltage across the switch should be maximum of $V_{R,L}+V_{R,R1}+V_{R,R2}$ which is equal to 275V.

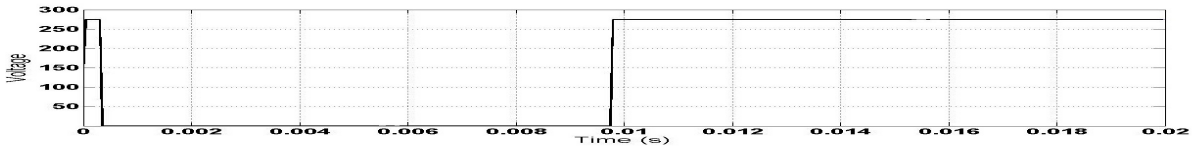

Fig.22 : Voltage waveform across switch SY2

V.CONCLUSION

The advantage of the proposed topology is,it has only 14 switches, 6 sources which leads to reduced harmonics less than 1%i.e. 0.85%. Compared to [7] the cascaded circuitry has the ability to add as well as subtract voltagelevels

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thereby reducing the no of sources across it. Based on the generalized method higher levels of multilevel inverter can be designed in future. The performance accuracy of the proposed single phase 121-level inverter with resistive load circuit had been verified using MATLAB simulation.

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