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A Novel Topology on Asymmetric Multilevel Inverter using Developed H-Bridge

Ashwinner.A[1], B.Prakash Ayyappan.,M.E.[2],

M.E. Power Electronics and Drives, Department of Electrical and Electronics Engineering, Chenduran College of Engineering and Technology, Lena Vilakku, Pilivalam Post, Pudukkottai, Tamil Nadu, India.

Assistant Professor, Department of Electrical and Electronics Engineering, Chenduran College of Engineering and Technology, Lena Vilakku, Pilivalam Post, Pudukkottai, Tamil Nadu, India.

ABSTRACT: This system presents an asymmetrical multilevel inverter topology with Different PWM techniques. This system uses one cell of conventional cascade H-Bridge Multilevel inverter structure with additional switch and voltage source to obtain high voltage level. The aim of this paper to enhance the voltage level at the output with using less switch. To improve the output voltage harmonic spectrum, the pulse width modulation (PWM) techniques used. The advantage of this proposed topology to reduce the circuit complexity and total harmonic distortion. The results of proposed 65-Level Asymmetrical multilevel Inverter are shown using MATLAB/SIMULINK software.

KEYWORDS: Pulse Width Modulation, PWM, H-Bridge, Voltage Maintenance, 65-Level Inverter.

I. INTRODUCTION

An inverter, also named as power inverter, is an electrical power device which is used to convert direct current (DC) into alternating current (AC). Using few control circuits and switches, one can get AC at any required voltage and frequency. Inverter plays exactly the opposite role of rectifiers as rectifiers are used for converting alternating current (AC) into direct current (DC). There are different types of inverters available these days. Few most commonly used inverter types are:

- Square wave inverters
- Modified sine wave inverters
- Multilevel inverters
- Pure sine wave inverters
- Resonant inverters
- Grid tie inverters
- Synchronous inverters
- Stand-alone inverters
- Solar inverters

Due to the development of power semiconductor switches such as MOSFETs and Insulated-gate bipolar transistor (IGBTs), which enables the research interest in high power converters, such as multilevel voltage-source inverters and its dual, multilevel current-source inverters and so on. Multilevel inverter have the capability to deliver higher output power with lower DV/DT with less-distorted output waveforms, resulting in reduction of electromagnetic interference (EMI) noise and size of an output filter. In most renewable energy sources, such as photovoltaic system, which deliver dc power; must be converted to ac power and is fed into the grid through grid connected inverter/ isolated

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loads. Various international standards, like and impose requirements on the inverter`s output power quality, i.e., harmonic currents and total harmonics distortion (THD) of the output current.

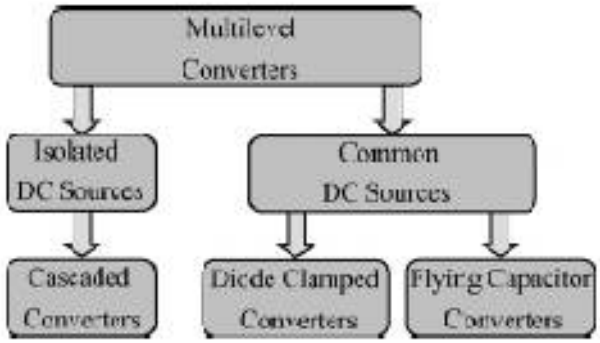

Fig.1 Types of Multi-Level Inverter

The Current Energy Arena is changing. The feeling of dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amounts of resources, economical and human, to develop new cheaper and cleaner energy resources not related to fossil fuels. In fact, for decades, renewable energy resources have been the focus for researchers, and different families of power converters have been designed to make the integration of these types of systems into the distribution grid a current reality.

Besides, in the transmission lines, high- power electronic systems are needed to assure the power distribution and the energy quality. Therefore, power electronic converters have the responsibility to carry out these tasks with high efficiency. The increase of the world energy demand has entailed the appearance of new power converter topologies and new semiconductor technology capable to drive all needed power. A continuous race to develop higher-voltage and higher-current power semiconductors to drive high- power systems still goes on. In this way, the last-generation devices are suitable to support high voltages and currents (around 6.5 kV and 2.5 kA). However, currently there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices.

This idea is shown in Figure 1, where multilevel converters built using mature medium-power semiconductors are fighting in a development race with classic power converters using high-power semiconductors that are under continuous development and are not mature. Nowadays, multilevel converters are a good solution for power applications due to the fact that they can achieve high power using mature medium-power semiconductor technology. Multilevel converters present great advantages compared with conventional and very well-known two-level converters.

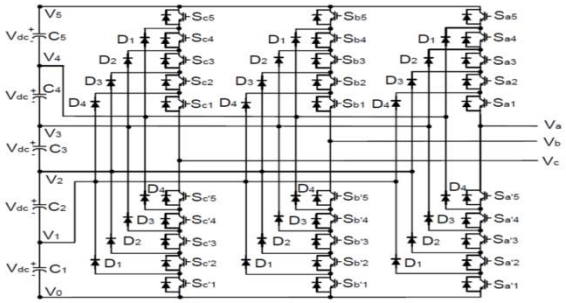

Fig.2 Diode Clamped Multilevel Inverter

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These advantages are fundamentally focused on improvements in the output signal quality and a nominal power increase in the converter. In order to show the improved quality of the output voltages of a multilevel converter, the output voltage of a single-phase two-level converter is compared to three and nine-level voltage multilevel wave forms. The power converter output voltage improves its quality as the number of levels increases reducing the total harmonic distortion (THD) of the output waveforms. Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly.

As a result, a multilevel power inverter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.

A. Multi-Level Inverter

The concept of multilevel inverters has been introduced since 1975. The term multilevel began with the three-level Inverter. Subsequently several multilevel inverter topologies have been developed. However, the elementary concept of a multilevel inverter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. There are several topologies of multilevel inverters available. The difference lies in the mechanism of switching and the source of input voltage to the multilevel inverters. Three most commonly used multilevel inverter topologies are:

(a) Diode Clamped multilevel inverters
(b) Flying Capacitor multilevel inverters
(c) Cascaded H-bridge multilevel inverters

As previously mentioned, three different major multilevel inverter structures have been applied in industrial applications: cascaded H-bridges inverter with separate dc sources, diode clamped, and flying capacitors.

Before continuing discussion in this topic, it should be noted that the term multilevel inverter is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode. Figure 2 shows the classification of multilevel inverters based on the input voltage sources. The multilevel inverter structures are the focus of in this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

B. Diode Clamped Multilevel Inverter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. In the 1990s several researchers published articles that have reported experimental results for four-, five-, and six-level diode-clamped converters for such uses as static var compensation, variable speed motor drives, and high-voltage system interconnections. A three-phase six-level diode-clamped inverter is shown in Figure2.2. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is Vdc, and the voltage stress across each switching device is limited to Vdc through the clamping diodes. The output voltage levels possible for one phase of the inverter with the negative dc rail voltage V0 as a reference. State condition 1 means the switch is on, and 0 means the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair require that the other complementary switch be turned off. The complementary switch pairs for phase leg are (Sa1, Sa'1), (Sa2, Sa'2), (Sa3, Sa'3), (Sa4, Sa'4), and (Sa5, Sa'5).

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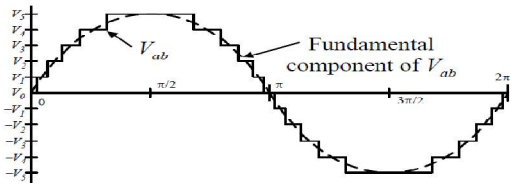

Fig.3 Output Voltage Waveform

C. Flying-Capacitor Multilevel Inverter

Meynard and Foch introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The circuit topology of the flying capacitor multilevel inverter is shown in Figure2.4. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage.

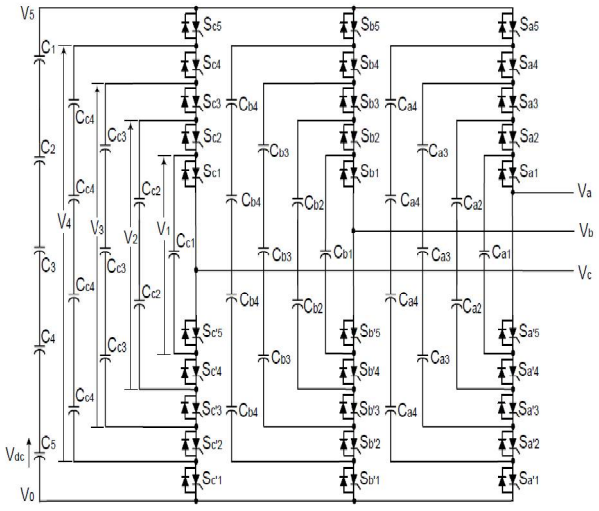

Fig.4 Flying Capacitor Multilevel Inverter

The combinations of phase voltage levels that is possible for the six-level circuit shown in Figure 2.4. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [2, 3, 33]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

D. Cascaded H-Bridge Multilevel Inverter

A single-phase structure of an m-level cascaded inverter is illustrated in Figure 5. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different

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voltage outputs, +Vdc, 0, and –Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain +Vdc, switches S1 and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0.

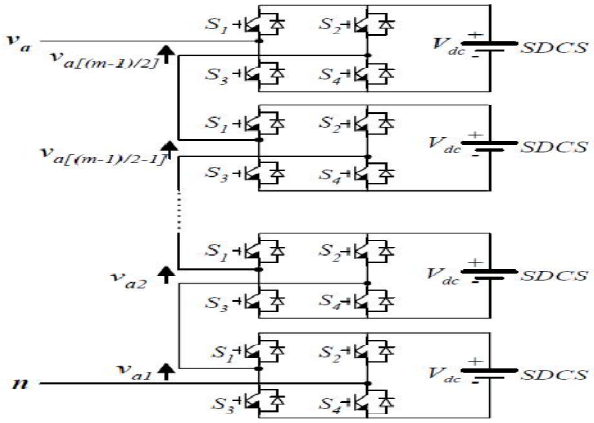

Fig.5 Cascaded H-Bridge Multilevel Inverter

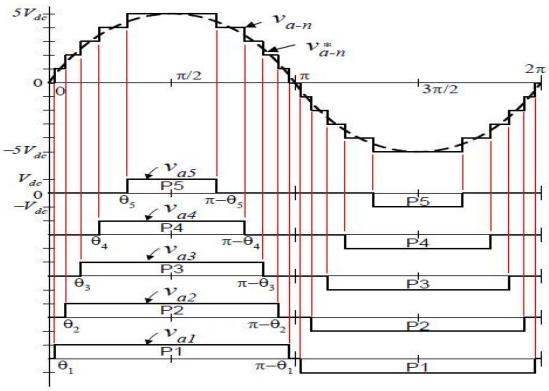

Fig.6 Output Voltage Waveform

The combinations of phase voltage levels that is possible for the six-level circuit shown in Figure 4. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) be in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [2, 3, 33]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for

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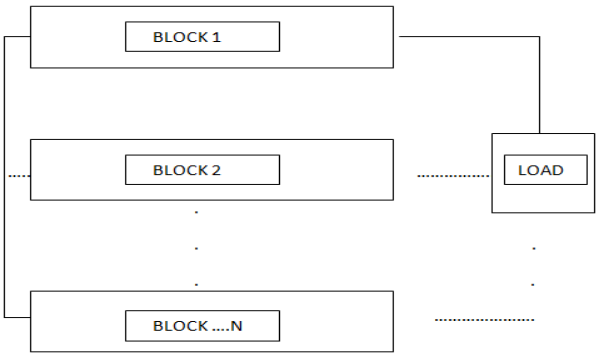

Fig.7 Proposed System Block Diagram

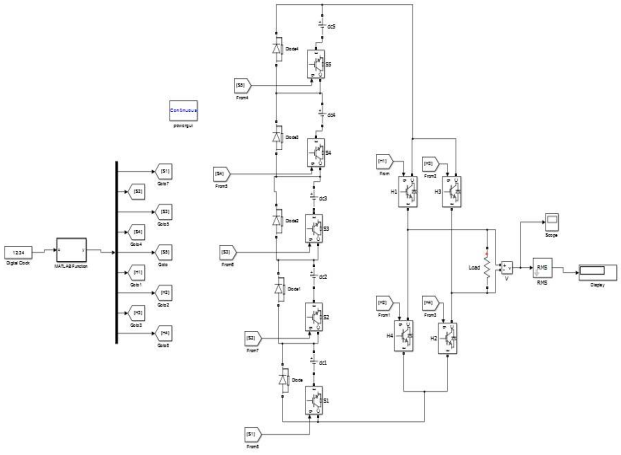

Fig.8 Proposed System Circuit Diagram

II. LITERATURE SURVEY

EbrahimBabaei (2014)discussed aMultilevel inverter technology has been developed recently as a very significant alternative in the area of medium and high power applications. The New General Topologies for Cascaded Multilevel inverters with Reduced Number of components based on Developed H Bridge to the general function of a multilevel inverter is to synthesize a desired output voltage from several levels of dc voltages as inputs. In order to increase the steps in the output voltage. In the procedure described in this reference, despite all the advantages, it is not possible to produce all the steps (odd and even) in the output. In addition, for producing an output voltage with a constant number of steps, there are different configurations with a different number of components.

In this paper, the optimal structures for this topology are investigated for various objectives such as minimum number of switches and different amplitude dc voltage sources and minimum standing voltage on the switches for producing the maximum output voltage steps. Two new algorithms for determining the dc voltage sources magnitudes have been proposed. Finally, in order to verify the theoretical issues, simulation and experimental results for a 31-level inverter by using 4Nos of Asymmetric voltage sources and 10Nos of bi directional power switches.

This paper help to the optimal structures for this topology are investigated for various objectives such as minimum number of switches and different amplitude dc voltage sources [1].Ali Ajami†, AtaollahMokhberdoran* and

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Mohammad Reza JannatiOskuee(2013)describedaboutthe multilevel inverters are developing generally due to reduced voltage stress on power switches and low total harmonic distortion (THD) in output voltage. However, for increasing the output voltage levels the number of circuit devices are increased and it results in increasing the cost of converter. In this paper, a novel multilevel inverter is proposed. The suggested topology uses less number of power switches and related gate drive circuits to generate the same level in output voltage with comparison to traditional cascaded multilevel inverter. With the proposed topology all levels in output voltage can be realized.

As an illustration, a symmetric 65-level and asymmetric 29-level proposed inverters have been simulated and implemented. The total peak inverse (PIV) and power losses of presented inverter are calculated and compared with conventional cascaded multilevel inverter. The presented analyses show that the power losses in the suggested multilevel inverter are less than the traditional inverters. Presented simulation and experimental results demonstrate the feasibility and applicability of the proposed inverter to obtain the maximum number of levels with less number of switches. This paper is very helpful to develop generally due to reduced voltage stress on power switches and low total harmonic distortion (THD) in output voltage[2].

M. R. Banaei† and E. Salary (2013)described about that the Multilevel inverters produce a staircase output voltage from DC voltage sources. Requiring great number of semiconductor switches is main disadvantage of multilevel inverters. The multilevel inverters can be divided in two groups: symmetric and asymmetric converters. The asymmetric multilevel inverters provide a large number of output steps without increasing the number of DC voltage sources and components. In this paper, a novel topology for multilevel converters is proposed using cascaded sub-multilevel Cells. These sub-multilevel converters can produce five levels of voltage.

Four algorithms for determining the DC voltage sources magnitudes have been presented. Finally, in order to verify the theoretical issues, simulation is presented [3].Thamizharasan. S*, Baskaran. J** and Ramkumar. S (2015) observed a new idea to arrive at reduced switch count topological structures configured in the form of a matrix for a cascaded Multi level inverter (CMLI). The theory encircles to minimize the number of switches involved in the conduction path and there from acclaim reduced input current distortion, lower switching losses and electromagnetic interference.

The focus extends to standardize the number of power devices required for reaching different levels of output voltage from the same architecture. It includes appropriate pulse width modulation (PWM) strategy to generate firing pulses and ensure the desired operation of the power modules. The investigative study carries with it MATLAB based simulation and experimental results obtained using suitable prototypes to illustrate the viability of the proposed concept. The promising nature of the performance projects a new dimension in the use of single phase MLIs for renewable energy related applications [4].

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III. EXPERIMENTAL RESULTS

The following table illustrates the number of levels.

TABLE.1 NUMBER OF LEVELS

NUMBER OF LEVELS	VOLTAGE	COMBINED VOLTAGE SOURCE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
1	5	V_1	0	0	1	1	0	1	0	1	0
2	10	V_2-V_1	0	1	0	1	0	1	1	0	1
3	15	V_2	1	1	1	0	0	1	0	0	1
4	20	V_1+V_2	0	1	1	0	0	1	0	1	1
5	25	V_3-V_1	1	0	0	1	1	0	1	0	0
6	30	V_3	1	1	0	0	1	0	0	1	0
7	35	V_3+V_1	0	0	0	0	1	1	1	1	0
8	40	V_3+V_2	0	0	1	1	1	0	1	0	1
9	45	V_1+V_2+V_3	0	1	0	1	1	0	0	0	0
10	50	V_4-V_1	1	1	1	1	0	1	0	0	1
11	55	V_4	0	1	1	1	1	1	0	1	1
12	60	V_4+V_1	1	0	0	0	0	1	1	1	1
13	65	V_4+V_2	1	1	0	0	1	1	0	0	1
14	70	V_4+V_2	1	0	0	0	0	0	1	1	1
15	75	V_4+V_3	1	1	1	1	1	0	1	1	1
16	80	V_1+V_2+V_3+V_4	1	0	1	0	0	0	1	0	0
17	85	V_5-V_1	1	1	0	1	0	1	1	0	0
18	90	V_5	0	1	1	0	0	0	1	0	0
19	95	V_5+V_1	0	0	1	1	0	1	1	1	1
20	100	V_5+V_2	0	1	0	1	1	0	0	1	1
21	105	V_5+V_3	1	0	0	1	1	1	0	0	1
22	110	V_5+V_4	1	1	0	0	1	1	0	1	0
23	115	V_1+V_2+V_3+V_4+V_5	1	1	1	0	1	1	1	1	0
24	120	V_5-V_4	0	0	1	0	0	0	1	0	0
25	125	V_5-V_3	0	1	0	1	1	0	1	1	1
26	130	V_5-V_2	0	1	1	1	0	0	0	1	1
27	135	V_5-V_3	1	1	1	0	1	1	0	0	0
28	140	V_5-V_2	1	0	0	0	0	1	0	1	0
29	145	V_5-V_2	0	0	1	1	1	0	1	1	0
30	150	V_5-V_5	0	0	1	0	0	0	1	0	1
31	155	V_5-V_4	0	1	0	0	0	1	0	0	0
32	160	V_5-V_2	1	1	1	1	0	0	0	0	1
33	0	0	0	1	1	1	0	0	0	1	1
34	-5	-(V_1)	1	0	0	1	1	1	1	0	0
35	-10	-(V_2-V_1)	1	1	0	1	1	1	0	1	0
36	-15	-V_2	0	0	0	0	1	1	1	1	0
37	-20	-(V_1+V_2)	0	0	1	0	1	1	1	0	1
38	-25	-(V_3-V_1)	0	1	0	0	1	0	0	0	0
39	-30	-V_3	1	1	1	1	0	0	0	0	1
40	-35	-(V_3+V_1)	0	1	1	0	1	0	0	1	1
41	-40	-(V_3+V_2)	1	0	0	1	0	1	1	1	1
42	-45	-(V_1+V_2+V_3)	1	1	0	0	1	0	0	0	1
43	-50	-(V_4-V_1)	1	0	0	1	0	1	1	1	1
44	-55	-V_4	1	1	1	1	1	0	1	1	1
45	-60	-(V_4+V_1)	1	0	1	1	0	1	0	0	0
46	-65	-(V_4+V_2)	1	1	0	0	0	1	1	0	0
47	-70	-(V_4+V_2)	0	1	1	0	0	1	1	0	0
48	-75	-(V_4+V_3)	0	0	1	0	0	0	0	1	1
49	-80	-(V_1+V_2+V_3+V_4)	0	1	0	0	1	0	0	1	1
50	-85	-(V_5-V_1)	1	0	0	1	1	0	0	0	1
51	-90	-V_5	1	1	0	1	1	1	1	1	0
52	-95	-(V_5+V_1)	1	1	1	1	1	1	0	1	0
53	-100	-(V_5+V_2)	0	0	1	0	0	0	1	0	0
54	-105	-(V_5+V_3)	0	1	0	0	1	0	1	1	1
55	-110	-(V_5+V_4)	0	1	1	0	0	0	0	0	1
56	-115	-(V_1+V_2+V_3+V_4+V_5)	1	1	1	1	1	1	0	0	0
57	-120	-(V_5-V_4)	1	0	0	0	0	0	0	0	1
58	-125	-(V_5-V_3)	0	0	1	1	1	1	1	1	1
59	-130	-(V_5-V_2)	1	0	0	0	1	0	1	1	1
60	-135	-(V_5-V_3)	1	1	0	1	0	1	0	1	0
61	-140	-(V_5-V_2)	1	0	0	1	0	1	1	0	0
62	-145	-(V_5-V_2)	0	1	1	0	1	0	1	0	0
63	-150	-(V_5-V_5)	0	0	1	0	1	0	1	0	1
64	-155	-(V_5-V_4)	0	1	1	1	0	0	0	1	0
65	-160	-(V_5-V_3)	1	1	1	1	1	1	0	1	1

The following table illustrates the comparison of multi-level inverter.

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TABLE.1 COMPARISON OF MULTILEVEL INVERTER

Inverter configuration	Diode Clamped	Flying Capacitor	Cascaded H-Bridge
Main switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-2)	0	0
Dc bus capacitors	(m-1)	(m-1)	(m-2)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

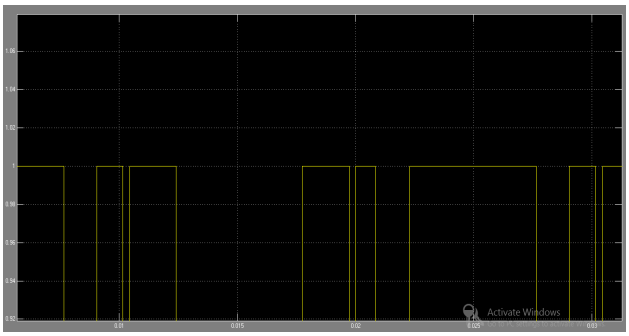
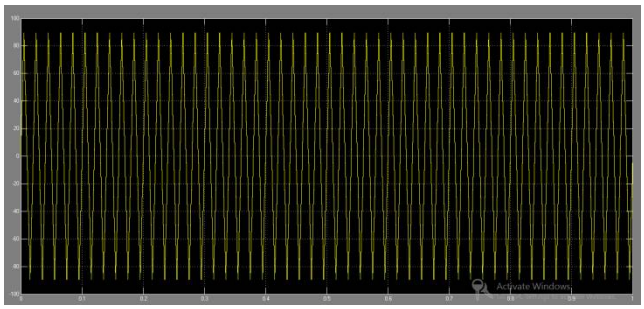


Fig.9 Output Pulse Given To Switches



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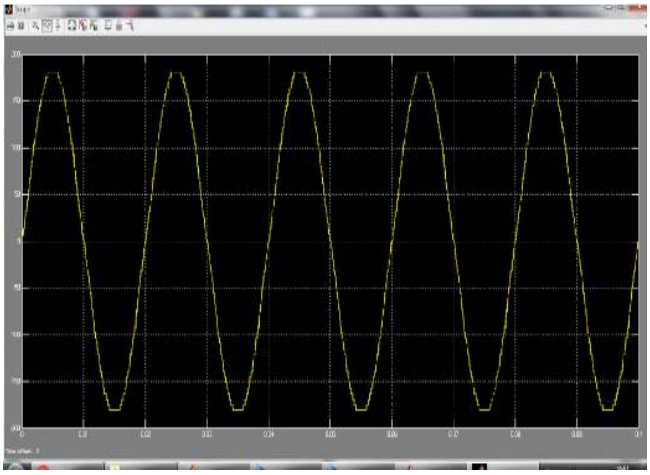

(b)

Fig.10 Output Voltage of 64-Level Inverter

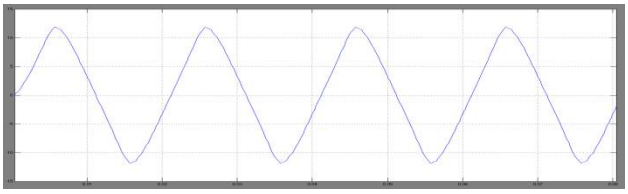

Fig.11 Output Current Waveform

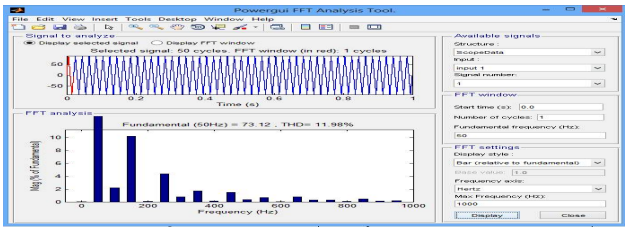

Fig.12 FFT Analysis

IV. CONCLUSION AND FUTURE SCOPE

The proposed system which utilizes four asymmetric dc sources and twelve power switches with resistive load. By proper switching sequence, the proposed inverter produces a 65 level output voltage with low switching losses; by operating the switches at fundamental frequency. The advantages of the proposed inverter are; reduction of number of switches, reduction of gate driver circuits, reduction of isolated power supply unit for gate diver, lower EMI and less harmonic distortion in the inverter output voltage. The computer aided simulation study has been carried out to validate the performance of proposed inverter. The proposed inverter can be recommended for distributed generators, stand alone and grid connected renewable energy power conversion applications.

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Further, the study has been extended to next phase II, by developing experimental set-up to validate the simulation results of phase I.

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