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Narrow Bus Encoding For Low-Power DSP Systems Using Universal Rotate Inverter Coding

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ABSTRACT: Power dispersal is an essential outline requirement in the present CMOS-VLSI plan and is tended to generally by the analysts over the globe. Switching/Exchanging action is one of the components that influence dynamic power in a chip and a few researches/productions have recommended different methods to lessen the same. Decrease of exchanging movement in the buses achieves importance as bus width, bus capacitance and the clock are recording consistent uptrend. In this paper, we propose a system for bus encoding, which, decreases the number of changes/transitions on the bus and performs superior to the current strategies, for example, bus alter coding what's more, move modify coding for irregular information as far as exchanging/switching action, without the requirement for additional overhead in calculation and circuit. Be that as it may, independent of the bus width it needs three additional bits and does not accept anything about the idea of the information on the bus.

KEYWORDS: CMOS-VLSI, Switching/Exchanging Action, Bus-Encoding, Power Dispersal, Low-Power-Plan.

I. INTRODUCTION

Power dispersal in CMOS circuits is a noteworthy worry for VLSI outline. The power scattering in CMOS can be grouped in to two kinds, to be specific, dynamic and static power dissemination. While the static power dispersal is caused by spillage streams in transistors the significant segments of dynamic power scattering is exchanging force and short out power. Exchanging power is dispersed when there is a progress from 1 to 0 or from 0 to 1. The likelihood of such change is called exchanging movement.

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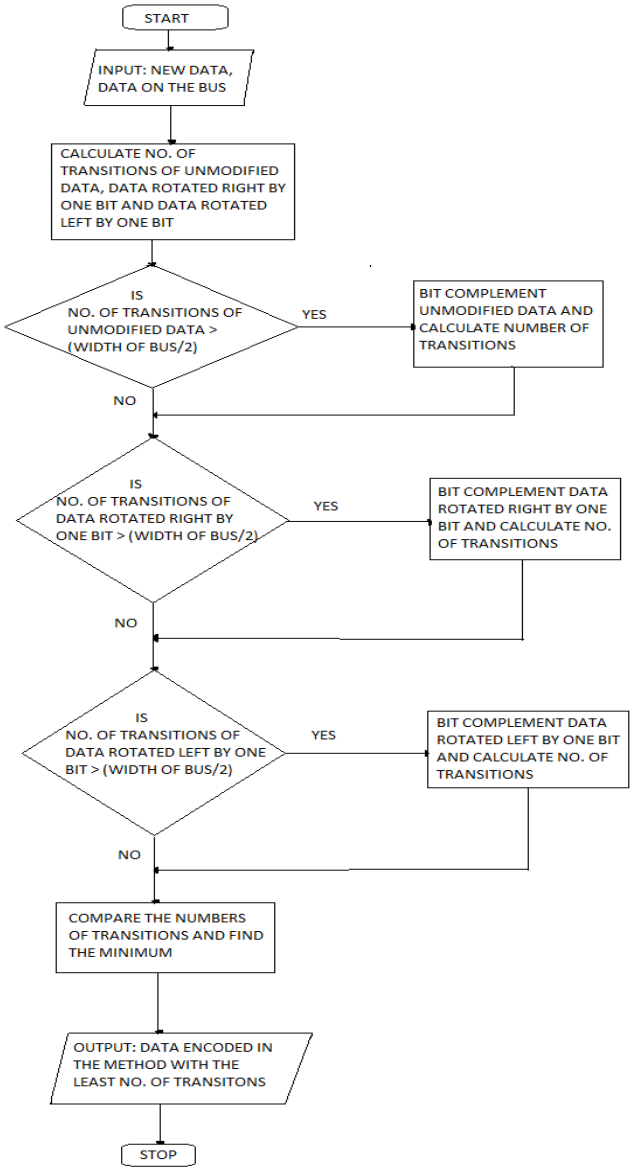

Fig.1 System Flow Diagram

We can express the dynamic power as:

$$Pd = {}^{a}.V2ddCLFClk \qquad (1)$$

Where, Pd = Dynamic power dispersal, ^{a} = Switching action, V2dd = Power supply, CL = Load Capacitance, FClk = Clock Frequency.

The condition for control dissemination in a transport is as per the following:

$$Pdbus = ({}^{a}.V2ddCLFClk)N \qquad (2)$$

Where = Width of the transport. Deriving from the above condition, the power dissemination in a transport relative to the exchanging movement and the width of the transport.

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A. Proposed Methodology

In the proposed strategy, numerous choices will be investigated and weighed to see which procedure will give the base number of exchanging and the system so chose will be put on the bus. The sort of coding so chose will be conveyed to the recipient by three extra bits. The choices attempted are recorded cry:

- ✓ Invert or bit supplement
- ✓ Rotate left by one piece
- ✓ Rotate appropriate by one piece
- ✓ Rotate left by one piece and upset
- ✓ Rotate appropriate by one piece and modify

In spite of the fact that the initial three choices were at that point announced, we add the last two strategies to get a coordinated approach and as found in the later piece of dialog, the mix comes about better exchanging proficiency. The way toward encoding is as per the following. Unmodified information is encoded utilizing turn ideal by one piece and pivot left by one piece codes. The quantity of changes between the unmodified information and the information on the bus are registered. This number of changes is contrasted and a large portion of the bus width (n/2), to check whether it is more noteworthy than n/2 or not. In the event that this number of advances is more prominent than n/2 then the unmodified information is encoded utilizing the modify code. The quantity of advances between this altered information and the information on the bus is ascertained.

The quantity of changes between the information turned ideal by one piece and the information on the bus is processed. This number of advances is contrasted and a large portion of the bus width (n/2), to check whether it is more noteworthy than n/2 or not. On the off chance that this number of changes is more prominent than n/2 then the information turned ideal by one piece is transformed. The quantity of advances between the information pivoted ideal by one piece and upset and the information on the bus is ascertained. The quantity of changes between the information pivoted left by one piece and the information on the bus is processed. This number of advances is contrasted and a large portion of the bus width (n/2), to check whether it is more prominent than n/2 or not. In the event that this number of advances is more noteworthy than n/2 then the information pivoted left by one piece is modified. The quantity of advances between the information pivoted left by one piece and altered and the information on the bus is computed. Since the quantities of changes are restrictively registered for any given case, we have three quantities of advances to be looked at. These three quantities of advances are analyzed and minimal number of changes is discovered. The encoding strategy comparing to this minimum number of advances is utilized to encode the information and it is sent over the bus. At the less than desirable end, the collector must be told as to which technique has been utilized to encode the information being sent over the bus. Since there are six unique kinds of information, at least three additional bits are required to demonstrate to the recipient who of them is being sent.

Table.1 Control Bit Representation for Proposed Technique

Bit representation	Method
000	Unmodified data
001	Invert / Bit complement
010	Rotate left by one bit
011	Rotate right by one bit
100	Rotate left by one bit and invert
101	Rotate right by one bit and invert

At the receiving end, the receiver must be notified as to which method has been used to encode the data being sent over the bus. Since there are six different types of data, a minimum of three extra bits are required to indicate to the receiver which of them is being sent. The binary codes used to identify the type of encoding selected in this technique are shown in table-1.

B. Proposed Algorithm Design

The algorithm for the proposed method is as follows:

```
Procedure rotate_inv()
{
Input: n_d, d_b, w
```

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Output: r_i_d
N= no. of transitions (n_d, d_b)
If (N > w/2)
{
N_I= no. of transitions (n_d(invert), d_b)
}
N_R= no. of transitions (n_d(rotate right), d_b)
If (N_R > w/2)
{
N_R_I= no. of transitions (n_d(rotate right & invert), d_b)
}
N_L= no. of transitions (n_d(rotate left), d_b)
If (N_L > w/2)
{
N_L_I= no. of transitions (n_d(rotate left & invert), d_b)
}
r_i_d= one of (n_d, n_d(i), n_d(rl), n_d(rr),
n_d(rli), n_d(rri)) depending on minimum(N, N_I, N_L, N_R, N_L_I, N_R_I)
}
In the given algorithm,
'n_d' is the new input data
'd_b' is the data on the bus
'w' is the width of the bus
'r_i_d' is the encoded data which will be sent on the bus
'N' is the number of transitions between the new input data and the data on the bus
'N_I' is the number of transitions between the inverted data and the data on the bus
'N_L' is the number of transitions between the data rotated left by one bit and the data on the bus
'N_R' is the number of transitions between the data rotated right by one bit and data on the bus
'N_L_I' is the number of transitions between the data rotated left by one bit and inverted and the data on the bus
'N_R_I' is the number of transitions between the data rotated right by one bit and inverted and the data on the bus.

The algorithm computes the number of transitions between the data on the bus and the six different types of data conditionally. The type of data which gives the least number of transitions is sent on the bus.

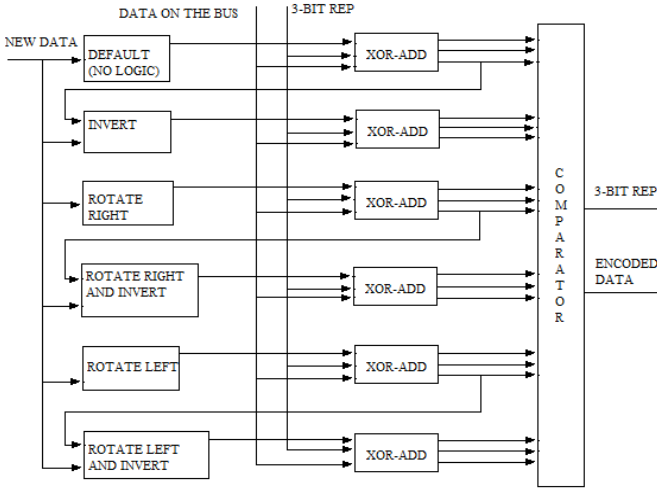

Fig.2 Basic Hardware Replication

C. System Flow Summary

✓ The inputs to the flow chart are the new data (unmodified data) and the data on the bus.

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- ✓ This unmodified data is rotated right by one bit and rotated left by one. The respective numbers of transitions are calculated by comparing these three types of data with the data on the bus.
- ✓ Then we decide whether the number of transitions of the unmodified data is greater than half the width of the bus or not.
- ✓ If YES, we invert or bit complement the unmodified data and compute the number of transitions between the inverted data and the data on the bus. If NO, then we move on to the next decision block. The output of the above mentioned block is also connected to this decision block.
- ✓ In this decision block we decide whether the number of transitions of the data rotated right by one bit is greater than half the width of the bus or not.
- ✓ If YES, we invert the data rotated right by one bit and calculate the number of transitions between the data rotated right by one bit and inverted and the data on the bus.
- ✓ If NO, then we move on to the next decision block. The output of the above mentioned block is also connected to this decision block.
- ✓ In this decision block we decide whether the number of transitions of the data rotated left by one bit is greater than half the width of the bus or not.
- ✓ If YES, we invert the data rotated left by one bit and calculate the number of transitions between the data rotated left by one bit and inverted and the data on the bus.
- ✓ If NO, then we move on to the next block. The output of the above mentioned block is also connected to this block.
- ✓ For any given case we need to compare only three numbers of transitions because they are computed conditionally.

II. LITERATURE SURVEY

In the year of 1994 the authors "C. L. Su, C. Y. Tsui, and A. M. Despain" proposed a paper titled "Saving power in the control path of embedded processors [1][4]" in that they described such as: CMOS circuits consume power during the charging and discharging of capacitances. Reducing switching activity then, saves power in embedded processors. The authors' two-pronged attack uses Gray code addressing and cold scheduling to eliminate bit switches.

In the year of 2004 the authors "Jun Yang, Rajiv Gupta, Chuanjun Zhang" proposed a paper titled "Frequent Value Encoding for Low Power Data Buses [3][5]" in that they described such as: Since the I/O pins of a CPU are a significant source of energy consumption, work has been done on developing encoding schemes for reducing switching activity on external buses. Modest reductions in switching can be achieved for data and address buses using a number of general purpose encoding schemes.

However, by exploiting the characteristic of memory reference locality, switching activity on the address bus can be reduced by as much as 66%. Till now no characteristic has been identified that can be used to achieve similar reductions in switching activity on the data bus. We have discovered a characteristic of values transmitted over the data bus according to which a small number of distinct values, called frequent values, account for 32% of transmissions over the external data bus. Exploiting this characteristic we have developed an encoding scheme that we call the FV encoding scheme. To implement this scheme we have also developed a technique for dynamically identifying the frequent values which compares quite favorably with an optimal offline algorithm.

Our experiments show that FV encoding of 32 frequent values yields an average reduction of 30% (with on-chip data cache) and 49% (without on-chip data cache) in data bus switching activity for SPEC95 and mediabench programs. Moreover the reduction in switching achieved by FV encoding is 2 to 4 times the reduction achieved by the bus-invert coding scheme and 1.5 to 3 times the reduction achieved by the adaptive method. The overall energy savings on data bus we attained considering the coder overhead is 29%.

In the year of 2001 the authors "S. Komatsu, M. Ikeda, K. Asada" proposed a paper titled "Bus Data Encoding with Couplingdriven Adaptive Code-book Method for Low Power Data Transmission [7][13]" in that they described such as: Reducing bus power dissipation has become one of key issues for low power System on a Chip (SoC) design. In this paper we have proposed bus data encoding schemes, which reduce coupling signal transitions of bus lines along with self signal transitions, based on adaptive code-book method.

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Experimental results show that proposed encoding schemes reduce effective signal transitions related to power dissipation as much as 25-50% in a 16-bit bus, which indicate the proposed scheme is suitable for IPs in future SoC designs.

III. EXPERIMENTAL RESULTS

The following table illustrates the Area Analysis scenario of the proposed work.

```
=========================================================================
Final Results
RTL Top Level Output File Name     : BinryCount73.ngr
Top Level Output File Name         : BinryCount73
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 10

Cell Usage :
# BELS                             : 8
#      LUT3                        : 8
# IO Buffers                       : 10
#      IBUF                        : 7
#      OBUF                        : 3
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s100evq100-5

 Number of Slices:                        4  out of    960     0%
 Number of 4 input LUTs:                  8  out of   1920     0%
 Number of IOs:                          10
 Number of bonded IOBs:                  10  out of     66    15%
```

Fig.3 Area Analysis Scenario

The following figure illustrates the encoder result of the proposed work.

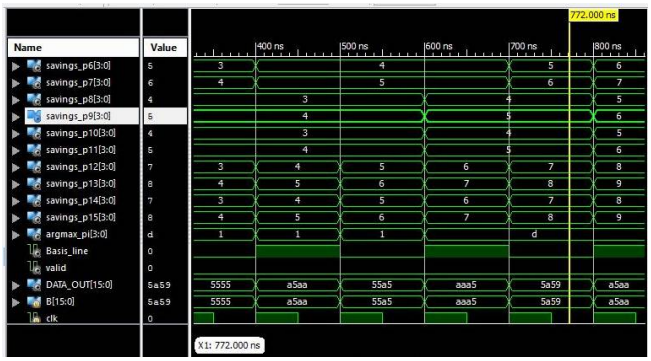

Fig.4 Encoder Result

The following figure illustrates the Decoder outcome of the proposed work.

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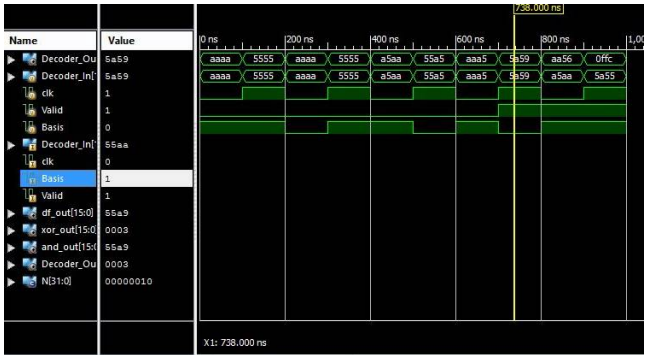

Fig.5 Decode Result

The following figure illustrates the LUT Count of the proposed work.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4	960	0%
Number of 4 input LUTs	8	1920	0%
Number of bonded IOBs	10	66	15%

Fig.6 LUT Count

The following figure illustrates the Multiplier RTL Perception of the proposed work.

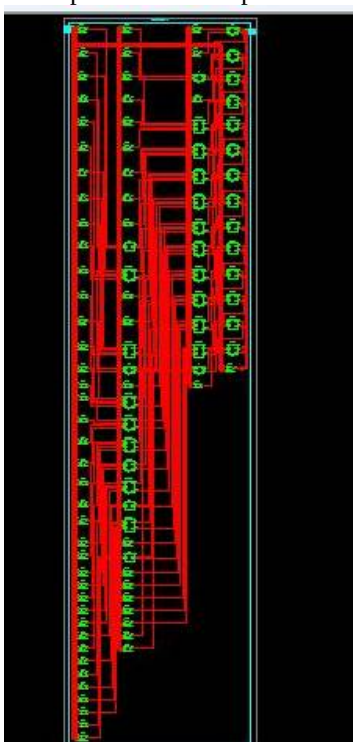

Fig.7 Multiplier RTL View

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The following figure illustrates the Power Analysis summary of the proposed work.

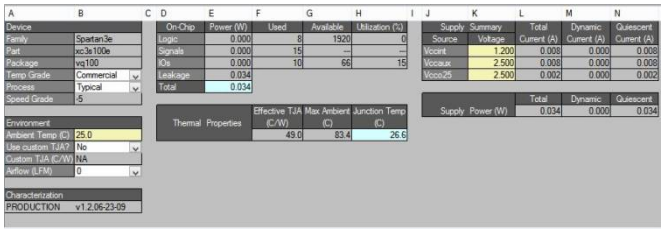

Fig.8 Power Analysis

V. CONCLUSION

The proposed procedure shows noteworthy lessening in exchanging action regardless of the bus width, and is along these lines more power effective contrasted with the comparable existing plans for example, Bus-Invert and Shift-Invert methods. The method can be utilized for buss of any width what's more, it requires just three additional bits regardless of the width of the bus. The proposed strategy does not require additional calculation and equipment overheads when contrasted with the current strategies. As appeared in the stream diagram, the method restrictively encodes the information and henceforth its utilization of the equipment is enhanced. The decrease in the quantity of advances and subsequently the diminishment in unique power by this strategy is extremely critical. While holding the value of the proposed technique – diminishment in exchanging action – we have to investigate the likelihood for diminishment of equipment overhead. We have plans to execute region and control proficient circuit for the encoder and decoder. The system proposed comprises of six alternatives for diminishing the quantity of changes on the bus. We can likewise add T0 coding to make it really widespread. It should be possible without including additional piece for distinguishing proof in spite of the fact that requires some additional equipment.

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