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# Design of 8 bit Analog to Digital Converter (ADC) in 45 nm CMOS Technology

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**ABSTRACT***:* In the current technological world, the technology advancement leads most of the application demanding for a reduction in total size of the system in terms of space the space they occupied in any device. The Data converter section, besides being very power demanding and it is also usually extremely power demanding in comparison with other blocks of any architecture and that's why low power has also become a tough requirement in most of the system being maintained in a low figure has almost become a mandatory specification in many application. In this thesis work we have chosen the SAR control logic architecture as it one of the very successful moderate resolution achievable converter systems available among all the data converter control logic architecture. Initially we encounter the different types of SAR control logic and focuses on selection of suitable comparator architecture and SAR Control Logic and DAC based on this analysis, dynamic two-stage comparator, SAR Control Logic and BWC Capacitive Array as DAC is selected due to its energy efficiency and capability of working in low supply voltages and consume Low Power and the schematic model of the entire system will try to implement using EDA tool Micro wind 3.5 and DSCH in order to fulfill the technical requirement of the project.

**KEYWORDS:** SAR, ADC, EOC, DAC, S/H.

## I.INTRODUCTION

Although in now continually changing technological world as all the electronics components are goes tiny day by day and large numbers of devices and micro-controllers are coming everyday it is necessary for all the supporting component of the devices and micro- controller to be fitted as per their requirement and specifications. In order to follow the trend of new technologies to become tiny and to be the better then the previous version and updating the old version with the new it is also essential for the Analog to Digital comparator to update themselves as per the trends. As per the previous fabrication technique all the Analog to Digital converters are mostly fabricated with the foundry of 120 nanometer technique and above than 120 nanometer i.e. 180nanometer etc. So in order to adapting the new technological revolution Analog to Digital converter also have to fabricate on lower scale than its previous foundry and in order to getting this we are going to design the Analog to Digital Converter with lower scale than 120 nanometer, which is 45 nanometer.

In this work we studied the each block diagram of ADC and construct these with the help of EDA tool. In order do to so we started with the Comparator block diagram and studied the different type of Architecture of comparator i.e open loop comparator, Latch comparator and Dynamic latch Comparator but we found that dynamic latch comparator introduces less delay and low power consumption so we further studied the different type of comparator i.e. N-type latched comparator, dynamic two stage latched comparator and modified two stage latched comparator and we also simulate these using different kind of Set-Reset latch i.e. NAND SR latch and NOR SR latch and on the basis of result we found that dynamic two stage comparator has low power consumption along with the low delay and then after that we proceed with the SAR control logic and we had the two methods for design the SAR logic and on the basis of previous work we found that SAR control logic proposed by Anderson consume the less power and we proceeds with this logic and we select the Binary Weighted Capacitor array over the resistive array as our DAC functional block among the Two stage weighted capacitor array and C-2C capacitor array as it also has the low power consumption which is our first priority. All these schematic architecture were simulated using the EDA tool Micro

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wind and DSCH in the 45 nanometer foundry and after inserting these functional block diagram we further construct the functional Analog to Digital Converter

## II. IMPLEMENTATION OF ADC

### *A. Comparator Implementation*

We studied the different type of Architecture of comparators i.e. open loop comparator, Latch comparators and Dynamic latch Comparators but we found that dynamic latch comparator introduces less delay and low power consumption so we further studied the different type of comparator i.e. N-type latched comparator, dynamic two stage latched comparator and modified two stage latched comparator and we also simulate these using different kind of Set-Reset latch i.e. NAND SR latch and NOR SR latch and on the basis of result we found that dynamic two stage comparator has low power consumption along with the low delay The power consumption and time delay comparison is given in below figure.

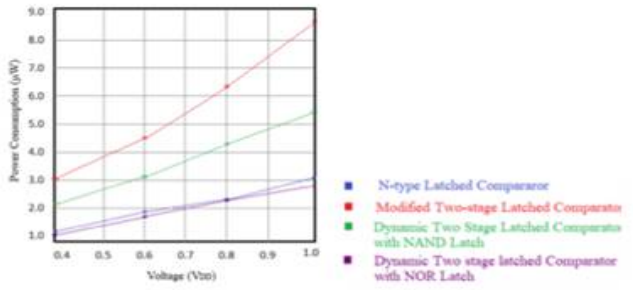


Figure 2.1 Power Consumption Comparisons

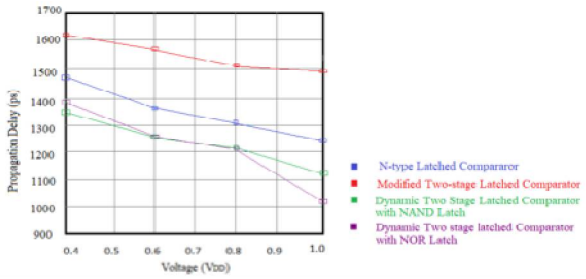


Figure 2.2 Time Delay Comparison

Since the Priority is the Power Consumption and Time Delay, Dynamic two stage Latched Comparator with the NOR latch Consumes minimum power and it has the lowest Time delay as shown in the figure 3.32 and 3.33 so in the fabrication of 8 bit Analog to Digital Comparator we used the Dynamic two stage latched comparator.

### *B. SAR Control Logic Implementation*

We found two different types of approaches to designing the SAR logic. The first one is proposed by Anderson consists of a ring counter and a shift register. At least 2N flip flops are employed in this kind of SAR [16]. The other, which is proposed by Rossi, contains N flip flops and some combinational logic [17].As Anderson's Proposed method consist of a ring counter and a shift register and Non- redundant SAR logic consists a combinational logic and flip flops but the logic proposed by Anderson has the low Power consumption[18] as explained in figure 2.3 [18].

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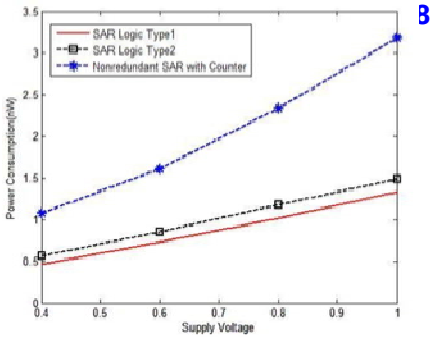


Figure 2.3 SAR Comparison of Average power vs. scaled supply voltage [18]

Since our priority is about Low Power Consumption so we consider the type 1 SAR logic which is proposed by the Anderson. The SAR architecture proposed by the Anderson is explained in the figure 2.4

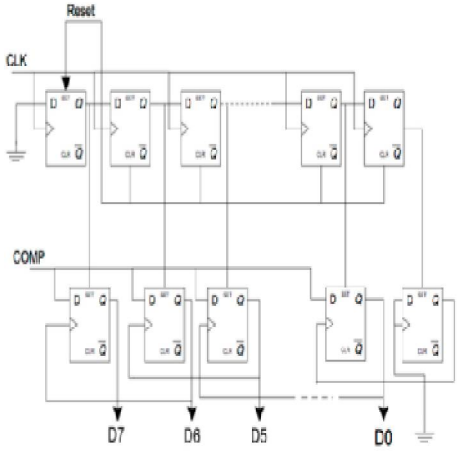


Figure 2.4 SAR Architecture

We implement the SAR Control logic using the EDA tool DSCH and Micro wind and simulate it and its simulation is stated below in figure 2.5 and it has the power consumption of 12.067µW.

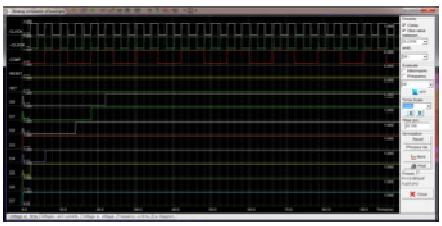

Figure 2.5 SAR Simulation Waveform

*C. DAC Implementation*

In this thesis a 8-bit charge-redistribution DAC with Binary Weighted Ccapacitor array was implemented in 45nm CMOS process. Figure 2.6 shows the block diagram of the 8-bit DAC we used in order to fabricate the 8 bit ADC.

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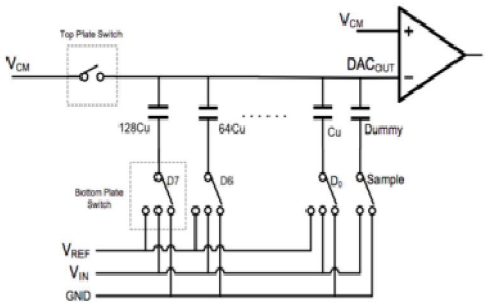


Figure 2.6 DAC schematic View

The Output of the DAC is defined by the equation described below:

$$V_{out-DAC} = -V_{IN} + V_{CM} + D_7\frac{V_{REF}}{2} + D_6\frac{V_{REF}}{4} + \ldots$$
$$\ldots\ldots + D_1\frac{V_{REF}}{2^7} + D_0\frac{V_{REF}}{2^8}$$

The linearity of ADC is restricted by the linearity of the DAC which is caused by the capacitor mismatch. Therefore, choosing an appropriate value for the unit capacitance is vital. Reducing the unit capacitance value improves the linearity but deteriorates the noise performance at the same time due to KT/C thermal noise. The minimum value of the unit capacitor is limited by several factors including KT/C thermal noise, capacitor matching and the value of the parasitic capacitances [21]. A unit capacitance of 20fF is chosen in this design. The values of the other capacitors in the capacitor array are defined based on the unit capacitance.

## III.PERFORMANCE EVOLUTION

We studied two different types of architecture of SAR Analog to Digital Comparator i.e. Separate Sample and Hold Circuit and Charge Redistribution Architecture of ADC but the main drawback of 'Separate DAC and Sample and Hold circuit ADC' is that it consume more power due to separate Sample and Hold circuit and as our concern is about the low power consumption we cannot use this design and we moved to the 'Charge Redistribution Architecture ADC' which has a different approach as this architecture encompasses a capacitive DAC which also operates as a sample and hold circuit. Figure 3.1 represents the test bench for ADC performance measurement.

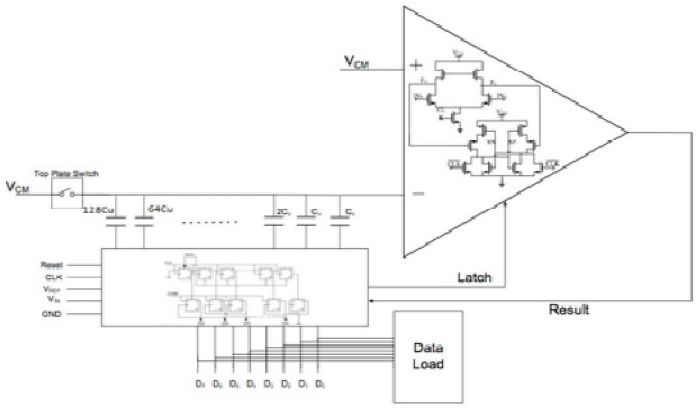


Figure 3.1 SAR ADC test bench

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We first design the high level schematic of the SAR ADC using the charge redistribution architecture and further replace the blocks by the chosen schematic circuits and construct the ADC using EDA tool Micro wind and DSCH. The ADC is simulated with $V_{DD}$= 1V, $V_{REF}$ =$V_{CM}$ = 0.5V, and clock period of 4ns and sample frequency of 500MHz and The input signal is a full swing sinusoidal with $f_{in}$= 250MHz. We simulatee results under 27°C and the total power consumption are of 683µW.

| Block | Power Consumption at 27°C (µW) |
|---|---|
| Comparator | 2.844 |
| SAR | 12.067 |
| DAC | 632.329 |
| Clock Power | 35.96 |
| Total | 683.2 |

DAC consumes the largest amount of power among other blocks which is 92.5%. As discussed above, the unit capacitance in the DAC is chosen to be 20 fF. After DAC, SAR control logic with 1.766%, clock power consumes 5.26% and comparator with 0.41% consumes the largest amount of power respectively.

## IV. CONCLUSION

This Projects presents implementation of a 8-bit SAR ADC operating at 500MS/s and supply voltage of 1 V in 45nm CMOS technology. The power consumption of 684µW is achieved. The ADC employs charge- redistribution DAC, a dynamic two-stage comparator, and a SAR control logic containing a sequencer and a ring counter. In this work, after a deep study on different possible structures of SAR logic, they are implemented and compared in terms of power consumption and speed. Comparison results obtained indicate that the designed conventional SAR logic with a sequencer and a ring counter, consumes the lowest power of 12.067µW at 500MS/s. Thus the power consumption of the SAR control logic is significantly reduced and consumes only 1.766% of the total power. The design of comparator is also a crucial part of ADC design In this work, comparator performance metrics as well as several types of comparators are studied, such as open loop comparator, pre-amplifier preceding a latch comparator, and dynamic comparator. Based on these studies, dynamic comparators consume lower power compared to the other approaches. Therefore, diverse architectures of dynamic comparators are implemented and compared regarding power consumption, speed, and accuracy. Consequently, the dynamic two-stage comparator is selected to be used in the designed ADC.

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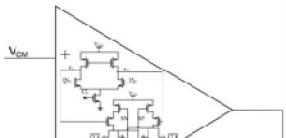

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