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Low Power & High Speed Optimization with hybrid Multibit Flip –Flops and Look Ahead Clock gating for VLSI Circuits

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ABSTRACT: Power has become a burning issue in trendy VLSI style and integrated circuits. In this paper we present a power optimization technique to reduce clock power by using hybrid of multi bit flop flop method and look ahead clock gating. Data-Driven Clock-Gating (DDCG) and Multi Bit Flip-Flops (MBFFs) in which several FFs are grouped and share a common clock driver are two effective low-power design techniques. Clock signal is considered as a great source of power dissipation in synchronous circuits because of high frequency and load.It does not carry any information but consumes high power at the switching activity which is to be avoided. So,by using clock gating we can save clock power by reducing unnecessary switching activity inside the gated module.Hence modified design of data driven clock gating and look ahead clock gating is designed to obtain the less power in the circuits.These two techniques are compared among them and by the results obtained through cadence virtuoso tool we can conclude that look ahead clock gating consumes low power,low noise response and higher performance.

KEYWORDS: Multibit Flipflop, Clock gating, DDCG, LACG.

I.INTRODUCTION

Due to the popularity of portable electronic products, Low power system has attracted more attention in recent years. Reducing the power consumption not only can enhance battery life but also can avoid the overheating problem, which would increase the difficulty of packaging or cooling. Moreover, in modern VLSI designs, power consumed by clocking has taken a major part of the whole design.. Given a design, the power consumed by clocking can be reduced further by hybrid multi-bit flip-flops method and Look ahead clock gating method. Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. The major dynamic power consumers in electronic product is the system's clock signal.

The data of digital systems are usually stored in flip-flops (FFs),each of which has its own internal clock driver. In an attempt to reduce the clock power, several FFs can be grouped into a module called a multibit FF (MBFF) .In many cases, transition of the clock causes a great deal of irrelevant gate activity. Thus, the dynamic power can be greatly decreased by reducing the clock power dissipation.So that, circuits are being developed with administrable clocks.Hence Clock gating can be enforced at all levels like system architecture, block design, logic design, and gates.So,this will allow the clock signal to be applied in the circuit in the controllable level. The clock signal applied to a flipflop is disabled when the flipflop state is not allowed to shift in the next clock cycle period. To reduce the aerial of the gating logic,several flip flops are combined and given the clone clock signal for all its operation.The combined all flipflop are named as multibit flipflop which also provides way for lesser power consumption in the electronic devices.In this paper, we present data driven clock gating and look ahead clock gating with modified design in the cadence virtuoso tool to obtain very low power,low noise response,lesser delay,lesser bandwidth and efficient reliability in the electronic devices.The power consumption detail is obtained accurately in the cadence virtuoso power calculator window and the noise response is also calculated using the same calculator window.The DC response analysis is also obtained for the modified design.

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II. RELATED WORK

The proposed data driven clock gating is defined by its operation in a very clear manner.A FF finds out that its clock cannot be applied in the next cycle by XORing its output with the present data input that will also be presented at its output in the next cycle. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, where those gating signals are latched to avoid glitches. In existing method, combinational logic which is a combination of a latch with AND gate is used and is named as integrated clock gating.The modified part of this paper is that the combinational logic circuit used in the existing method is replaced by half Adder circuit which provides the clock enabling/disabling signal for the flipflop at the change of its each state in the circuit.The half adder logic does not provide the clock signal to the flipflop when the previous output of the flipflop and the present input of the flipflop are at same state.So that the clock power is not supplied to the flipflop because there is no change of state. So the previously given clock power itself is enough to supply for the flipflop operation.Additionally it is not needed to provide the clock signal again in the next clock cycle.The half adder logic gives the clock signal to the flipflop when the previous output of the flipflop and the present input of the flipflop are at different state that is toggle of the other input.So that the clock power is supplied to the flipflop because there is a change of state. So the previously given clock power is not enough to supply for the flipflop.Additionally,we need to provide the clock signal in the next clock cycle.By these logic at each clock cycle the power consumption is getting reduced which is required by all electronic circuits.The circuit diagram of the data driven clock gating is shown fig.1 which performs the operation that is explained above.This modified design is implemented in cadence virtuoso tool to analyse the power details,noise details and its other circuit parameters.

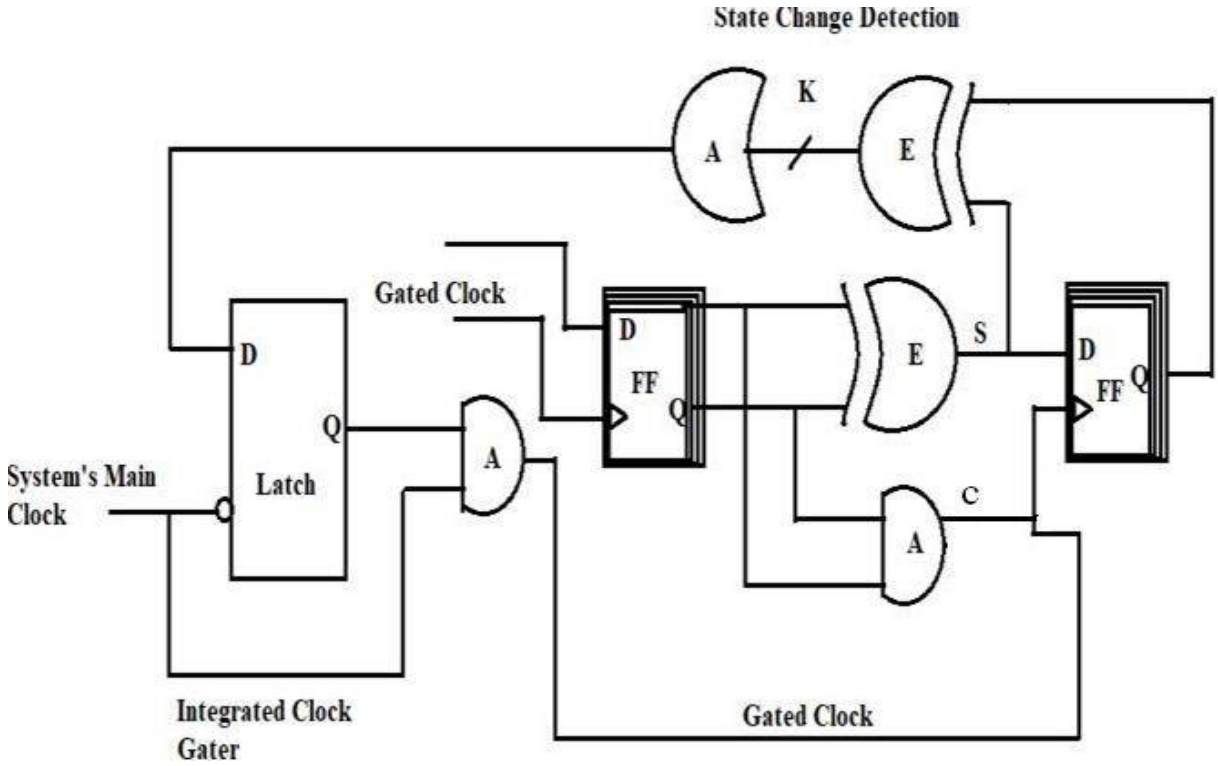

Fig 1.1. Data Driven Clock Gating

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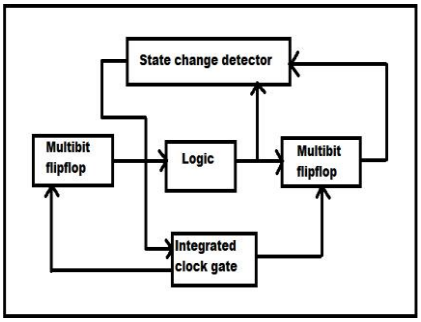

Fig 1.2. Block diagram data driven clock gating

In data driven clock gating the dynamic power consumption of synchronous digital system is reduced by minimizing the number of power is consumed by the clock signal.. In the data driven clock gating, clock is also not straight while minimizing the power consumption . Clock gating technique is one of the most important and it is widely used for reducing dynamic power consumption and minimizing of region. Clock gating is widely used technique for saving the clock power. The high switching activity is obtained in clock net which outcomes larger power dissipation in the adders . The clock net is produces a more power dissipation and it is avoided by removing clock in part of the device is known as clock gating. Clock gating technique is generally used to reduce power consumption by avoiding unwanted switching activity . Clock gating is prescribed at all levels like system architecture, logic design, gates and block design.

The OCV they implemented a clock gating in on-chip variations (OCV). The clock gating is carefully designed for successful timing closure under the influence of OCV which no longer guarantee the perfect result on clock. To implement an OCV on timing end the multi-level gated clock structure should be considered. Gated-clock design is one of the approaches to reduce the dynamic power consumption. The set of strategies termed DPM is used to reduce power consumption in a digital system. This strategy allows us disabling the logic circuits that functional operations are not performed during specified time slot. The FF clock will be disabled with an approach called gated-clock . The gated clock design approach is depending on the technological parameters of adopted gates and its offer a significant power reduction. By decreasing the number of clock gaters, we can achieve an extra power reduction. Look ahead clock gating is also another technique to achieve a more power reduction. In this, the output of XOR gate is clock enable signal (clk_en) which the present data input that will appear at the current output and the output of device. If current output and current input have different number therefore the clk_en is high and this is an active period. In slumber period, the clk_en is low then the current output and current input have similar values and the clock is not provided so it is gated.

III. PROPOSED METHOD

In this paper, we propose Look Ahead Clock Gating (LACG). It shows clock enabling signal at each flip flop. It depends on present cycle data same as data driven gating with MBFF method and the data driven is enable for full clock signal. Data Driven requires optimization of FF. The simplified gating implementation is Auto gated Flip flop. This is advance than data driven clock gating because the clock gating circuit consists of flipflop based circuit for gating the clock signal.Hence this reduces the majority of redundant clock pulses. It has a great advantage of avoiding the tight timing constraints data driven clock gating, by giving a full clock cycle for the enabling signals to be calculated and propagated to their gaters.The modified part of this paper is in the combinational logic that is present in the circuit diagram where a new logic called Half Adder is used as combinational part which provides the clock enabling/disabling signal for the flipflop at the change of its each state in the circuit.The half adder logic does not provide the clock signal to the flipflop when the previous output of the flipflop and the present input of the flipflop are

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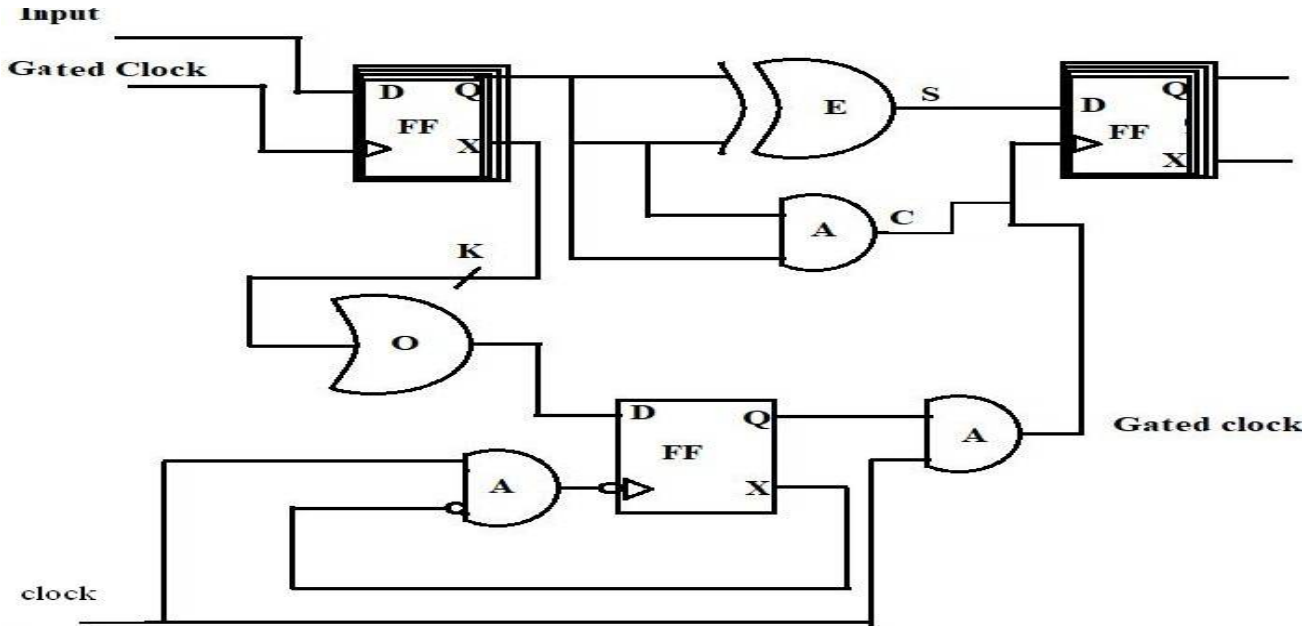

Figure 2. Look Ahead Clock Gating.

IV. APPLICATION DEVELOPED

The look ahead clock gating circuit takes an input clock signal and generates a gated clock based on a control signal. The look ahead clock gated clock signal is used to activate the arithmetic or logic or shift unit. It prevents unnecessary charging and discharging of the clock signal in inactive modules which leads to lower dynamic power dissipation. Look ahead clock gating technique is a power down methodology, which involves selectively clocking modules as and when required while keeping other inactive modules in sleep mode.LFSR is known as shift register whose input bit is precise

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function of its past state .The input to the LFSR comes from the XOR of particular bits of the register. The result is shifted into the leftmost bit of the register and the rightmost bit is shifted into the output. LFSR is a sequential circuit basically used in test pattern generators, Signature analysis and in Spread spectrum communications. In the applications like pseudo-random bit generators (PRBGs), LFSR is used to generate a pseudo random sequence. A good PRBG is identified by repeatability and randomness. Linear feedback shift registers are simple, but they consume a large amount of dynamic power. The circuit diagram of the linear feedback shift register without and with look ahead clock gating (LACG) is shown below

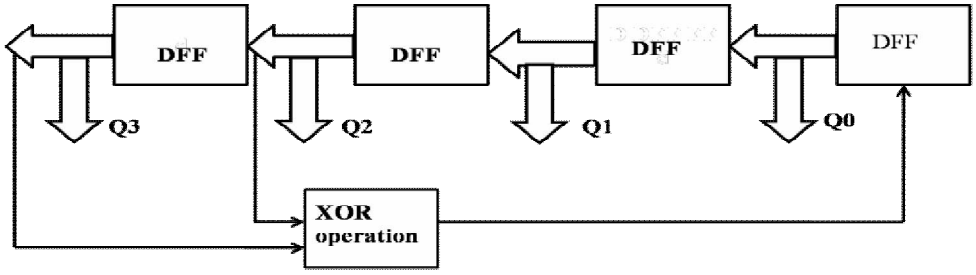

Figure 3. Schematic of LFSR without LACG Technique

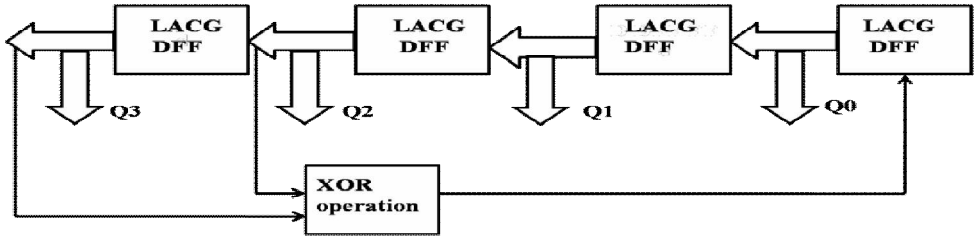

Figure 4. Schematic of LFSR with LACG Technique

V. SIMULATION RESULTS AND DISCUSSION

The following figures shows the implementation part for the modified data driven clock gating and look ahead clock gating methods and their power and noise reports. The below circuit diagrams are designed using cadence virtuoso tool.

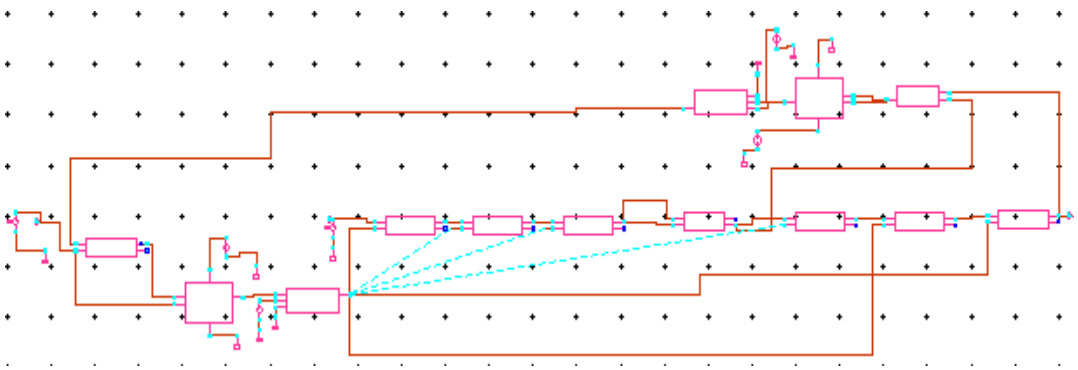

Figure 5. Data Driven Clock Gating in Cadence

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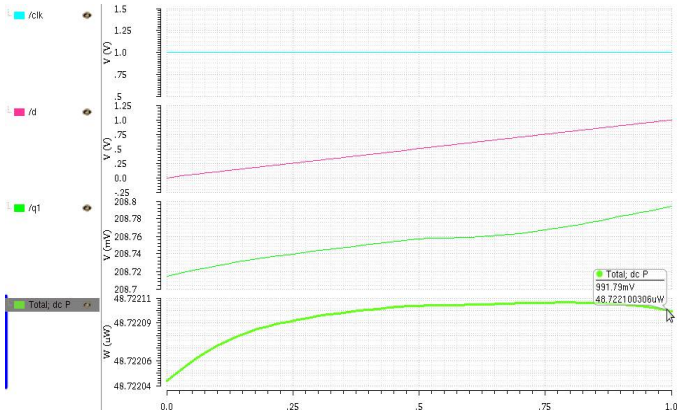

Figure 6. Power Response of data driven clock gating

Modified data driven clock gating circuit diagram implementation is shown in the above fig 5 and its respective power and noise waveforms in Fig 6 and 7. This modified data driven clock gating causes area and power overhead. The power consumption can be reduced by using clock gating technique. This modified data driven clock gating signals having proceedings to enable the clock signals. So,the flip flops and the latches are to be enabled by using the gate signals. The outputs from the XOR gates are ORed to give the combination of output joint gate signals from the flip flops and then latched to avoid the glitches presented inthe specified units. The clock of the flip flop can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the maximum setup time of the flip flop. Such constraints may exclude five percent to ten percent of the flip flops from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by down sizing or turning the transistors of non critical path to high threshold voltage for future power savings.

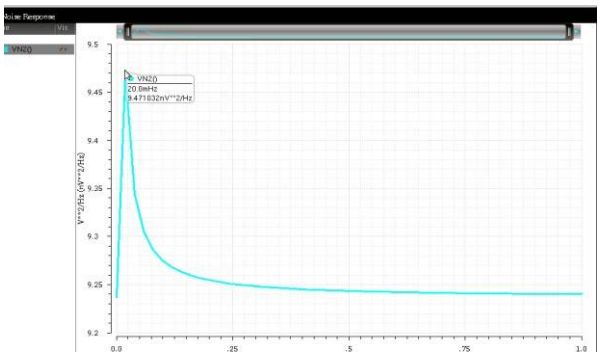

Figure 7. Noise Response of Data driven Clock Gating

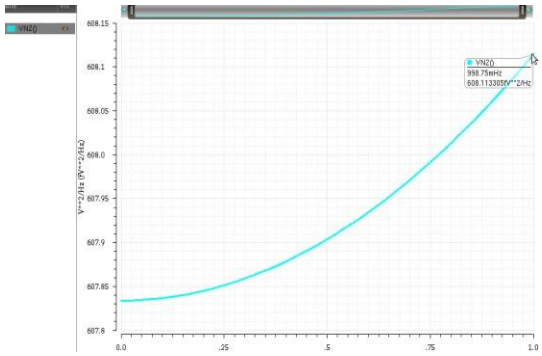

Figure 8. Noise Response of look ahead Clock Gating

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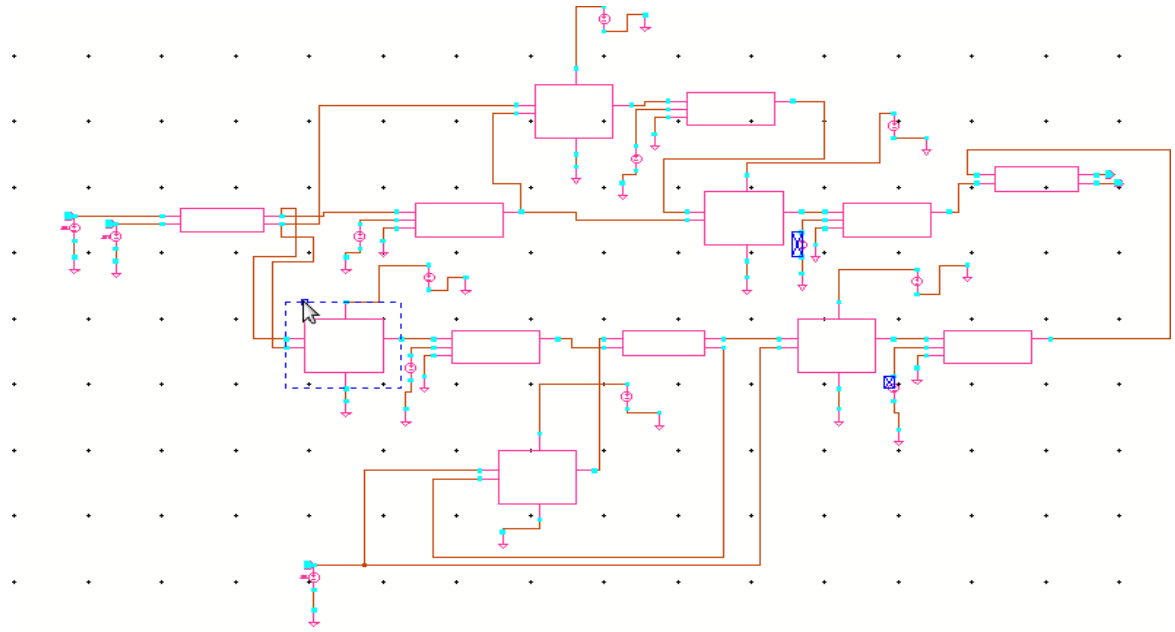

Figure 9. Look Ahead Clock Gating in Cadence

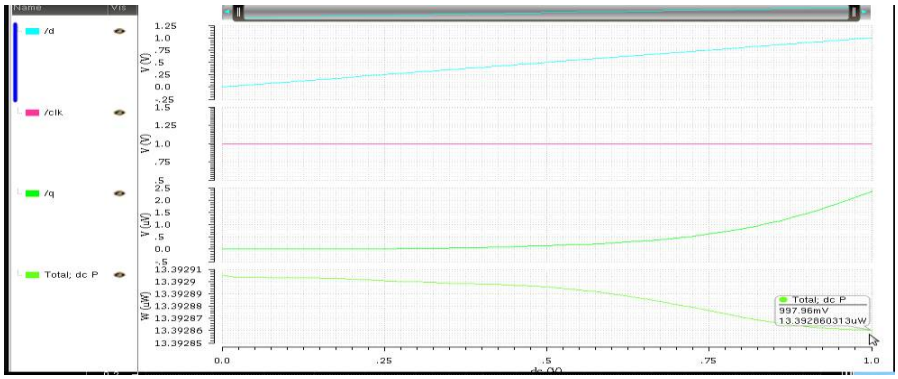

Figure 10. Power Response of Look Ahead Clock Gating

The above fig 9 shows the implementation of modified look ahead clock gating and and fig8 and fig10 shows the power analysis and noise report of modified LACG using cadence virtuoso tool.Data driven gating is suffered by short time- window. Data driven Clock gating is explained in Fig1. Design methodology is very difficult in data driven method. In order to maximize the power saving flip flop are grouped together. The main applications are unknown redundant clock pulses may increase in specific application. In this paper we propose Modified look Ahead clock Gating (LACG). It shows clock enabling signal at each flip flop depends on present cycle data same as data driven gating AGFF and data driven enable full clock signal but the combinational logic is different. Data Driven requires optimization of FF. The simplified gating implementation is Auto gated Flip flop.In modified Look ahead clcok gating Clock enabling signals are usually introduced by designers during the system and clock design phases, where the

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mutualities of the various functions are well established. In contrast, it is very difficult to define such signals in the gate level, especially in control logic, since the mutual among the states of the various flip flops depend on automatically synthesized logic. The modified Look ahead clock gating designed is very useful for reducing Clock switching power. Clock signal avoids timing constraints from existing clock gating methods are closed model of the power saving technique by Auto gated Flip flop is implemented in look ahead gating logic. The modified look ahead gating logic will optimize the FF for joint gating, the above discussed power can be saved when universal clock is given into the logic gates costuming of ff by group and yield high power saving this matter left for further research.

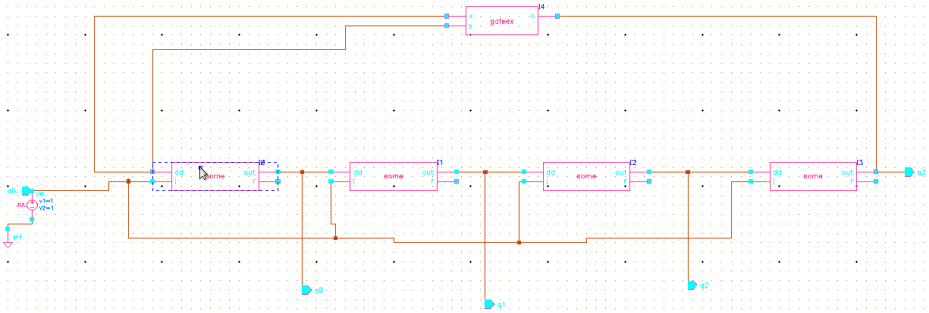

Figure 11. LFSR with LACG Clock Gating.

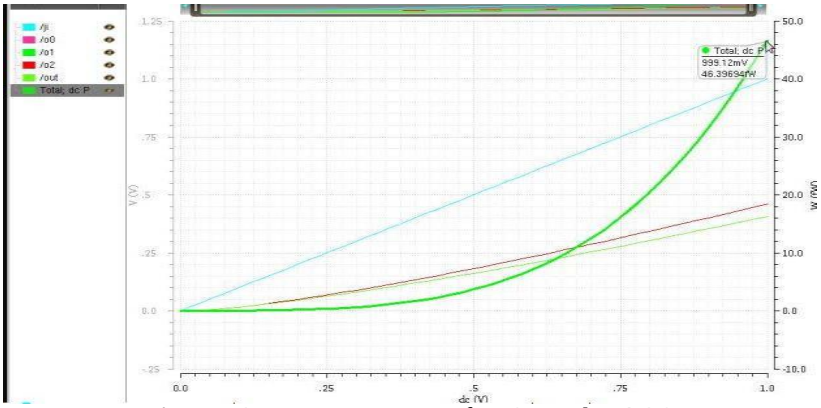

Figure 12. Power Response of LFSR with LACG

Fig11 and fig 12 shows the Application of modified look ahead clock gating in LFSR and power response by using cadence virtuoso tool. This modified look ahead clock gating finds the clock enabling signals of each flip flop one cycle ahead of time, based on information of the present data of flip flop on which it depends. This look ahead clock gating takes the auto gated flip flop a leap forward. It deals with three goals; taking the clock pulse in the master latch also, making it practical for large and general designs and avoiding the issues of timing constraints. The main objective of look ahead is to reduce the power consumption and this technique is considerably simpler.

TABLE I

S.NO	CLOCK GATING TECHNIQUES	TOTAL POWER	TOTAL NOISE
1.	Datadriven clock gating technique	48.7221uW	9.4710nV/sqrt(Hz)
2.	Look Ahead clock gating technique	13.39288uW	0.6081pV/sqrt(Hz)

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TABLE II

S.NO	LFSR	TOTAL POWER	TOTAL NOISE
1.	LFSR without look ahead clock gating	0.0 921pW	5.754nV/sqrt(Hz)
2.	LFSR with look Ahead clock gating	0.0463pW	1.126nV/sqrt(Hz)

The simulation results for the modified clock gating techniques were obtained and shown, in a 45nm technology at room temperature using cadence virtuoso tool. The following table I shows the power comparison results for the modified data driven clock gating and modified look ahead clock gating. Table shows that data driven clock gating consumes 48.7221uW and the look ahead clock gating consumes 13.39288uW which is less than the data driven clock gating. With the more reduction in the power consumed, the proposed technique is beneficial. The following table II shows the power comparison results for application developed by using modified look ahead gating.The modified design of data driven clock gating and look ahead clock gating is designed using cadence virtuoso tool and the power result is obtained which is compared as shown above in the table.As well as noise is also compared and it is found that look ahead clock gating is the best suitable clock gating technique with efficient performance.This clock gating can disable the redundant clock pulses in the devices and pave the way for low power devices in the electronic world.This can be applied at all sequential level circuits where clock power is a great source of power dissipation.

VI. CONCLUSION

The modified clock gating will increase the performance and reduce the dynamic power consumption. The modified Look-Ahead Clock Gating reduces the power by reducing the ON period of the device based on computing the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. In this work, the design is done to overcome the drawback of data driven clock gating ,that is stop the majority of redundant clock pulses. The power analysis and noise analysis of modified look-ahead clock gating is observed. From the analysis, it's found that the modified method consumes less power when compared to the conventional method.

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