ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

VLSI Implementation of Binary to Gray Converter Using Asynchronous Circuits in FPGA

E. Rajalakshmi[1], A. Jossie Pushpa[2], T. P. Deepikajee[3].

Assistant Professor, Department of ECE, Mepco Schlenk Engineering College, Virudhunagar, Tamil Nadu, India[1.]

UG student, Department of ECE, Mepco Schlenk Engineering College, Virudhunagar, Tamil Nadu, India [2,3.]

ABSTRACT: This paper presents a simple implementation method of pipelined asynchronous circuits. Asynchronous systems may have some advantages such as lower power consumption, no clock skew. The essential component of the proposed method is the asynchronous pipeline register (APR) module. This method of implementation of the asynchronous circuits doesn't require delay elements and increases the operation speed. Here binary to gray converter is implemented using synchronous, asynchronous and APR circuits. Compared to synchronous, asynchronous, APR realization leads to better performance in terms of area and delay.

KEYWORDS: Asynchronous, Pipeline, clock skew.

I. INTRODUCTION

The vast majority of digital circuits are designed as synchronous circuits. Yet, asynchronous circuits may offer some advantages, including lower power consumption and no clock skew. The asynchronous circuits faces problems such as difficult design process and lack of design tools. Some issues are raised regarding performance advantage and power reduction of asynchronous circuits in comparison with synchronous circuits. Despite the development of asynchronous circuits, some factors make synchronous circuits predominate. Nevertheless, asynchronous circuits are used in research area. The field programmable gate arrays (FPGA) acts as a hardware platform for implementation of asynchronous circuits. There are many methods proposed for implementation of asynchronous circuits. It is important to note that the existing implementation methods in commercial FPGAs require very high designer efforts. A micro pipeline architecture with bundled data has better performance when Compared with mousetrap architecture was proposed in [4].The pipeline architecture has some advantages and disadvantages. It was briefly proposed in [5]. Chong-Fatt Law, Bah-Hwee Gwee and Joseph S. Chang proposed certain rules while designing an asynchronous pipeline circuit in [6]. A asynchronous FPGA architecture for a handshake component was proposed by Yoshiya Komatsu, Masanori Hariyama and Michitaka kameyama in [7]. A methodology to convert synchronous circuits to null conventional logic was discussed by Kyung Ki Kim in [8]. In [9] ultra low power design combined with power switch to reduce leakage current in asynchronous circuits were discussed by Kim and Kyung Ki . Clock behavior of a sequential circuit is modeled and it's timing relation is analyzed in [3]. The proposed design in [2] offers a low power high performance analog to digital conversion in asynchronous circuit. The proposed method in [1] when compared with previous works proved that it offers a simple design method which allows the implementation of asynchronous pipelined circuits in commercial FPGAs. Its advantage is that it does not require any user specific actions.In this work design Binary to Gray Converter combinational logic circuit is considered. The circuit is designed in the synchronous, asynchronous and asynchronous pipeline register realization. The implementation area and delay are measured using real time hardware and compared.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

II. METHODOLOGY

A. ASYNCHRONOUS PIPELINE REGISTER:

The asynchronous pipeline register (APR) module proposed in [1] is essential component in this work. APR latches input data and also generates control signals. The architecture of the APR is shown in fig: 1.

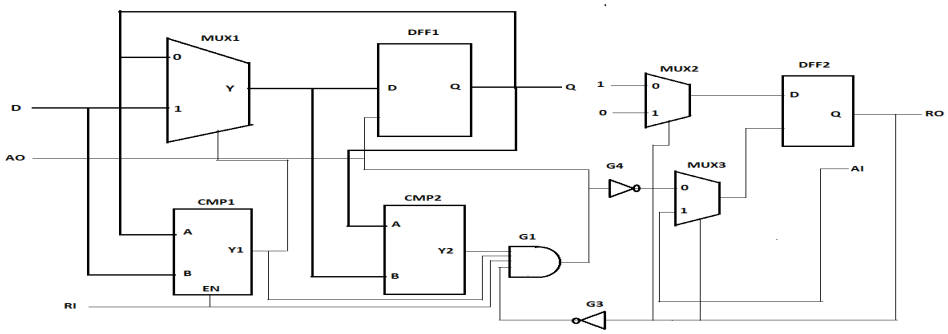


Figure:1 Asynchronous pipeline register

It is developed from previously existing architecture of the asynchronous module for the fuzzy Petri net (FPN) as proposed by J. Kluska, Z. Hajduk in [10] . The method for asynchronous FPN implementation has now been extended and applied for pipelined asynchronous circuit's realization. The bold lines in Fig. 1 represent multi-bit buses. The first part of the circuit is comprised of two comparators CMP1, CMP2. The CMP1 is activated using the enable input EN. The multiplexer MUX1 and comparator CMP2 is responsible for generating the clock signal for the D flip-flop DFF1. The second half of the circuit consists of multiplexers MUX2, MUX3 and flip-flop DFF2. This part deals with asynchronous pipeline control signals. The performance of the module from Fig. 1 is as follows. The emergence of a new data, different than those present in the flip-flop DFF1, causes an activation of the comparator CMP1. The comparator is activated only when RI input is kept. This, in turn, switches the multiplexer MUX1 active and new input data is asserted to the D input of the DFF1 block. Next, the CMP2 comparator compares the data and is activated when the data existing on the input are different. The activation of both comparators, under the condition that the RO which is the output of the DFF2 flip-flop is held low causes the activation of the AND gate G1. The rising edge of the G1 signal latches the input to output in the flip-flop DFF1. As the DFF1 output is updated the comparators gets deactivated and it in turn switches MUX1 back and turns the G1 gate off. The fall in G1 output, through the inverter G2 and multiplexer MUX3, causes an activation in DFF2 flip-flop. As a result, the DFF2 flip-flop switches from low to high. The DFF2 flip-flop stays high until the arrival of the rising-edge signal on the external AI input. It is must be taken into consideration that the APR will operate properly only if the new data delivered to its D input different from the data present on the APR's Q output. Therefore, every time the RI signal is activated, the input data must be different than the data during previous RI activation.

B. PIPELINE CIRCUITS

The APR described in the previous section plays a important role in the implementation of pipelined asynchronous circuit of the proposed method. Pipelined circuit of a (a) synchronous realization (b) common asynchronous realization, (c) proposed APR realization is shown in Fig: 2

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

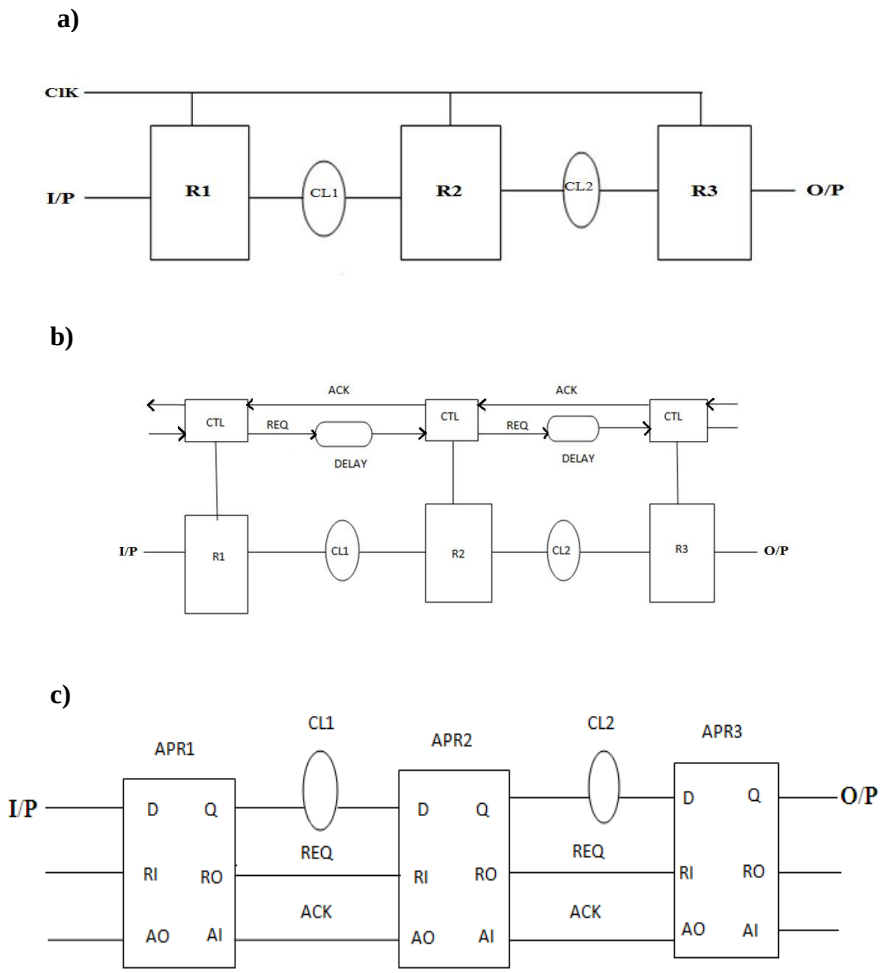


Figure:2 (a)synchronous realization (b) asynchronous realization (c)propsed asynchronous realization

The synchronous pipelined circuit consists of a registers – R1, R2, R3and combinational logic blocks CL1, CL2. The combinational logic blocks are connected in between the two registers as shown in Fig: 2(a). The asynchronous pipelined circuit consists of three control circuit block CTL1, CTL2, CTL3 which generates the clock signal for every register. This block generates asynchronous control signals such as request signal and acknowledgment signal. A very important element in asynchronous circuit's realization is the delay block as shown in Fig: 2(b). The delay value of the delay block must be equal to the propagation delay value of combinational block. Fig. 2(c) represents implementation of pipeline circuits using the proposed asynchronous pipeline register (APR). In this work the CL1,Cl2 combinational logic is replaced by Binary to Gray converter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

C. BINARY TO GRAY CONVERTER PIPELINED CIRCUITS:

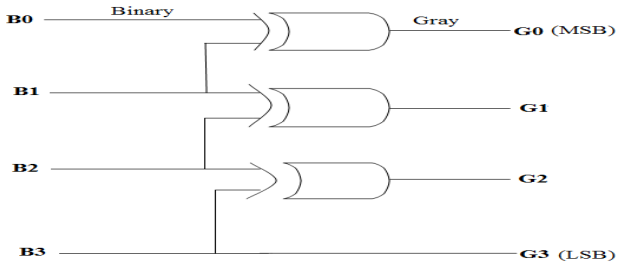
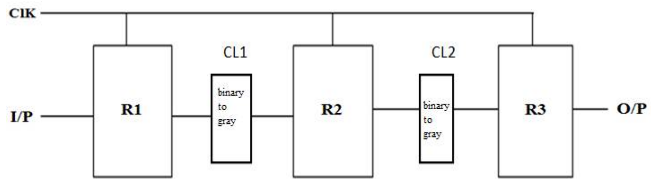


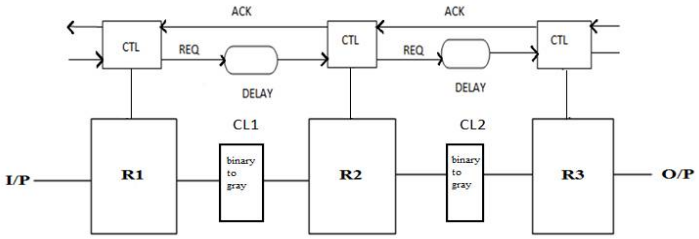
Figure:3Binary to Gray Converter

Fig: 4 shows a simple combinational binary to gray converter circuit is replaced in place of combinational circuits as in fig: 2.

a)



b)



c)

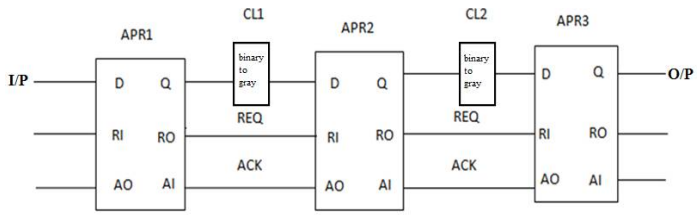


Figure:4 (a) synchronous realization using Binary to gray converter (b) asynchronous realization using Binary to gray converter (c) propsed asynchronous realizationusing Binary to gray converter

The registers mentioned in Fig :4are taken as D flip-flops. In synchronous pipelining realization a global clock is given to all registers. The asynchronous pipelined realization of the binary to gray converter is next considered. In asynchronous pipelined circuits the clock signal is generated using a control circuit.

The registers in synchronous pipeline circuit are replaced by asynchronous pipeline registers (APR). Here AI, RI are activated externally. And AO, RO are output signals produced.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

III. RESULTS AND DISCUSSION

A. Simulation Results:

The simulation results are obtained using Modelsim-Altera6.4a (Quartus II 9.0) starter edition. The waveform of Asynchronous Pipeline Register is shown in Fig:5

Figure:5 Simulation of asynchronous pipeline register

In the above wave form when EN is kept high, AO is made high .Therefore input from d is latched to output Q2 of the flip-flop. In similar way RO must be low initially which becomes high after receiving the output in Q2.
The waveform of synchronous pipeline circuit using Binary to gray is shown in fig: 6.

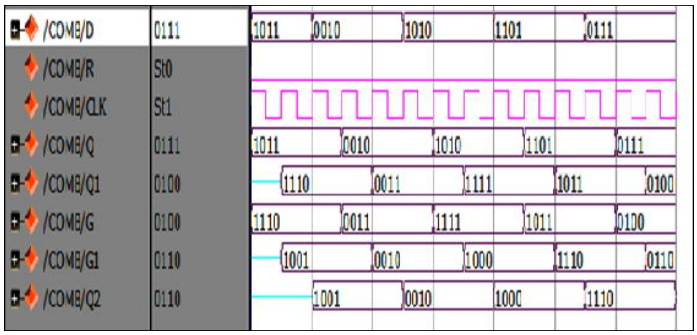


Figure:6 Simulation of synchronous circuits

The input is given to R1 register and the output isconverted and produced in G.Then the output of register R2 is produced in Q1 after some delay .Then it's is converted and produced in G1. The final output i.e output of register R3 is produced after two clock pulses after some delay greater than first delay.
The waveform asynchronous pipeline realization using Binary to gray converter shown in Fig : 7

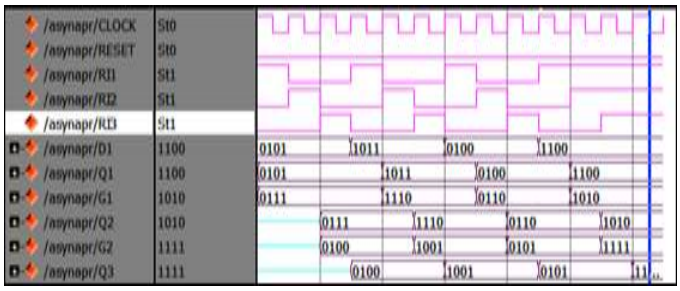


Figure:7 Simulation of typical asynchronous circuits

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

In asynchronous pipeline circuits the clock is generated using control block.A request signal RI1 is given and it in turn produces acknowledgement signal. After,Receiving the acknowledgment signal the control circuits produces the clock to Register R1.Therefore the input D1 latches the data to the Q1 during the first clock signal when RI 1 is high.Then In similar way RI2 is kept high when G1 latches the date to Q2.The output appears in Q2 after two clock pulses and it is converted to gray in G2.The G2 latches the data to Q3 after three clock pulses.Therfore data is produced in G1 at first clock,in G2 after two clock pulses and in G3 after three clock pulses. The waveform of proposed pipeline structure using Binary to gray converter shown in Fig:8

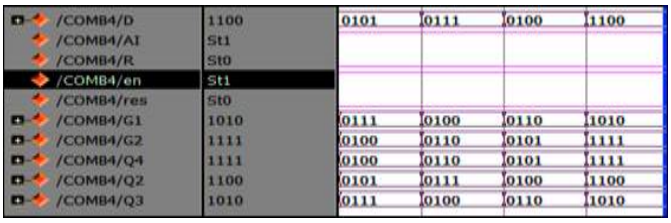


Figure:8 simulation of proposed apr

In proposed pipeline structure the instead of D flip-flop the Asynchronous pipeline Register proposed is used. The APR doesn't need a clock signal, therefore output appears when input is given in D at AI and RI high.

B. Implementation Results:

1) Performance Comparison:

Table:1 Resource Utilization of synchronous, asynchronous and APR realization.

Circuits/ Parameters	Synchronous Realization	Asynchronous Realization	APR Realization
BELs	6	6	4
Flip-Flop	12	15	0
Clock Buffer	1	1	0
I/O Buffer	9(I/O-5 O/P-4)	12(I/P-8,O/P-4)	9(I/P-5,O/P-4)

The performance of the (Synchronous realization, Asynchronous realization, and APR realization) compared using Xilinx implementation (ISE design Suite). The kit used for hardware implementation is SPARTAN 6 which has the operating frequency of 20MHz.The delay and resource utilization comparison is tabulated in Table: 1.From the Table:1, it is observed that when compared to synchronous and asynchronous the proposed realization has less number of BELs(basic element logics), no flip flop and no clock buffer. The Basic Element Logic is used to create LUT (Look Up table) and convert it into physical elements. So APR realization having less area.

From the Table: 2, It is observed that the proposed method consists of only combinational delay. But the synchronous and asynchronous circuits consists of both offset delay before clock and offset delay after clock which constitutes internal delay. So on the whole of considering delay our proposed APR realization consists of less delay when compared with synchronous and asynchronous realization. The proposed APR realization consist of only

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

combinational path delay and doesn't have minimum period ,input arrival time, output arrival time since it is combinational Circuit.

In Table:2 The delay and time period of synchronous, asynchronous and APR realization

Circuits	Synchronous Realization	Asynchronous Realization	APR Realization
Minimum period	1.68ns	-	-
Input arrival time	2.855ns	2.941	-
Output required time	4.118ns	4.118	-
Combinational path Delay	-	-	6.188
Offset Delay before Clock	2.855ns	11.764	-
Offset Delay after Clock	4.188ns	4.188ns	-

2) Schematic Layout:

The RTL schematic realization of synchronous realization is shown in fig:6(a).

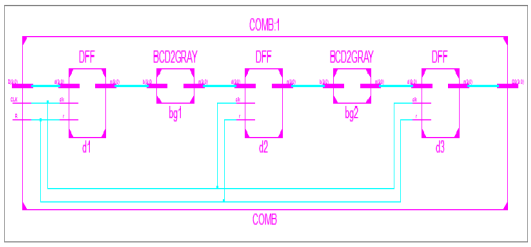


Figure:6(a)RTL schematic of synchronous realization

The RTL schematic of asynchronous realization is shown in fig:6(b).

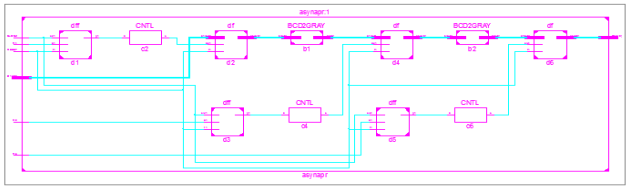


Figure:6(b)RTL schematic of asynchronous realization

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 3, March 2018

The RTL schematic of proposed APR realization is shown in fig:6(c).

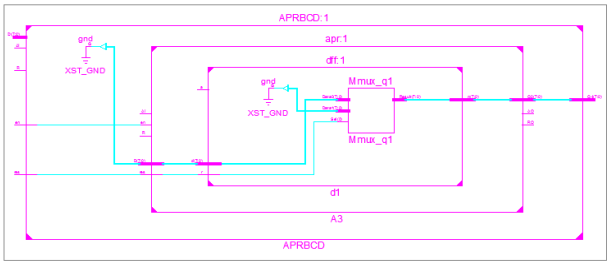


Figure:6(c)RTL schematic of APR realization

IV. CONCLUSION

Thus, the proposed APR method has less delay when compared with synchronous realization and asynchronous realization method. When implemented in Xilinx the number of flip flops and clock buffer is nil in proposed APR method whereas in synchronous realization and asynchronous realization method has number of flip flop and clock buffers respectively. As denoted in table:2 in synchronous realization method has both external delay and internal delay. Therefore the proposed method has less delay, high operation speed, less resource requirements when compared with synchronous and asynchronous circuits. In further work different circuits can be implemented instead of (combinational circuit) Binary to Gray converter.

REFERENCES

1. ZBIGNIEW HAJDUK "simple method of asynchronous circuits implementation in commercial fpgas" in integration the vlsi journal 59 2017
2. vishnu unnikrishnan and mark vesterbacka "time-mode analog-to-digital conversion using standard cells" in ieee transactions on circuits and systems-1: vol. 61, no. 12, december 2014
3. qing wu, massoud pedram, and xunwei wu "clock-gating and its application to low power design of sequential circuits" in ieee transactions on circuits and systems-1: fundamental theory and applications, vol. 47, no. 103, march 2000.
4. duarte l. oliveira, kledermon garcia and roberto d'amore "using fpgas to implement asynchronous pipelines" in ieee 5th latin american symposium on circuits and systems, 2014.
5. steven.m.nowick and montek singh "high- performance asynchronous pipelines" in ieee design and test of computers journal. vol:28 ,issue:5, 2011
6. Chong-Fatt Law, Bah-Hwee Gwee and Joseph S. Chang"Modeling and Synthesis of Asynchronous Pipelines" IEEE Transactions on very large scale integration (VLSI) Systems, VOL: 19,NO:4, April 2011.
7. YoshiyaKomatsu, MasanoriHariyama and Michitaka kameyama "Architecture of an Asynchronous FPGA for handshake-Component Based Design" in IEICE Transaction on Information And System Vol:E96-D, NO:8, August 2013.
8. Kyung Ki Kim "Design and Implementation of Asynchronous 8-bit Microprocessor" in ISSN International Journal of Applied Engineering Research Volume 12, NO: 7, 2017.
9. Kim and Kyung Ki." Asynchronous Circuit Design Combined with Power Switch Structure" in Journal of the Industrial Information Systems Research Volume 21, Issue:1, 2016.
10. J. Kluska, Z. Hajduk, Hardware implementation of a fuzzy Petri net based on VLSI digital circuit, in: Proceedings of Conference of the European Society for Fuzzy Logic and Technology EUSFLAT, 2003, pp. 789–793.
11. D.L. oliveria,K.Garcia,R.d'Amore,using FPGAs to implement asynchronous pipelines ,IEEE Lat.Am.Symp.circuits syst.(2014).
12. P.A.Beerel,R.O.Ozdag,A Designer Guide to Asynchronous VLSI, Cambridge University Press,Cambridge,2010