ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

Serial Transmission Of Video Signal Using Tmds Encoder And Vhdl Implementation

Roshan Kumar Chate, Prof.S.S.Patil

Student, Department of ENTC, Sinhgad Institute of Technology, Lonavala, India

Asst. Professor, Department of ENTC, Sinhgad Institute of Technology, Lonavala, India

ABSTRACT: Computerized visual interface transmitter and recipient in an intuitive media structure contemplate transmitting of first rate video and sound data between the source and the beneficiary over a serial association at high speeds. This endeavor includes a point by point change of cutting edge visual interface (DVI) transmitter and beneficiary in blended media system. These join developing the outline DVI gatherer and transmitter, quick serializer, clock and data recovery circuits and deserializer through the beneficial use of FPGA resources. The undertaking impacts use of TMDS (To change Minimized Differential Signaling) strategy, that incorporates advanced TMDS encoding and deciphering counts using DC balanced transmission, and helps diminishing EMI over the transmission lines.

KEYWORDS: DVI, HDL. Serial Communication, TMDS Encoder.

I. INTRODUCTION

The customary basic video designs exhibit (VGA) standard has been supplanted by the standard advanced visual interface (DVI) with the improvement of the show development. Automated sight and sound interface made use of LVDS development, in the LVDS advancement connect length was confined to short detachment. The proposed work makes use of TMDS development with TMDS encoding and making an interpretation of estimations to vanquish the drawbacks of the LVDS advancement The modernized visual interface (DVI) assurance gives a quick propelled relationship for visual data composes that are demonstrate development self-governingly. The interface is basically connected with at giving a relationship between a PC and its show contraption. The DVI transmitter and beneficiary are related through a singular or twofold TMDS serial association. The TMDS interface is used to send representations data to the screen. A TMDS associate involves a singular clock channel and three data channels (RGB). The progressions minimization is expert by executing pushed encoding figuring on every one of the three channels, change more than 8 bit of video or sound data into a 10 bit advance restricted DC balanced gathering. This move coding figuring enables intense clock recovery and data recovery at the recipient. Along these lines, it achieves more significant skew opposition for transmission over longer connection length. In the TMDS standard the kind of I/O basis, which is CML (Current Mode Logic circuit), is in like manner included subsequently the name "TM" due to the encoder/decoder and "DS" relates to the I/O circuit.

The paper is sorted out as takes after: Introduction of the paper is in Section I. Area II illuminates about the related work. Area III and IV gives the itemizing of the proposed work, its fundamental and result. Area V closes the paper.

II. LITERATURE SURVEY

C.Srinivasan [1] presents a HDMI Transmitter Transaction Level Modeling Design which can be used to easily transform to HDL descriptions for subsequent RTL (Register Transfer Level) Design. Digital Visual Interface[2] Digital Visual Interface, Revision 1.0, Digital Display Working Group.SkandhaDeepsita S. [3]TMDS(transition minimized differential signalling) encoder using QCA.TMDS is a method of transmitting high speed digital signals serially. It is a technology used in DVI(digital visual interface) for establishing communication between graphic board

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

and display. This interface specification provides high speed digital connection for visual data and overcomes the drawback of conventional LVDS technology.

III. PROPOSED SYSTEM

DVI piece chart is as appeared in the fig.1 DVI link and connectors convey four differential match that makes up the TMDS information and the clock channels. These channels are utilized to convey the sound, video and the control information.

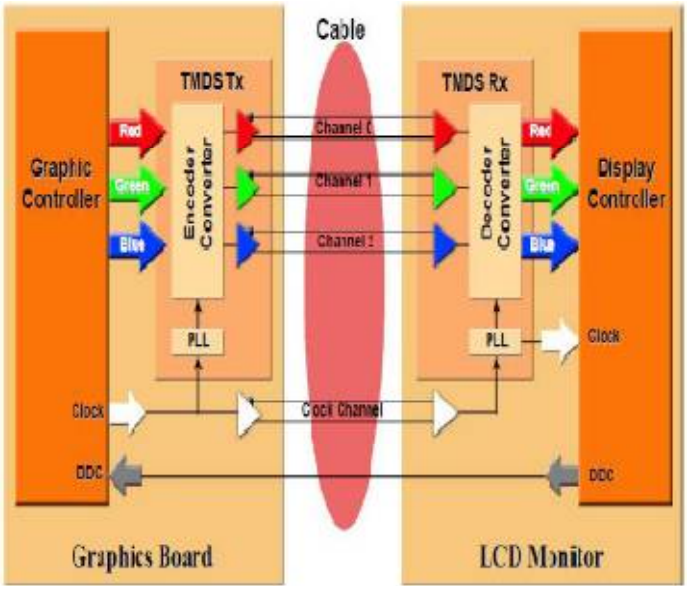

Fig.1. DVI block diagram

The DVI framework comprises of a transmitter and beneficiary, the transmitter encodes and serially transmits a computerized information stream over the wound match of wires to a collector. The sound, video and helper information are conveyed by the three information channel of the TMDS. The video pixel clock is transmitted on the TMDS clock channel and is utilized by the recipient as the recurrence references for the information recuperation on the three TMDS information channels.

Every pixel has three hues, individually, transmitting through three information channels in the meantime, and each shading has 8 bit source word extending from 0-255. The encoded procedure for the dynamic information can be seen as a two phase system. The methodology changes over 8bits for every channel into the 10 bit DC adjusted, progress limited grouping which is then transmitted serially over the combine at a rate of 10bits for each pixel clock period. The TMDS Clock channel conveys a character proportion recurrence reference. The collector/decoder produces bit-rate test clock in light of this reference, which is balanced for each of the information streams, empowering legitimate interpreting.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

IV. PROPOSED ARCHITECTURE

The fig 2 demonstrates the TMDS interface incorporates three TMDS Data channels and a solitary TMDS clock channel.

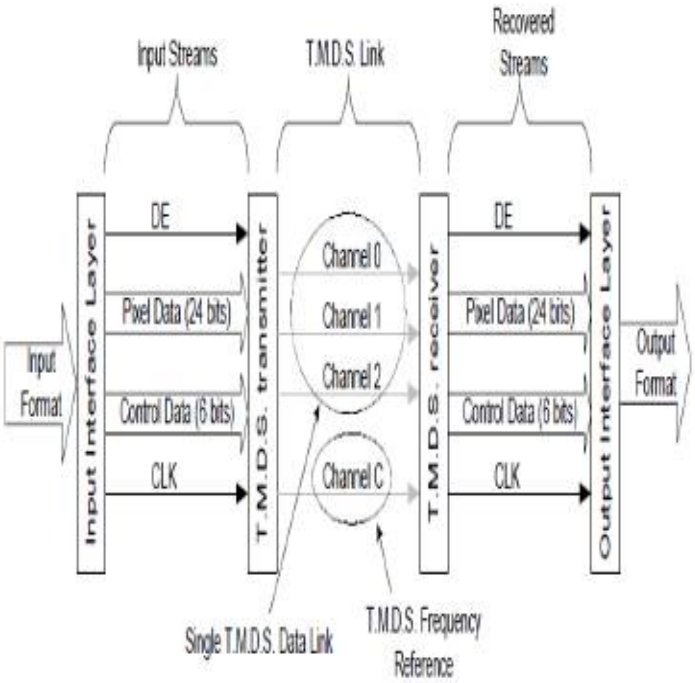

Fig.2. TMDS link architecture

This interface determination takes into account two TMDS joins empowering vast pixel organize computerized show gadgets. Maybe a couple TMDS joins are accessible relying upon the pixel

organization and timings wanted. The two TMDS joins share a similar clock enabling the data transfer capacity to be uniformly partitioned between the two connections. As the capacities of the screen are resolved, the framework will empower one or both TMDS joins.

The info stream contains pixel and control information each of 24 bits. The transmitter encodes either pixel information or control information on any given info clock cycle, contingent upon the condition of the information empower flag (DE). At the TMDS collector, the recuperated pixel information may have progress just when DE is dynamic.

The transmitter contains three indistinguishable encoders, each driving one serial TMDS information channel. The contribution to each encoder is two control signs and eight bits of pixel information.

Contingent upon the territory of DE, the encoder will deliver 0 bit TMDS character from either the two control signals or from the eight bits of pixel information. The yield of every decoder is a consistent stream of serialized TMDS characters.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

V. PROPOSED SYSTEM

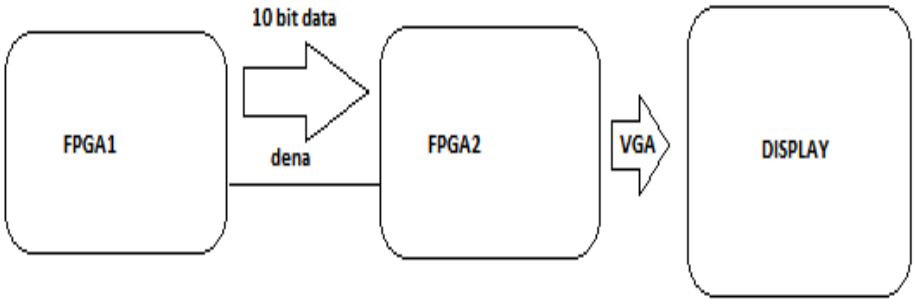

Fig.3. Block diagram of proposed system.

In this we had implement complete display transmitter for power saving. The above block diagram show the communication flow of data. The data is encoded on first FPGA1 and send to FPGA2. The second FPGA decode and send it to display unit. Basically we implement this decoder on display chip.
The dena signal is used as control signal for data and control bit mode.

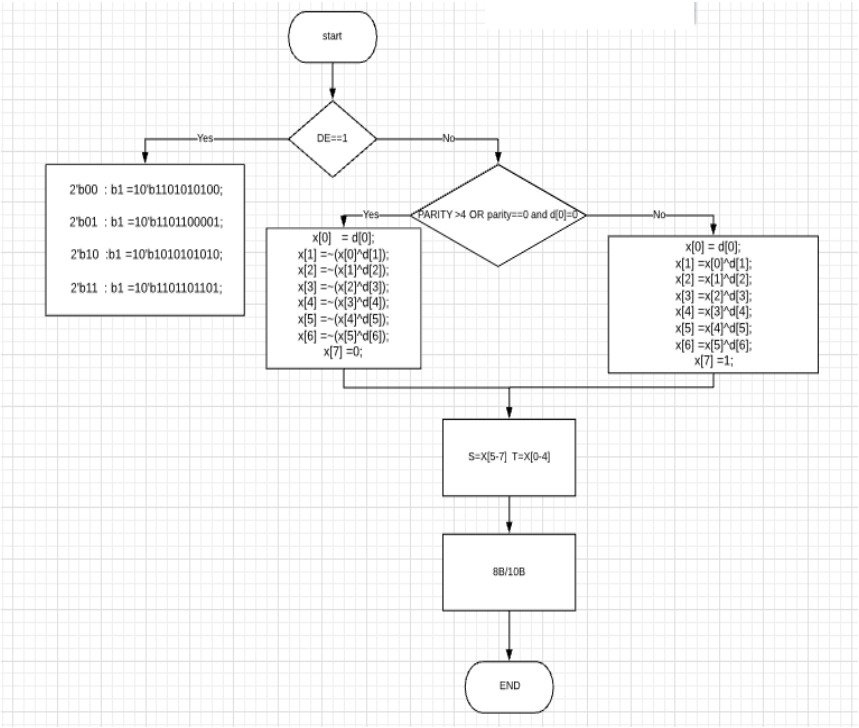

Fig 3: Flow chart of encoding algorithm.

In the give we had encoded the data for dc balancing. In the TMDS encoder the first stage is an XOR/XNOR operator which minimizes the number of transitions and the second stage is a swap the first 3 bit and last 5bit. These group is encoded with 8B/10B then this 10 bit send through transmitter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

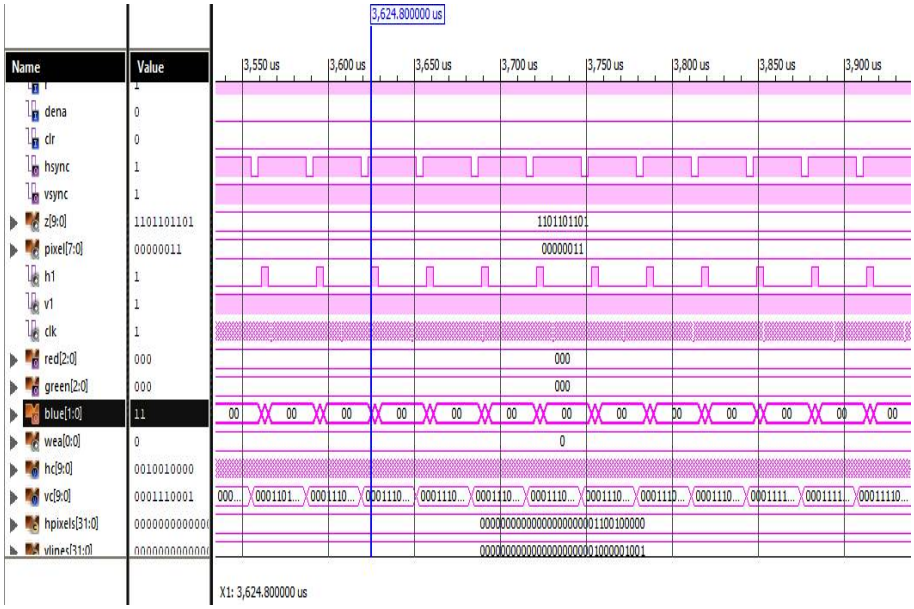

Fig .4.Simulation of proposed system

In above figure we can the pixel is z is encoded data and pixel is decoded 8 bit data. This data is send on VGA using red. Green, blue values for display.

Source Pad	Destination Pad	Delay
dena	blue<0>	12.221
dena	blue<1>	13.596
dena	green<0>	14.097
dena	green<1>	13.554
dena	green<2>	13.853
dena	red<0>	13.410
dena	red<1>	13.049
dena	red<2>	12.878

Fig.5. output latency of proposed system

Figure 5 shown the output latency of system.This show that is fast encoder for transmission.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	87	11440	0%
Number of Slice LUTs	148	5720	2%
Number of fully used LUT-FF pairs	82	153	53%
Number of bonded IOBs	23	102	22%
Number of BUFG/BUFGCTRLs	2	16	12%

Fig.6. Show the area constrain of FPAG by mean of slice LUT and regsistor.

The area cover by proposed system is 2% of XC6SLX9 FPGA. This is merge in existing system with the chip area.

VI. CONCLUSION

The DC-Balanced code sets that fully met the 8b10b benchmark criteria. Which make it power efficient transmitter. This above system is implemented on XC6SLX9 and ISE 14.7. The encoding and decoding doesn't cover more area on chip i.e shown is below figure and also it's also fast (figure 6) for processing. This system can efficiently save 30-40% power as compare to existing system.

REFERENCES

[1] Design and implementation of high definition multimedia interface transmitter and receiver, International Journal of Advanced Technology & Engineering Research (IJATER).
[2] Digital Visual Interface, Revision 1.0, Digital Display Working Group, http://www.ddwg.org.
[3] AlWidmer, Peter Franaszek, ―A DC-Balanced, Parti-tioned-Block, 8B/10B Transmission Code‖ IBM.
[4] Journal of research and development, Volume 27, Number 5, Septem-ber 1983.