ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

Fixed and Floating point-Based High-Speed Chaotic Oscillator Design with Different Numerical Algorithms on FPGA

Murat Tuna[1], İsmail Koyuncu[2], Murat Alçın[3]

Assistant Professor, Dept. of EE, Technical Sciences Vocational High School, Kirklareli University, Kirklareli, Turkey[1]

Assistant Professor, Dept. of EEE, Faculty of Technology, Afyon Kocatepe University, Afyon, Turkey[2]

Assistant Professor, Dept. of ME, Faculty of Technology, Afyon Kocatepe University, Afyon, Turkey[3]

ABSTRACT:In this paper, the design of 3D PC chaotic system has been implemented using Euler, Heun, RK4 and RK5-Butcher numerical algorithms in VHDL with 32 bit IQ-Math fixed point number format (16I-16Q) on FPGA. The chaotic system designed with different numerical algorithms has been tested by being synthesized in Xilinx Virtex–6 (*xc6vlx75t*) FPGA chip. Additionally, the statistics of FPGA chip resource consumption have been investigated. It has been observed that the chaotic oscillators that designed on FPGA in fixed point number format have not only higher operating frequencies but also lower resource consumption ratio with respect to observed results and floating point designs in literature. As a result, various chaos based engineering applications can be performed using chaotic system model that realized in fixed point number format with different algorithms as hardware.

KEYWORDS: Chaos;Chaotic Systems; Numerical Algorithms; FPGA; VHDL

I.INTRODUCTION

Nonlinear chaotic systems and their negative/positive effects on the circuits are one of the scientific areas that have been researched in recent years. Chaos, which has been researched in dynamic systems, is known as the most complicated steady state behavior. When the definition of chaos is investigated, it is seen that it is a nonlinear system having sensitive dependence on initial conditions, deterministic character and aperiodicity in long term [1]–[3]. Although chaotic systems do not have too complex circuit structures, having interesting dynamic properties have quietly increased the interest to chaotic systems recently [4], [5]. During the recent years, important studies related to research and application of chaotic systems have carried out in scientific and industrial areas [6]. Biomedical [7], communication [8], optic electronic and electromagnetic [9], [10], image processing [11], [12], fuzzy logic [13], power electronic [14], optimization [15], robot control and mechatronic [16], [17] can be given as examples for these application areas. Due to the properties of chaotic systems including generating noise like signals, exhibiting aperiodic behaviors and having sensitive dependence on initial conditions, chaotic systems have often been used in the areas of communication engineering like cryptography, secure communication [18], noise generators, encryption and random number generators [19]–[24].

Because of chaotic systems' having a wide application area in information security, these systems can be realized in two different ways as analog and digital. Since digital circuit-based FPGA (Field Programmable Gate Array) chips have features of high speed and capacity, FPGA chips have important potential in applications like cryptology and secure communication that require high performance and high power of processor. FPGA-based chaotic systems and the applications which these systems used draw interest from literature due to the properties of these chips including running in parallel, having very modular structure, low design & test cost and being able to be reprogrammed in the field [25]–[28]. Table 1 presents the mathematical properties and the technical details of FPGA based chaotic oscillator designs in recent years.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

Reference	The mathematical properties of the chaotic system	Algorithm	Number Format	Opr. Freq. (MHz)
[3]	3D Burke-Shaw non-linear autonomous chaotic system, 2 quadratic nonlinearities, 6 terms, 2 parameters	RK5-Butcher	32 Bit IEEE-754 Float. point	373.094
[21]	3D a new chaotic system without equilibrium points, continuous time, 5 quadratic nonlinearities, 10 terms, 6 parameters,	RK4	32 Bit IEEE-754 Float. point	373.094
[26]	3D continuous time, quadratic autonomous, hybrid chaotic systems, four complex chaotic attractors (Lorenz, Lü, Chen and Liu-Chen)	Euler	32 bits (16Q16) Fixed-point	38,86
[27]	3D continuous time, autonomous, 8 terms, 4 quadratic nonlinearities, 1 parameters	Euler Heun RK4	32bit IEEE 754 Float. point	463.688
[28]	3D continuous time autonomous, having golden-section equilibra, 2 quadratic nonlinearities, 8 terms, 2 parameters	Heun	32 bits (16Q16) Fixed-point	406.736
[29]	3D continuous autonomous, 6 terms, 2 quadratic nonlinearities, 1 parameter	Feed Forward ANN,Log-Sig. Tran. function	32bit IEEE 754 Float. point	266.429
[30]	3D continuous-time autonomous chaotic system, 5 quadratic nonlinearities, 10 terms, 2 parameters	Heun RK4	32 Bit IEEE-754 Float. point	390.076
This Article	**3D continuous-time autonomous chaotic system, 5 quadratic nonlinearities, 10 terms, 2 parameters**	**Euler Heun, RK4 RK5-Butcher**	**32 bits (16Q16) Fix.-point**	**464.688**

Table. 1 The technical properties of FPGA based chaotic oscillator designs in recent years.

As summarized in Table 1, the hardware studies related to FPGA-based chaotic systems have generally carried out using floating point number system. Although fixed point number representation presents more effective way to realize in hardware, the chaotic systems designed using fixed point number representation have not commensurately studied, yet. 3D PC chaotic system [30], which presented to literature in 2016 by Tuna et al., has been implemented on FPGA by using four different numerical algorithms in fixed point number format. Tuna has designed PC chaotic system using Heun and RK4 numerical algorithms in IEEE 754-1985 floating point number format on FPGA [30].

In this article, the same chaotic systems (PC chaotic system) has been designed not only using Euler and RK5-Butcher numerical algorithms in floating point number format but also using Euler, Heun, RK4 and RK5-Butcher numerical algorithms in fixed point number format. Thus, it is aimed to design and implement fixed point number based PC chaotic system as hardware in a simple, rapid and more effective way. In the second section, the discretized mathematical models of PC chaotic system have been extracted. In the third section, the discretized designs of PC chaotic system have been presented using four different numerical algorithms in VHDL with 32 bit IQ-Math (16I-16Q) fixed point number format on FPGA. The designed systems have been synthesized and tested in Xilinx Virtex-6 XC6VLX75T-3FF784 FPGA chip. In the last section, the results obtained from the design of PC chaotic system using different algorithms in fixed point number representation and floating point number representation on FPGA have been compared and then evaluated.

II.HARDWARE IMPLEMENTATION OF PC CHAOTIC SYSTEM

A. MATHEMATICAL MODEL OF PC CHAOTIC SYSTEM

The mathematical equation of PC chaotic systems is given in Eq. 1. Here ρ *and* σ are the state variables of PC chaotic systems and the initial conditions of PC chaotic systems are defined as (x_0=-1, y_0=0, z_0=1) [30].

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

$$\begin{cases} \dot{x} = yz - y\rho \\ \dot{y} = yz - y\rho - xz + x\rho \\ \dot{z} = -\rho yx - \sigma z + y^2 + \sigma\rho \end{cases} \quad (1)$$

B. DISCRETE MATHEMATICAL EQUATIONS OF THE PC CHAOTIC SYSTEM

In this part, PC chaotic systems has been modeled using Euler, Heun, RK4 and RK5-Butcher numerical algorithms in VHDL with 32 bit IQ-Math fixed point number standart. The performance and chip statistics of the results obtained from the implementation on FPGA have been investigated and the precision analysis of the numerical algorithms has been performed. Since the discretized mathematical equations of Heun and RK4 numerical algorithms have been previously reported in the study [30], here the discretized mathematical equations of Euler and RK5-Butcher numerical algorithms have been presented. The initial conditions of *x(k), y(k)* and *z(k)* in discretized models of algorithms have been defined as *x(k)=-1.0, y(k)=0,0* and *z(k)=1.0* for PC chaotic systems. The discretized mathematical model of PC chaotic systems using Euler algorithm is given in Eq. 2.

$$\begin{aligned} x(k+1) &= x(k) + \Delta h\left(y(k).z(k) - \rho.y(k)\right) \\ y(k+1) &= y(k) + \Delta h\left(y(k).z(k) - \rho.y(k) - x(k).z(k) - \rho.x(k)\right) \\ z(k+1) &= z(k) + \Delta h\left(-y(k).\rho.x(k) + y^2(k) - \sigma.z(k) + \sigma.\rho\right) \end{aligned} \quad (2)$$

The discretized mathematical model of PC chaotic systems using RK5-Butcher algorithm is given in Eq. 3. Although RK5-Butcher algorithm and RK4 algorithm have similar structures, RK5-Butcher algorithm generates more sensitive solutions than RK4 due to RK5-Butcher's having the terms of 5th and 6th degrees.

III. THE IMPLEMENTATION OF PC CHAOTIC SYSTEMS ON FPGA

In this part, the PC chaotic systems has been modeled using Euler, Heun, RK4 and RK5-Butcher numerical algorithms in 32 bit IQ-Math fixed point number standart on FPGA and coded in VHDL. The units including subtractor, multiplier and adder which are suitable for fixed point number standard and are utilized for the designs, have been generated with IP-CORE Generator developed by Xilinx ISE Design Tools.The top level block diagrams of Euler, Heun, RK4 and RK5-Butcher-based units are the same for all algorithms as shown in Fig. 1. *Start* and *Clk* signals are one bit signals that are ready at inputs of the unit. These signals are utilized for scheduling all units and synchronizing all units and their connections. *Δh* is responsible for determining the precision of the algorithm and it represents the step size parameter. This signal is applied from the outer side so it presents modularity for the implementation. The initial values have responsibility for the system startup and they have been embedded into the implementation for reducing the chip resource usage. However, when it is essential to utilize these signals, it is convenient to implement the system to arrange the initial values describing 3 signals that have 32-bit by changing slightly the design. In the designed Euler, Heun, RK4 and RK5-Butcher-based chaotic oscillators, there exist three 32-bit output signals namely, *X_out, Y_out* and *Z_out* and all of them compatible with fixed point number representation and one bit *xyz_ready* signal to demonstrate if the outputs are ready.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

$$x(k+1) = x(k) + \frac{1}{90}\Delta h\left[7\kappa_1(k) + 32\kappa_3(k) + 12\kappa_4(k) + 32\kappa_5(k) + 7\kappa_6(k)\right]$$

$$y(k+1) = y(k) + \frac{1}{90}\Delta h\left[7\lambda_1(k) + 32\lambda_3(k) + 12\lambda_4(k) + 32\lambda_5(k) + 7\lambda_6(k)\right]$$

$$z(k+1) = z(k) + \frac{1}{90}\Delta h\left[7\zeta_1(k) + 32\zeta_3(k) + 12\zeta_4(k) + 32\zeta_5(k) + 7\zeta_6(k)\right]$$

$$\kappa_1 = f(x(k), y(k), z(k))$$

$$\lambda_1 = g(x(k), y(k), z(k))$$

$$\xi_1 = \delta(x(k), y(k), z(k))$$

$$\kappa_2 = f(x(k) + \frac{1}{4}\Delta h\kappa_1, y(k) + \frac{1}{4}\Delta h\lambda_1, z(k) + \frac{1}{4}\Delta h\xi_1)$$

$$\lambda_2 = g(x(k) + \frac{1}{4}\Delta h\kappa_1, y(k) + \frac{1}{4}\Delta h\lambda_1, z(k) + \frac{1}{4}\Delta h\xi_1)$$

$$\xi_2 = \delta(x(k) + \frac{1}{4}\Delta h\kappa_1, y(k) + \frac{1}{4}\Delta h\lambda_1, z(k) + \frac{1}{4}\Delta h\xi_1)$$

$$\kappa_3 = f(x(k) + \frac{1}{8}(\Delta h(\kappa_1 + \kappa_{2)}, y(k) + \frac{1}{8}(\Delta h(\lambda_1 + \lambda_{2)}, z(k) + \frac{1}{8}(\Delta h(\xi_1 + \xi_{2)})$$

$$\lambda_3 = g(x(k) + \frac{1}{8}(\Delta h(\kappa_1 + \kappa_{2)}, y(k) + \frac{1}{8}(\Delta h(\lambda_1 + \lambda_{2)}, z(k) + \frac{1}{8}(\Delta h(\xi_1 + \xi_{2)})$$

$$\xi_3 = \delta(x(k) + \frac{1}{8}(\Delta h(\kappa_1 + \kappa_{2)}, y(k) + \frac{1}{8}(\Delta h(\lambda_1 + \lambda_{2)}, z(k) + \frac{1}{8}(\Delta h(\xi_1 + \xi_{2)})$$

$$\kappa_4 = f(x(k) - \frac{1}{2}\Delta h\kappa_2 + \Delta h\kappa_3, y(k) - \frac{1}{2}\Delta h\lambda_2 + \Delta h\lambda_3, z(k) - \frac{1}{2}\Delta h\xi_2 + \Delta h\xi_3) \quad (3)$$

$$\lambda_4 = g(x(k) - \frac{1}{2}\Delta h\kappa_2 + \Delta h\kappa_3, y(k) - \frac{1}{2}\Delta h\lambda_2 + \Delta h\lambda_3, z(k) - \frac{1}{2}\Delta h\xi_2 + \Delta h\xi_3)$$

$$\xi_4 = \delta(x(k) - \frac{1}{2}\Delta h\kappa_2 + \Delta h\kappa_3, y(k) - \frac{1}{2}\Delta h\lambda_2 + \Delta h\lambda_3, z(k) - \frac{1}{2}\Delta h\xi_2 + \Delta h\xi_3)$$

$$\kappa_5 = f(x(k) + \frac{3}{16}\Delta h\kappa_1 + \frac{9}{16}\Delta h\kappa_4, y(k) + \frac{3}{16}\Delta h\lambda_1 + \frac{9}{16}\Delta h\lambda_4, z(k) + \frac{3}{16}\Delta h\xi_1 + \frac{9}{16}\Delta h\xi_4)$$

$$\lambda_5 = g(x(k) + \frac{3}{16}\Delta h\kappa_1 + \frac{9}{16}\Delta h\kappa_4, y(k) + \frac{3}{16}\Delta h\lambda_1 + \frac{9}{16}\Delta h\lambda_4, z(k) + \frac{3}{16}\Delta h\xi_1 + \frac{9}{16}\Delta h\xi_4)$$

$$\xi_5 = \delta(x(k) + \frac{3}{16}\Delta h\kappa_1 + \frac{9}{16}\Delta h\kappa_4, y(k) + \frac{3}{16}\Delta h\lambda_1 + \frac{9}{16}\Delta h\lambda_4, z(k) + \frac{3}{16}\Delta h\xi_1 + \frac{9}{16}\Delta h\xi_4)$$

$$\kappa 6 = f(x(k) - \frac{3}{7}\Delta h\kappa_1 + \frac{2}{7}\Delta h\kappa_2 + \frac{12}{7}\Delta h\kappa_3 - \frac{12}{7}\Delta h\kappa_4 + \frac{8}{7}\Delta h\kappa_5, y(k) + -\frac{3}{7}\Delta h\lambda_1 + \frac{2}{7}\Delta h\lambda_2 +$$
$$\frac{12}{7}\Delta h\lambda_3 - \frac{12}{7}\Delta h\lambda_4 + \frac{8}{7}\Delta h\lambda_5, z(k) - \frac{3}{7}\Delta h\xi_1 + \frac{2}{7}\Delta h\xi_2 + \frac{12}{7}\Delta h\xi_3 - \frac{12}{7}\Delta h\xi_4 + \frac{8}{7}\Delta h\xi_5)$$

$$\lambda 6 = g(x(k) - \frac{3}{7}\Delta h\kappa_1 + \frac{2}{7}\Delta h\kappa_2 + \frac{12}{7}\Delta h\kappa_3 - \frac{12}{7}\Delta h\kappa_4 + \frac{8}{7}\Delta h\kappa_5, y(k) + -\frac{3}{7}\Delta h\lambda_1 + \frac{2}{7}\Delta h\lambda_2 +$$
$$\frac{12}{7}\Delta h\lambda_3 - \frac{12}{7}\Delta h\lambda_4 + \frac{8}{7}\Delta h\lambda_5, z(k) - \frac{3}{7}\Delta h\xi_1 + \frac{2}{7}\Delta h\xi_2 + \frac{12}{7}\Delta h\xi_3 - \frac{12}{7}\Delta h\xi_4 + \frac{8}{7}\Delta h\xi_5)$$

$$\xi 6 = \delta(x(k) - \frac{3}{7}\Delta h\kappa_1 + \frac{2}{7}\Delta h\kappa_2 + \frac{12}{7}\Delta h\kappa_3 - \frac{12}{7}\Delta h\kappa_4 + \frac{8}{7}\Delta h\kappa_5, y(k) + -\frac{3}{7}\Delta h\lambda_1 + \frac{2}{7}\Delta h\lambda_2 +$$
$$\frac{12}{7}\Delta h\lambda_3 - \frac{12}{7}\Delta h\lambda_4 + \frac{8}{7}\Delta h\lambda_5, z(k) - \frac{3}{7}\Delta h\xi_1 + \frac{2}{7}\Delta h\xi_2 + \frac{12}{7}\Delta h\xi_3 - \frac{12}{7}\Delta h\xi_4 + \frac{8}{7}\Delta h\xi_5)$$

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

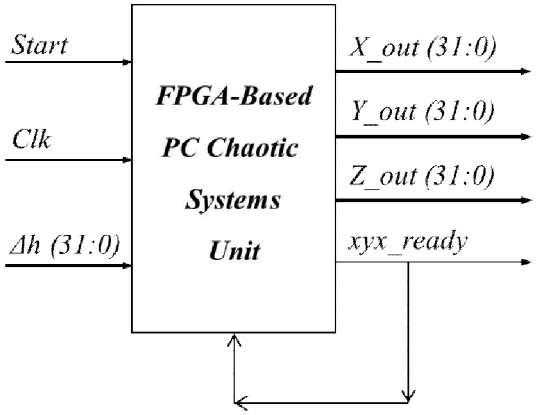

Fig. 1 The Top level block diagram of FPGA-based PC chaotic systems unit.

The third top level block diagram of Euler-Based PC Chaotic Systems unit is illustrated in Fig. 2. The units namely *Mux*, *Multiplier*, *Adder*, *Filter* and *f* are utilized in the construction of the oscillator unit. The unit runs in pipelined manner and Euler-based PC chaotic oscillator unit generates the first results after 28 clock pulse. The signals produced by chaotic oscillator unit namely, *x(k+1)*, *y(k+1)* and *z(k+1)* constitute not only the outputs of the system but also new initial conditions for system by being sent to *MUX* unit for calculating the next algorithm.

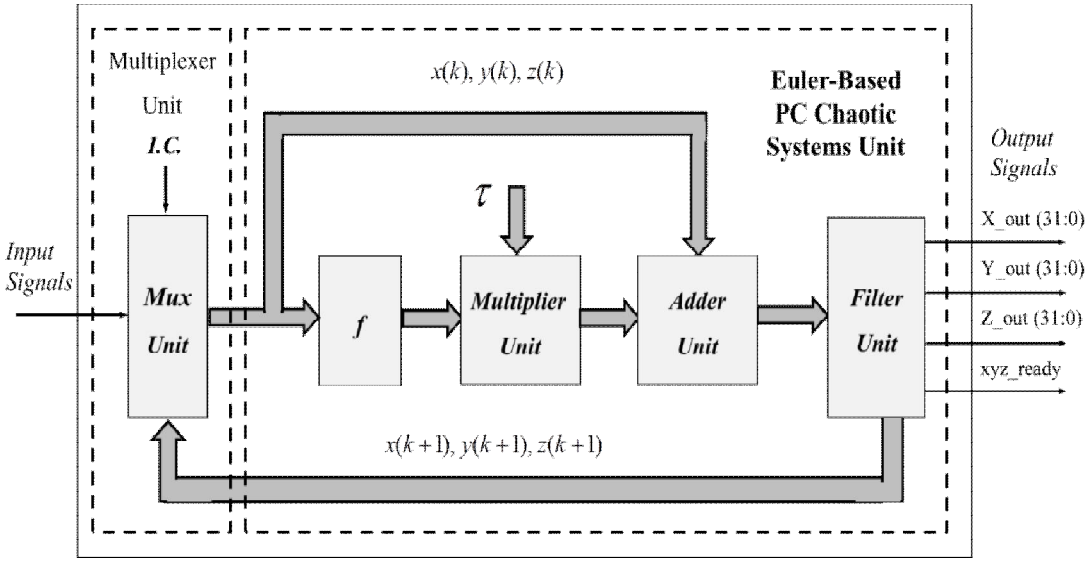

Fig. 2 The third top level block diagram of Euler-based PC chaotic systems unit.

The third top level block diagram of RK5-Based PC chaotic Systems unit is shown in Fig. 3. There are 9 units (k_1, k_2, k_3, k_4, k_5, k_6*ys* and *Filter*) in the construction of the chaotic oscillator unit. Differently from the RK4-Based design, thispart includes k_5 and k_6 units to compute 5th and 6th degree terms. Apart from that, it runs very analogue to RK4-based new chaotic oscillator unit.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

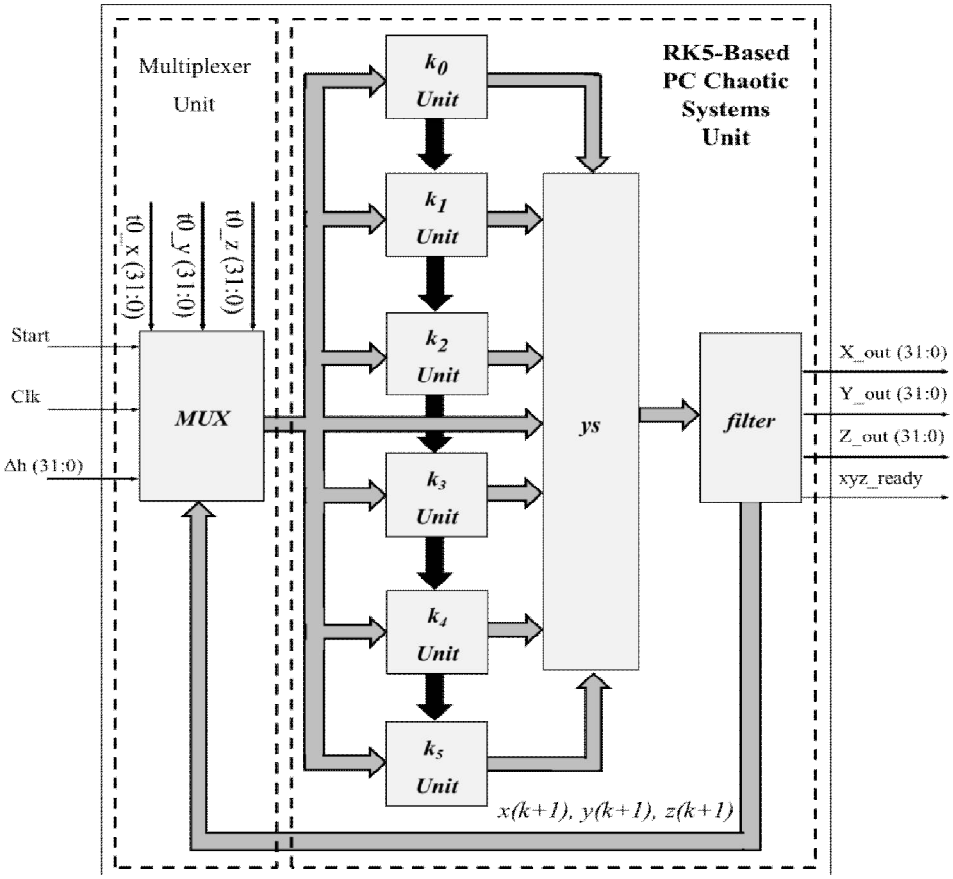

Fig. 3 The third top level block diagram of RK5-Butcher-based PC chaotic systems unit.

IV. TEST RESULTS OF FPGA-BASED PC CHAOTIC SYSTEM

Euler, Heun, RK4 and RK5-Butcher-based oscillator units are synthesized for the *Xilinx Virtex–6* chip. The detail of FPGA resource usage and the units' parameters about clock frequencies have been examined. The data operation time of units contemplated on 4 distinct architectures have been attained by Xilinx ISE Design Tools 14.2. The "*x*", "*y*" and "*z*" signals of the chaotic oscillator correspond to *X_out*, *Y_out* and *Z_out* signals of chaotic oscillator unit by implementing on FPGA using ISE Design Tools software. The values related to time series of *X_out*, *Y_out* and *Z_out* signals are represented by 32 bit fixed point number format. Xilinx ISE simulator results of the Euler, Heun, RK4 and RK5-Butcher-based PC chaotic system units that designed on FPGA in fixed point number format are presented in Fig. 4-7.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

Fig. 4. Xilinx ISE simulator results of the Euler-based PC chaotic oscillator unit.

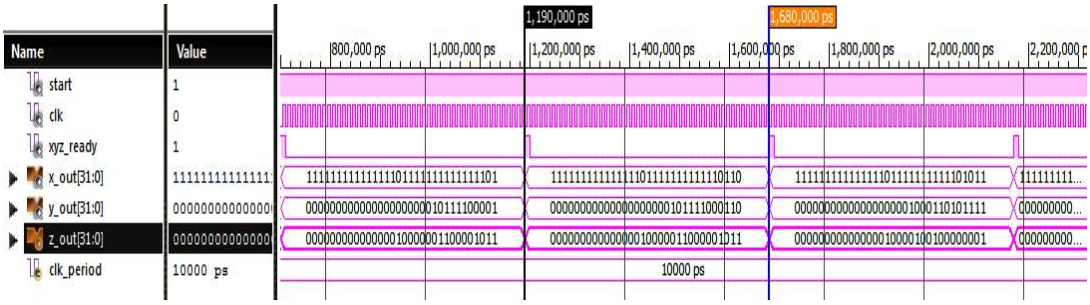

Fig. 5 Xilinx ISE simulator results of the Heun-based PC chaotic oscillator unit.

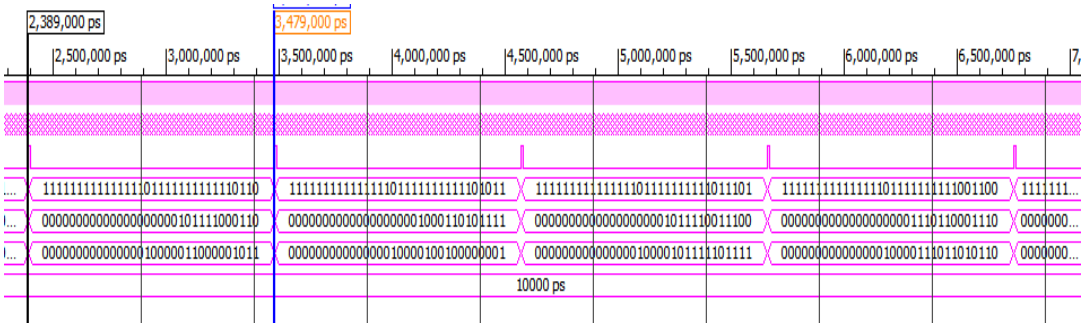

Fig. 6 Xilinx ISE simulator results of the RK4-based PC chaotic oscillator unit.

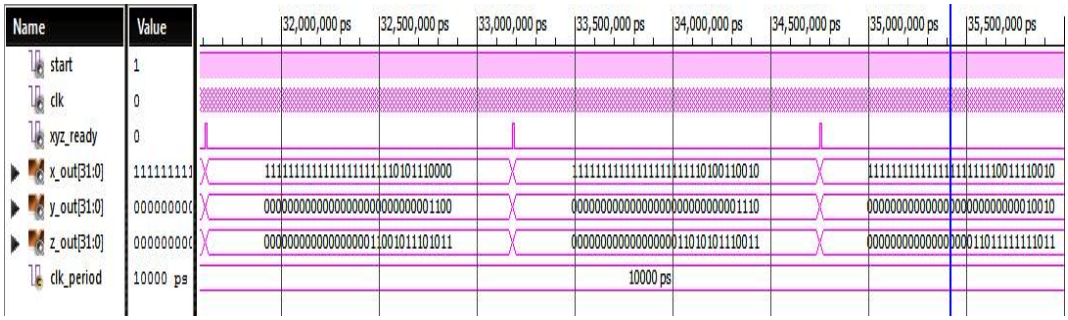

Fig. 7 Xilinx ISE simulator results of the RK5-Butcher-based PC chaotic oscillator unit.

After the Place&Route procedure that has been carried out at the end of synthesizing the Euler, Heun, RK4 and RK5-Butcher-based PC chaotic oscillators in 32 bit IQ-Math fixed point number format, Xilinx Virtex-6 xc6vlx75T-3ff784

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

chip statistics are achieved and illustrated in Table 2. As observed from Table 2, the maximum usable frequencies of the chaotic oscillators have been measured as 464.688 MHz.

Device Utilization Summary (estimated values)	Euler-Based PC chaotic system	Heun-Based PC chaotic system	RK4-Based PC chaotic system	RK5- Butcher PC chaotic system
	Used / Utilization (%)			
Number of Slice Registers	1471 / 1	2998 / 3	6439 / 6	12444 / 13
Number of Occupied slices	2475 / 24	3750 / 34	4248 / 39	5247 / 42
Number of Slice LUTs	1249 / 2	2687 / 5	5756 / 12	11144 / 23
Number of fully used LUT-FF pairs	999 / 58	2117 / 59	4548 / 59	8769 / 59
Number of bonded IOBs	99 / 27	99 / 27	99 / 27	99 /27
Number of BUFG/BUFGCTRLs	1 / 3	1 / 3	1 / 3	1 / 3
Number of DSP48E1s	36 / 12	72 / 25	168 / 58	315 / 120 (*)
Max. Clock Frequency (MHz)	464,688	464,688	464,688	436,143
(*) More than 100% of Device resources are used				

Table. 2 The chip statistics of PC chaotic system that designed with different numerical algorithms in 32 bit IQ-Math fixed point number format (16I-16Q) onFPGA.

Table 3 shows the chip statistics attained from Euler, Heun, RK4 and RK5-Butcher-based implementation that designed with different numerical algorithms in 32 bit IQ-Math floating point number format onFPGA. The purpose is to make the comparison of two different number system on hardware with respect to performances and chip statistics. As seen in Table 2 and Table 3, the PC chaotic system designed by fixed point number format has not only lower FPGA resource consumption but also greater operating frequency than floating point number format.

Device Utilization Summary (estimated values)	Euler-Based PC chaotic system	Heun-Based PC chaotic system	RK4-Based PC chaotic system	RK5- Butcher PC chaotic system
	Used / Utilization (%)			
Number of Slice Registers	11275 / 15	21499 / 23	45805 / 49	53475 / 58
Number of Occupied slices	4752 / 46	6283 / 53	7585 / 65	8785 / 71
Number of Slice LUTs	18475 / 38	20333 / 43	47273 / 101 (*)	57485 / 127 (*)
Number of fully used LUT-FF pairs	14895 / 62	16925 / 67	36939 / 65	41751 / 72
Number of bonded IOBs	131 / 36	131 / 36	131 / 36	131 / 36
Number of BUFG/BUFGCTRLs	1 / 3	1 / 3	1 / 3	1 / 3
Max. Clock Frequency (MHz)	**390,076**	**390,076**	**390,076**	**359,475**
(*) More than 100% of Device resources are used				

Table. 3 The chip statistics of PC chaotic system designed with different numerical algorithms in 32 bit IEEE 754-1985 floating point number format on FPGA.

V. CONCLUSION

In this study, the design of 3D PC chaotic system has been realized using 4 different numerical algorithms in VHDL with 32 bit IQ-Math fixed point number format (16I-16Q) on FPGA. The implemented 4 different chaotic oscillator have been synthesized and tested. The maximum operating frequency of the designed chaotic oscillators has been obtained as 464,688 MHz. Besides, the chip utilization statistics of PC chaotic system designed in fixed point number format and the chip utilization statistics of the same system designed in floating point number format have been compared. It is observed that the PC chaotic system designed in fixed point number format on FPGA has better results than the PC chaotic system designed in floating point number format on FPGA. Embedded chaos based engineering applications including cryptography, secure communication and random number generators can be performed with even low cost and high speed using PC chaotic oscillator that designed in fixed point number format on FPGA. In future, various applications like chaos-based synchronization, data encryption and random number generation can be realized using the discrete time PC chaotic oscillator in IQ-Math fixed point number format on FPGA.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 7, July 2018

REFERENCES

[1] V. Sundarapandian and I. Pehlivan, "Analysis, control, synchronization, and circuit design of a novel chaotic system," Math. Comput. Model., vol. 55, no. 7–8, pp. 1904–1915, Apr. 2012.
[2] M. Tuna and C. B. Fidan, "A Study on the importance of chaotic oscillators based on FPGA for true random number generating (TRNG) and chaotic systems," J. Fac. Eng. Archit. Gazi Univ., vol. 33, no. 2, pp. 469–486, 2018.
[3] I. Koyuncu, A. T. Ozcerit, and I. Pehlivan, "An analog circuit design and FPGA-based implementation of the Burke-Shaw chaotic system," Optoelectron. Adv. Materıals-Rapıd Communıcatıons, vol. 7, no. 9, pp. 635–638, Sep. 2013.
[4] İ. Pehlivan and Y. Uyaroğlu, "A new 3D chaotic system with golden proportion equilibria: Analysis and electronic circuit realization," Comput. Electr. Eng., vol. 38, no. 6, pp. 1777–1784, Nov. 2012.
[5] A. Akgul, S. Hussain, and I. Pehlivan, "A new three-dimensional chaotic system, its dynamical analysis and electronic circuit applications," Opt. - Int. J. Light Electron Opt., vol. 127, no. 18, pp. 7062–7071, Sep. 2016.
[6] İ. PEHLİVAN and Z. WEI, "Analysis, nonlinear control, and chaos generator circuit of another strange chaotic system," Turkısh J. Electrıcal Engıneerıng Comput. Scıences, vol. 20, no. Sup.2, pp. 1229–1239, Dec. 2012.
[7] A. Xiong, X. Zhao, J. Han, and G. Liu, "Application of the Chaos Theory in the Analysis of EMG on Patients with Facial Paralysis," Robot Intell. Tech. App, pp. 805–819, 2014.
[8] I. Koyuncu, M. Alcin, and I. Pehlivan, "Electronic circuit realization and synchronization application of Sprott 94 S chaotic system for secure communication systems," in 2013 21st Signal Processing and Communications Applications Conference (SIU), 2013, pp. 1–4.
[9] Y. Ji et al., "Microwave-Photonic Sensor for Remote Water-Level Monitoring Based on Chaotic Laser," Int. J. Bifurc. Chaos, vol. 24, no. 3, p. 1450032, Mar. 2014.
[10] J. Zhang et al., "A robust random number generator based on differential comparison of chaotic laser signals," Opt. Express, vol. 20, no. 7, p. 7496, Mar. 2012.
[11] Ü. Çavuşoğlu, S. Kaçar, I. Pehlivan, and A. Zengin, "Secure image encryption algorithm design using a novel chaos based S-Box," Chaos, Solitons & Fractals, vol. 95, pp. 92–101, Feb. 2017.
[12] S. Janakiraman, K. Thenmozhi, J. B. B. Rayappan, and R. Amirtharajan, "Lightweight chaotic image encryption algorithm for real-time embedded system: Implementation and analysis on 32-bit microcontroller," Microprocess. Microsyst., vol. 56, pp. 1–12, Feb. 2018.
[13] S.-H. Yu, H. S. Kang, Y.-T. Kim, C.-H. Hyun, and M. Park, "Fuzzy adaptive modular design of uncertain chaotic Duffing oscillators," Int. J. Control. Autom. Syst., vol. 12, no. 1, pp. 188–194, Feb. 2014.
[14] S. Ashita, G. Uma, and P. Deivasundari, "Chaotic dynamics of a zero average dynamics controlled DC–DC Ćuk converter," IET Power Electron., vol. 7, no. 2, pp. 289–298, Feb. 2014.
[15] A. Anees, A. M. Siddiqui, and F. Ahmed, "Chaotic substitution for highly autocorrelated data in encryption algorithm," Commun. Nonlinear Sci. Numer. Simul., vol. 19, no. 9, pp. 3106–3118, 2014.
[16] D. Q. Wei, L. Wan, X. S. Luo, S. Y. Zeng, and B. Zhang, "Global exponential stabilization for chaotic brushless DC motors with a single input," Nonlinear Dyn., vol. 77, no. 1–2, pp. 209–212, Jul. 2014.
[17] J. Pomares, I. Perea, and F. Torres, "Dynamic Visual Servoing With Chaos Control for Redundant Robots," IEEE/ASME Trans. Mechatronics, vol. 19, no. 2, pp. 423–431, Apr. 2014.
[18] S. Çiçek, Y. Uyaroğlu, and İ. Pehlivan, "Simulation and Circuit Implementation of Sprott Case H Chaotic System and its Synchronization Application for Secure Communication Systems," J. Circuits, Syst. Comput., vol. 22, no. 4, p. 1350022, Apr. 2013.
[19] G. Jakimoski and L. Kocarev, "Chaos and cryptography: Block encryption ciphers based on chaotic maps," IEEE Trans. Circuits Syst. I Fundam. Theory Appl., vol. 48, no. 2, pp. 163–169, 2001.
[20] M. Tuna, I. Koyuncu, C. B. Fidan, and I. Pehlivan, "Real time implementation of a novel chaotic generator on FPGA," in 2015 23nd Signal Processing and Communications Applications Conference (SIU), 2015, pp. 698–701.
[21] A. Akgul, H. Calgan, I. Koyuncu, I. Pehlivan, and A. Istanbullu, "Chaos-based engineering applications with a 3D chaotic system without equilibrium points," Nonlinear Dyn., vol. 84, no. 2, pp. 481–495, Nov. 2015.
[22] Ü. Çavuşoğlu, A. Akgül, S. Kaçar, İ. Pehlivan, and A. Zengin, "A novel chaos-based encryption algorithm over TCP data packet for secure communication," Secur. Commun. Networks, vol. 9, no. 11, pp. 1285–1296, Jul. 2016.
[23] E. Avaroğlu, "Pseudorandom number generator based on Arnold cat map and statistical analysis," Turkısh J. Electrıcal Engıneerıng Comput. Scıences, vol. 25, no. 1, pp. 633–643, 2017.
[24] Ü. Çavuşoğlu, A. Zengin, I. Pehlivan, and S. Kaçar, "A novel approach for strong S-Box generation algorithm design based on chaotic scaled Zhongtang system," Nonlinear Dyn., vol. 87, no. 2, pp. 1081–1094, Jan. 2017.
[25] K. Eguchi, T. INOUE, and A. TSUNEDA, "FPGA Implementation of a Digital Chaos Circuit Realizing a 3-Dimensional Chaos Model," IEICE Trans. Fundam. Electron. Commun. Comput. Sci., vol. E81–A, no. 6, pp. 1176–1178, Jun. 1998.
[26] M. S. Azzaz, C. Tanougast, S. Sadoudi, R. Fellah, and A. Dandache, "A new auto-switched chaotic system and its FPGA implementation," Commun. Nonlinear Sci. Numer. Simul., vol. 18, no. 7, pp. 1792–1804, Jul. 2013.
[27] I. Koyuncu, A. T. Ozcerit, and I. Pehlivan, "Implementation of FPGA-based real time novel chaotic oscillator," Nonlinear Dyn., vol. 77, no. 1–2, pp. 49–59, Feb. 2014.
[28] M. Tuna, C. B. Fidan, I. Koyuncu, and I. Pehlivan, "Real time hardware implementation of the 3D chaotic oscillator which having golden-section equilibra," in 2016 24th Signal Processing and Communication Application Conference (SIU), 2016, pp. 1309–1312.
[29] M. Alçın, İ. Pehlivan, and İ. Koyuncu, "Hardware design and implementation of a novel ANN-based chaotic generator in FPGA," Opt. - Int. J. Light Electron Opt., vol. 127, no. 13, pp. 5500–5505, Jul. 2016.
[30] M. Tuna and C. B. Fidan, "Electronic circuit design, implementation and FPGA-based realization of a new 3D chaotic system with single equilibrium point," Opt. - Int. J. Light Electron Opt., vol. 127, no. 24, pp. 11786–11799, 2016.