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TCAD Device Design and Analysis of 20nm DGTFET

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ABSTRACT: Power consumption is one of the most important constraint in the design of CMOS higher technology nodes. Various methods to decrease the power ranging from the architecture level to the semiconductor device level are prominent topics in research. From device level perspective it is seen that the operating voltage can be reduced without sacrificing the switching properties with the use of devices with low subthreshold swings. Tunnel Field Effect transistors (TFETs) are promising class of the steep slope devices[1]. The switching mechanism in TFET is quantum tunneling rather than thermionic emission of electrons as in traditional CMOS. In this work, a Dual Gate TFET (DGTFET) of gate length(Lg) 20nm is modeled in Sentaurus TCAD tool. The effect of variation of source doping level, drain doping level, poly doping level, high-k oxide material and variation of the body thickness is analyzed. The 20nm DGTFET shows the substhreshold swing of 48.485 mV/dec which is much lesser than traditional MOSFET.

KEYWORDS: DGTFET, TCAD, Tunnel Field Effect Transistor, steep slope, quantum tunneling, SDE

I.INTRODUCTION

According to the Moore's law, the number of transistors on an unit area of IC doubles for every two years. According to the International Technology Roadmap for semiconductors (ITRS), the scaling of the CMOS technology can sustain till 2019[2]. Electron migration, power dissipation, and leakage current are some of the issues faced by CMOS today in higher technology nodes. Reducing the power dissipation per unit area in an integrated circuit (IC) is an interesting research area. Two possible levels are important to be explored. One is at architectural level and other is at fundamental semiconductor device level. One interesting way of approaching this problem at device level is to reduce the operating voltage without compromising the switching characteristics. This can be achieved by investigating the steep slope devices that can provide less subthreshold slope(SS) than the traditional CMOS. Tunnel Field Effect Transistors (TFET) are most promising candidates of steep slope devices whose switching is based on quantum tunneling mechanism rather than thermionic emission as in CMOS. Due to quantum tunneling of electrons, the subthreshold swing of TFET is not limited by 60mv/dec. And also the leakage current is much lower than CMOS. This is because the of the high barrier that exists in the reverse biased P-I-N junction of TFET. Hence TFET has attractive applications in low power designs[13]. This paper gives a detailed comparison of effects of changing parameters like source doping , drain doping, using different gate oxide material and variation of body thickness for 20 nm DGTFET.

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II. MODELING OF DUAL GATE TFET(DGTFET)

This paper gives a detailed comparison of effects of changing parameters like source doping variation, drain doping variation, effect of high-k dielectric oxide material and variation in body thickness in 20 nm DGTFET.

Effect of gate oxide material variation: The effect of different gate materials on the performance of DGTFET is analysed. The source doping, drain doping, polydoping and body thickness are fixed to the values in Table 1 and different gate oxide materials are considered. The materials considered are SiO2, Si3N4 and HfO2 with the dielectric constants 3.9,7 and 25 respectively. In Fig 1, the Id-Vgs characteristics of the DTFET device with different gate oxide material is shown. When a high-k dielectric gate oxide layer is used, it increases the on current since the gate coupling is increased, in other words the control on gate is increased. So, the dielectric oxide layer most suited is HfO2 as it provides increased on current compared to other two oxide materials.

Effect of source doping level: The doping levels of the Tunnel FET device must be carefully optimized in order to maximize on current and Ion/Ioff ratio and minimize off-current. In tunneling transistors, the tunneling mechanism can be observed mostly between the interface of source and channel, hence the source doping must be carefully optimized. The drain doping, polydoping, oxide layer material and body thickness are fixed to the values in Table 1 and the effect of source doping level is studied. The DGTFET is simulated at source doping levels such as $1x10^{18}$, $1x10^{19}$,$1x10^{20}$ and $2x10^{20}$.The Figure 2 shows the graph that compares the Id-Vgs characteristics of DGTFET with these source doping concentrations. As the source doping is increased, the on-current is also increased since the bandgap is reduced. With the reduction in band gap, current characteristics parameters of the device are improved. Hence, the highest possible source doping is recommended for DGTFET optimization.

Effect of drain doping level: The source doping, polydoping, oxide layer material and body thickness are fixed to the values in Table 1 and the effect of drain doping level is studied. The drain doping level does not have much effect on the on current. However, the drain doping level is of importance in negative region of the operation. Tunnel FET shows ambipolar characterisctics which is undesirable. When the drain and source are equally doped, the ambipolar current is observed to be maximum. If the drain doping level is too low, the contact formation during the fabrication becomes extremely difficult. Hence for the optimization of the device, a relatively low drain doping level must be selected but it must not be too low that contact formation is not possible. Fig 3 shows the comparative graph of current characteristic of DG-TFET device with varying drain doping in atoms/cm^3 such as $1x10^{20}$, $1x10^{19}$, $5x10^{18}$and $1x10^{18}$.

Effect of poly doping level: The poly doping effects the control of gate in modulating the quantum tunneling. Hence poly doping is important aspect in the TFET device modeling. After the source and drain doping values are fixed to 10^{20} and $5x10^{18}$, the poly doping variation is performed for different values as in Figure 4. The best Id-Vgs curve was found for the poly doping value of $5x10^{18}$.

Effect of Body Thickness Variations: Another important parameter is body thickness of Silicon and TFET is very much sensitive to this thickness. The source doping,drain doping, polydoping, oxide layer material are fixed to the values in Table 1 and the effect of body thickness is studied. Fig 20 shows, the comparison of Id-Vgs characteristics of DG-TFET device with varying body thickness. For larger body TFET device, the tunneling probability reduces thus on-current also reduces. Therefore, thin body TFET structures are needed for better performance.. So for DGTFET optimization, thin body structures are beneficial but it must stay above some critical thickness so that on-current will not degrade.

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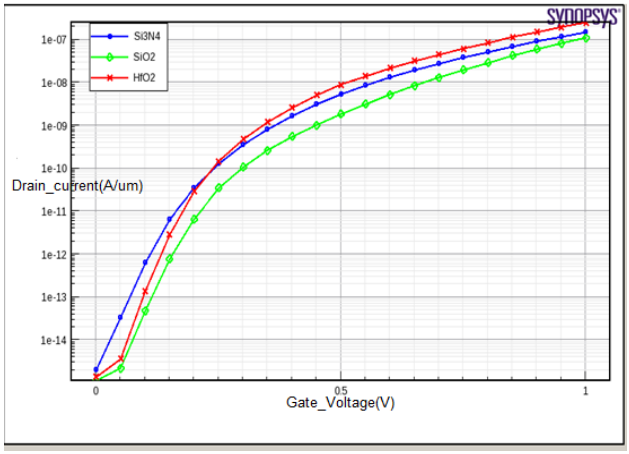

Fig. 1 Effect of high-k dilectric material oxides such as SiO2, Si3N4 and HfO2

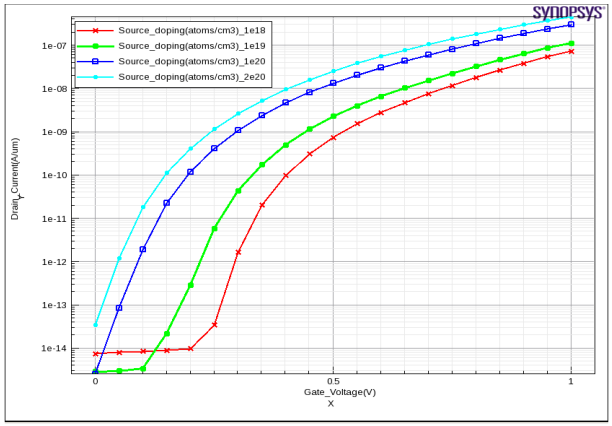

Fig. 2 Effect of source doping variation on TFET characteristics

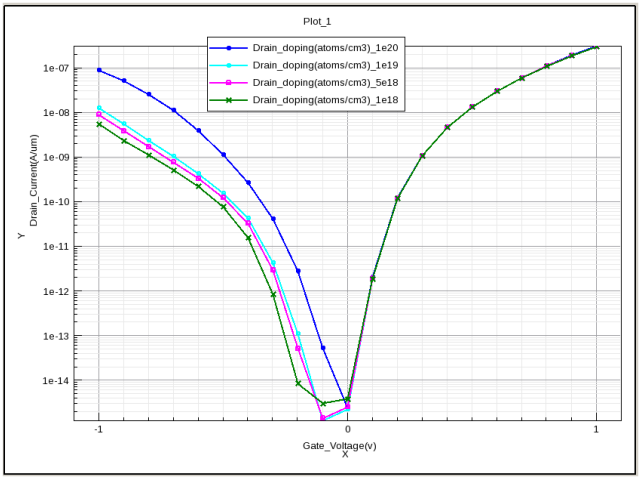

Fig. 3 Effect of drain doping variation on TFET characteristic

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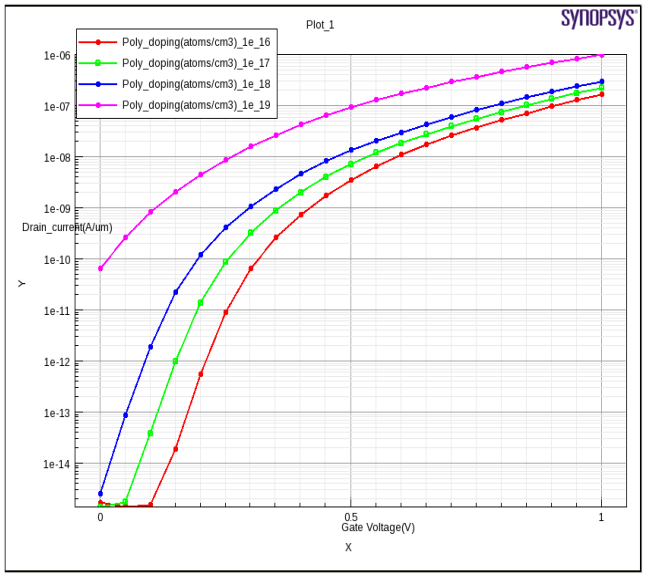

Fig. 4 Effect of poly doping variation on TFET characteristic

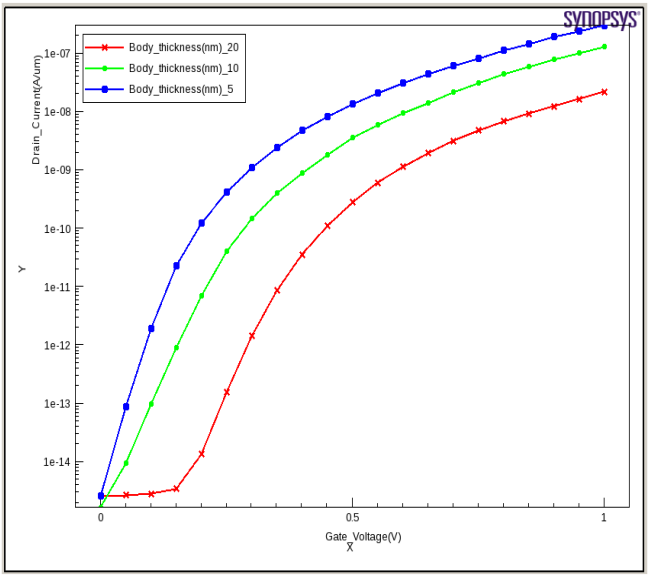

Fig. 5 Effect of body thickness variation on TFET characteristics

III. DEVICE STRUCTURE OF DGTFET AND SIMULATING THE I-V CHARACTERISTICS IN SENTAURUS TCAD

Based on the study of effects of different parameters the optimized device is modeled. The parameter table giving details of gate length, source doping, drain doping, effective oxide thickness and body thickness are selected by performing design of experiments[3] and the values are as given in Table 1. The optimized structure of DGTFET of gate length(Lg) 20nm is given in the Figure 6.

Figure 7 gives the I-V characteristics of the device. The values of the on current (Ion), off current(Ioff), Ion/ Ioff ratio, threshold voltage, subthreshold swing(SS) are respectively 0.256 uA/um, 1.425 fA/um, 10^8, 0.747V, 48.452 mv/dec.

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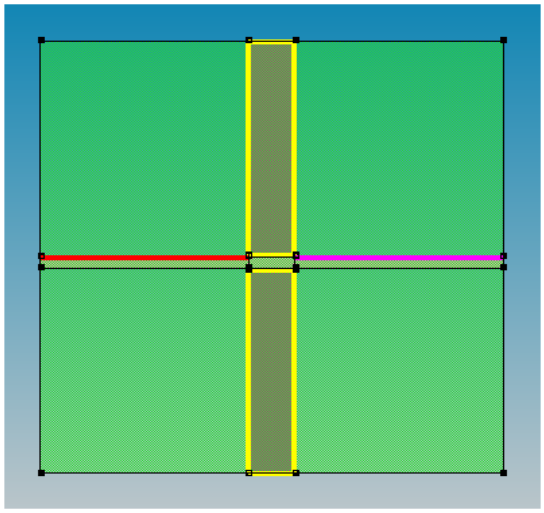

Fig. 6 Structure of DTFET of gate length 20nm in Sentaurus structure editor

TABLE I
Parameters used for DGTFET in fig. 6

Parameter	***Value***
Gate Length	20nm
Source doping (Boron)	1e+20/cm^3
Drain doping(Arsenic)	5e+18/cm^3
EOT	0.3nm SiO2 +0.6 HfO2
Body Thickness	5nm

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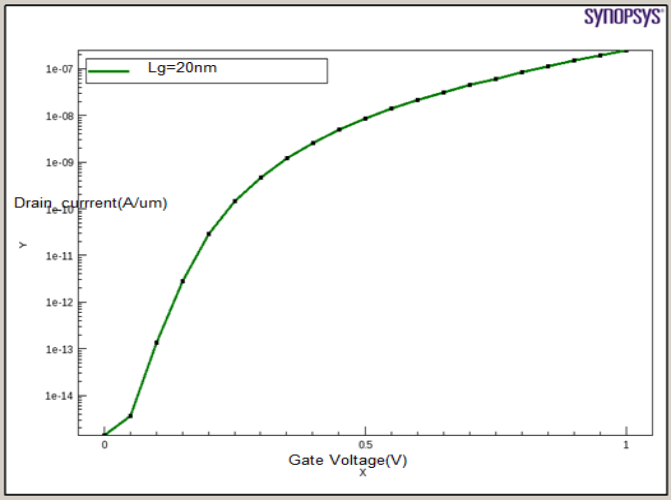

Fig. 7 Id-Vg Curve for DFET of Lg =20nm

IV. CONCLUSION

It can be summarized from the above work that the high performance TFET requires thin gate oxide with high-k dielectric material, abrupt doping profile, and source doping concentration must be relatively higher than that of drain doping concentration. When both the source and the drain are equally doped to a high doping concentration, then TFET exhibits ambipolar behavior which is not desired. The DGTFET shows a suthreshold slope of 48.452 mv/dec which is much less than the subthreshold slope of 60mv/dec as found in traditional CMOS. When compared to the ITRS for LSTP applications, the leakage current in DGTFET is decreased by 3 decades. Even though the off current is less (in terms of fA) in TFET when compared to the traditional CMOS, the on current is also decreased considerably. As a future work scope, to increase the on current, a heterojunction TFET can be explored with materials of different bandgap

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