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Design and Analysis of Arbiters for the NoC's Routers

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ABSTRACT: When number of Intellectual properties (IPs) increases in system on chip (SoC), bus based interconnection architecture may fail to provide power, latency and bandwidth. Solution to this problem is provided by NoC (Network on Chip). NoC is an embedded switching network. NoC approach helps in building communication systems among intellectual property cores in SOC which provides higher efficiency. There exists a logical element called router in NoC which selects the order of access of shared resources. There is increase in demand for efficient arbiters are in recent times. In this paper we propose fixed priority arbiter, variable priority arbiter and round robin arbiter that are more efficient when compared with previous arbiter architectures. FPGA implementation results of previous architectures and proposed architectures are provided, which shows improvement in performance of proposed arbiters.

KEYWORDS: Network on Chip, Routers, Round Robin Arbiter, FPGA implementation.

I.INTRODUCTION

Multiprocessors which integrate multiple cores has become the mainstream of computer architecture. In multiprocessors network on chip has become very popular as it provides high bandwidth[1]. Network on Chip consists of three fundamental building blocks, which are links, routers and Network interface. Links provides communication between routers. Links are nothing but a set of wires and it may contain a number of channels. Channel bandwidth is number of wires present in a channel. Link in network on chip comprises of synchronizing protocol from source node to target node or from target node to source node. Protocol consists of set of wires or it can be realized with the help of first in first out approach. Asynchronous links are an interesting case. It can be realized with the help of local handshake protocol. Links play a major role in determining performance characteristics of network on chips.

Routers consist of incoming ports, outgoing ports and crossbar switch matrix. Figure1 shows typical NoC router containing input ports, output ports and crossbar switch matrix[2]. Switch matrix helps in providing communication between incoming ports and outgoing ports. Apart from this physical network router comprises of logic module which is responsible for control flow in network on chip. Logic module helps in movement of data throughout network on chip. Control flow policy categorizes data communication throughout network on chip. Communication may be in network on chip level or in router level. If control flow policy is designed properly, issues related to deadlocks can be eliminated.

There are two types of control flow strategies, namely distributed and centralized. Centralized scheme aims at reducing the contentions by making decisions of routing at network on chip level. In centralized strategy, need of arbitration module is eliminated. Majority of the routers use distributed strategy. When the control flow is distributed decisions related to routing are carried out at router level. Virtual channels helps in multiplexing individual channel into number of independent channels with separate buffer queues. The fundamental job of virtual channel is to eliminate deadlocks and increase the performance of the system by reducing usage of wires. Usage of virtual channel makes the structure of arbiters more complicated. Let us consider an example wherein we have four virtual channels VC(0-3). Suppose, if VC0 and VC1 issues request through request lines r0 and r1. The arbiter performs arbitration and assigns one of the virtual channels VC0 to any of the output port.

Network interface provides communication interface between network and intellectual property core. Network interface helps to separate computation processes from communication processes. This helps in independent usage of

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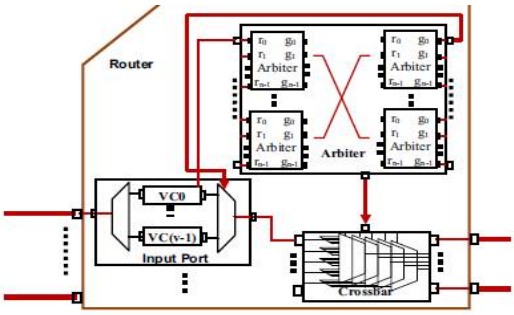

Figure 1:- NoC router

Communication infrastructure and core infrastructure effectively. Network interface is divided into two parts which are back end and front end. Front end deals with request from cores. Back end deals with protocol of the network.

II.LITERATURE SURVEY

In fixed priority arbiter the priority of the request lines is fixed. Figure 2 shows typical Fixed Priority Arbiter(FPA) with four input request. In fixed priority arbiter every input request is assigned with a fixed priority. If at any given time two requests arrives at the arbiter. Then only request with highest priority will be issued with a grant signal whereas, request with least priority is made to wait until request with higher priority ceases to exist.

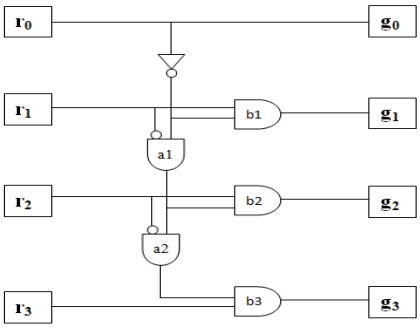

Figure 2:-Fixed Priority Arbiter architecture

These arbiters have the advantages of low power consumption, it occupies less area and architecture of these arbiters is simple when compares with other arbiters. These arbiters are commonly used in real time systems. The major disadvantage of fixed priority arbiter the lower priority requests should have to wait indefinitely until higher priority requests are serviced. This decreases the fairness of the arbiter and problems such as starvation requests increases.

Variable priority arbiter(VPA) has an advantage of modifying priority of the requests which is not present in fixed priority arbiters. In VPA search for successful request must start from highest priority and should carry on in cyclic order. The fairness of these arbiters are better when compared to fixed priority arbiters. Figure 3 shows typical variable priority arbiter with p_0,p_1,p_2 and p_3 as priority selection lines[3].

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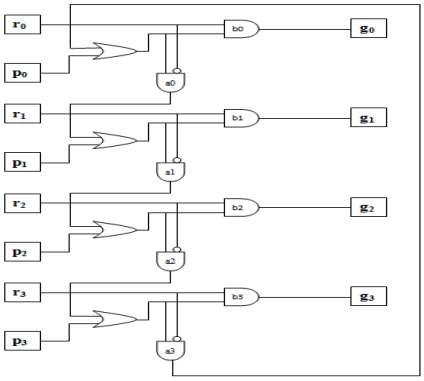

Figure 3:-Variable priority arbiter architecture

In round robin arbiter incoming requests are initially sorted in a cyclic order, so that we can find out the request with higher priority. In the next cycle of arbiter, the latest granted input gets the least priority. In this scheme, the recently granted input request will be served again only after all other requests are served. These arbiters can be used to build starvation free circuits. There are many variants of round robin arbiters which includes High Speed Decentralized Round Robin Arbiter(HDRA)[4]. HDRA is illustrated in Figure 4. Logic enclosed in the circle represents a filter circuit. These filter circuits' helps in finding the requests lines with no request and request line which has been processed recently serviced. The remaining request lines are then serviced one by one by setting the D flip flops of the filter to zero.

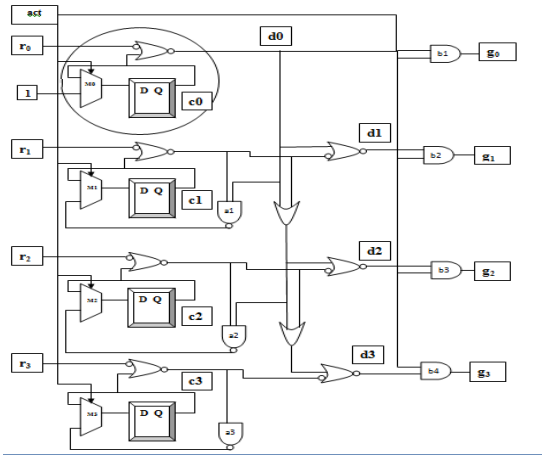

Figure 4:- Architecture of HDRA

III.PROPOSED ARBITERS

FPA occupies less area when compared to other arbiters trade off is that FPA exhibits weak fairness when compared to variable priority and round robin arbiters. Round robin arbiters' exhibits strong fairness but trade off is it occupies more area and has comparatively less maximum frequency than FPA and VPA. Hence, in this paper we are proposing a Fixed priority Arbiter(FA), Variable priority arbiter(VA) and a Round robin Arbiter(RA). Our proposed FA has multiplexers as shown in figure 5. The input requests are connected to the select lines of the multiplexers. The

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order of priority for requests is in the order $r_0 > r_1 > r_2 > r_3$. The output of multiplexer M_0 consists of the code corresponding to highest priority request line. We have designed an arbitration block which is shown in figure 6, that helps in analysing the code present at the output of M_0 and provides suitable grant signal.

Variable priority arbiter(VA) consists of multiplexer MP that helps in sorting of the codes produced by series of multiplexes having request lines as its select lines. The select line of MP is connected to priority selection input terminal P as shown in the figure 7. The output of MP is given to arbitration block which analyses the incoming code and issues corresponding grant signals. Since priority of the requests can be controlled with the help of P terminal, these arbiters' exhibits improved fairness when compared to fixed priority arbiters. Proposed Round Robin Arbiter(RA) is illustrated in figure 8. RA has series of multiplexers which are connected as shown in figure 8. These multiplexers help in providing code to the multiplexer MP corresponding to the input requests. For example if request r_1 is active then multiplexer M_1 provides 01 at the input terminal of MP. In RA select terminal of MP is connected to next_g and is incremented after every clock cycle in order to process every input request. MP is connected to arbitration block through D flip flop, which analyses the coded signals of MP and issues corresponding grant signals. In RA after servicing of each input request it is assigned with least priority and is serviced only after analysis of remaining requests. Hence, RA exhibits strong fairness compared to fixed priority arbiter and variable priority arbiter.

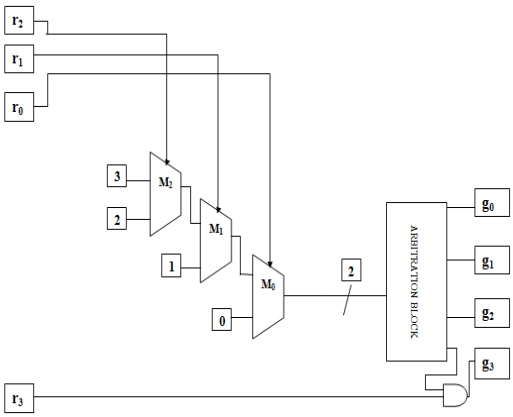

Figure 5:- Proposed fixed priority arbiter

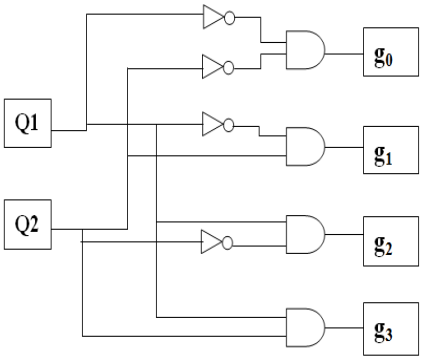

Figure 6:- Arbitration block

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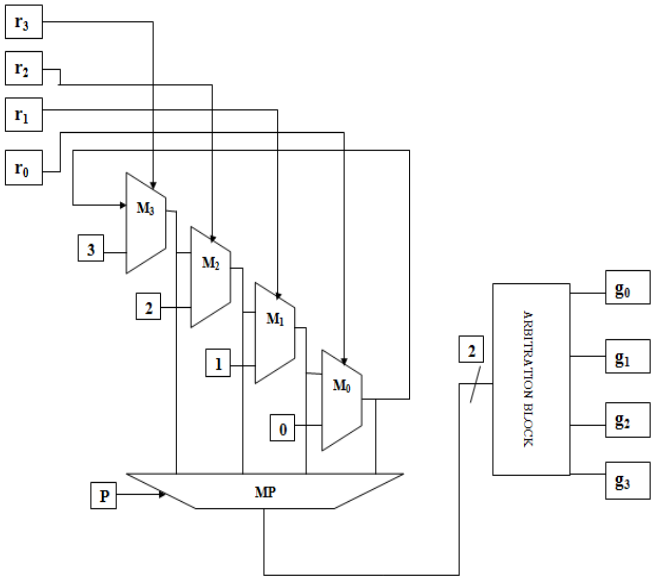

Figure 7:- Proposed variable priority arbiter

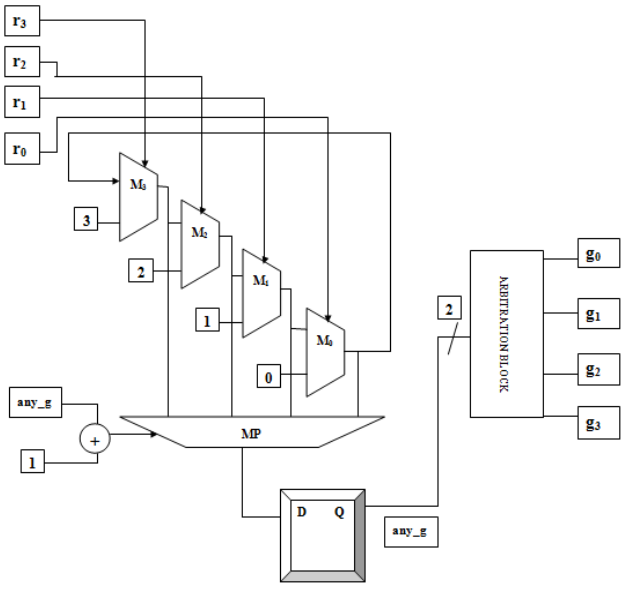

Figure 8:- Proposed round robin arbiter

IV.FUNCTIONAL BEHAVIOUR OF THE ARBITERS

In this paper implementation of the arbiters are done using Xilinx ISE 14.5 for Spartan 3E FPGA. In this section we are analysing functional behaviour of the proposed arbiter discussed in section III. Analysis of functional behaviour of the arbiters is done using timing diagram obtained after implementation of the arbiters in Xilinx ISE 14.5 which is illustrated in figure 9, 10, and 11. Input requests 1, 1, 0, 0 are applied to input terminals r_0, r_1, r_2, r_3 respectively of the proposed Fixed priority Arbiter(FA). As priority of r_0 is greater than that of r_1 only r_0 is issued with grant signal

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g_0. After 160ns, the inputs of the arbiter are 0, 1, 1, 1. Now grant signal is issued in the form of g_1 as, the priority of r_1 is greater with respect to r_2 and r_3 which is shown in figure 9. Figure 10 shows the timing diagram of proposed Variable priority Arbiter(VA) initially inputs of the arbiter are 1, 1, 1, 0. Priority input terminal P has a value of 0 which indicates that request r_0 has the highest priority hence, grant signal is issued for r_0 in the form of g_0. After 160ns, the inputs of the arbiter are 0, 1, 1, 1 and priority input terminal P has a value of 2 which indicates request r_2 is given highest priority. So, grant signal is issued for r_2 in the form of g_2. In proposed round robin arbiter(RA) initially the input are provided as 1, 1, 1, 0. In round robin arbiter whenever a grant signal is issued for a request it is assigned with least priority during next arbitration cycle and is only serviced after all other requests are serviced. Hence, grant signals g_1, g_2, g_3 are issued in cyclic order at each arbitration cycle as shown in the figure 11.

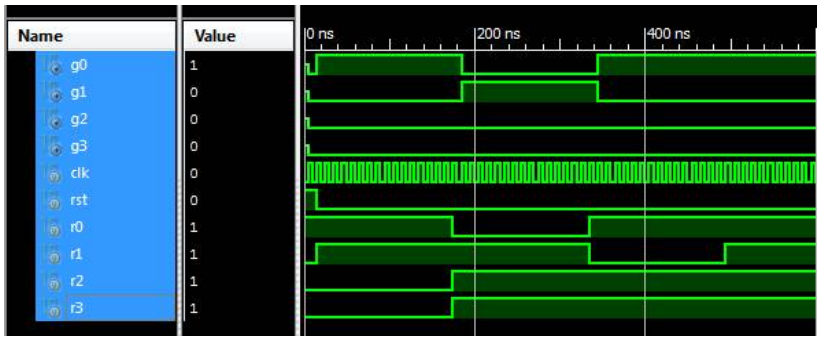

Figure 9:- Timing diagram of proposed fixed priority arbiter

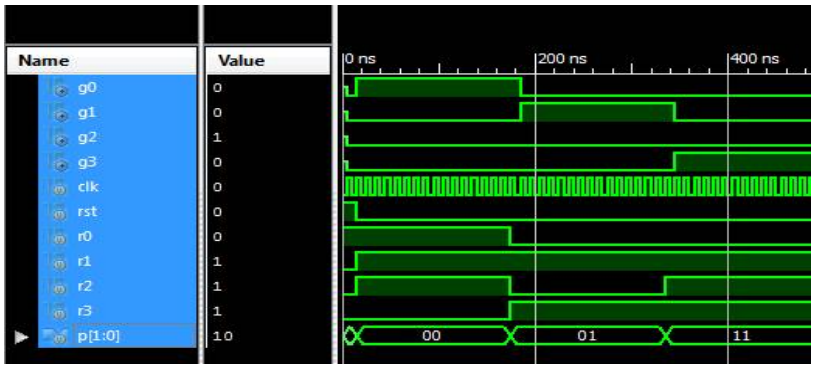

Figure 40:- Timing diagram of proposed variable priority arbiter

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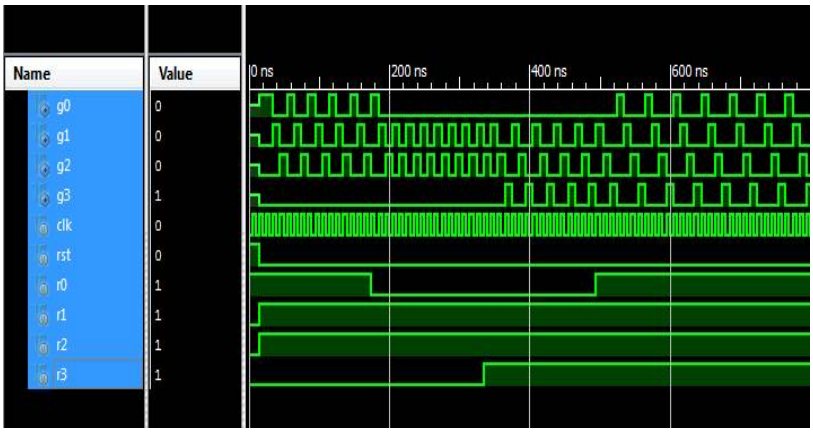

Figure 51:- Timing diagram of proposed Round robin arbiter

V. RESULT AND DISCUSSION

In this section we compare the results obtained from implementing the different arbiter architecture which are discussed in the previous sections. We have implemented FPA, VPA, HDRA, FA, VA, RA in Xilinx ISE 14.5 tool in order to analyse these arbiters. Number of slices and number of LUTs of the arbiter is the measure of its area. Speed of an arbiter is measured in terms of its maximum frequency. These parameters are tabulated in TABLE I, II, III. Characteristics of FPA and FA are tabulated in TABLE I which indicates that there is 11% increase in maximum frequency of proposed FA when compared with FPA. This implies that FA runs 11% faster when compared with FPA. Characteristics of VPA and VA are tabulated in TABLE II which indicates that proposed VA is 351% faster when compared to VPA. Characteristics of Round robin arbiters (HDRA, RA) are tabulated in TABLE III. TABLE III indicates that proposed RA occupies less area as it utilizes less resources of the FPGA when compared to HDRA. RA is 62% faster when compared to HDRA.

TABLE I. CHARACTERISTICS OF FIXED PRIORITY ARBITERS

TYPE OF ARBITER	NO. OF SLICES	NO.OF 4 INPUT LUTs	SLICE FF	NO.OF IOB	MINIMUM TIME PERIOD IN ns	MAXIMUM FREQUENCY IN MHz
FPA	5	3	8	10	1.793	557
FA	7	5	8	10	1.593	627

TABLE II. CHARACTERISTICS OF VARIABLE PRIORITY ARBITERS

TYPE OF ARBITER	NO. OF SLICES	NO.OF 4 INPUT LUTs	SLICE FF	NO.OF IOB	MINIMUM TIME PERIOD IN ns	MAXIMUM FREQUENCY IN MHz
VPA	7	9	8	14	5.562	179
VA	11	8	8	12	1.236	809

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TABLE III. CHARACTERISTICS OF ROUND ROBIN ARBITERS

TYPE OF ARBITER	NO. OF SLICES	NO.OF 4 INPUT LUTs	SLICE FF	NO.OF IOB	MINIMUM TIME PERIOD IN ns	MAXIMUM FREQUENCY IN MHz
HDRA	21	21	8	12	4.349	229
RA	9	9	6	10	2.675	373

VI.CONCLUSION

Arbiter plays a significant role in on chip communication of System on chips. Network on Chip is the latest method which helps in providing communication mechanism between intellectual properties(IPs) of a chip. In this paper we did comparative analysis of different arbiters and we conclude that proposed Fixed priority arbiter(FA) runs 11% faster when compared to FPA, proposed Variable priority Arbiter(VA) has an increase of 351% in its maximum frequency when compared with VPA, proposed Round robin Arbiter(RA) runs 62% faster when compared to HDRA. RA occupies lesser area when compared with HDRA.

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