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Simulation and Hardware Implementation of a New Multilevel Inverter Topology with Symmetric DC Sources Using Fundamental PWM Technique

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ABSTRACT: Multilevel inverters are preferred over conventional inverters as the quality of the voltage improves with the number of voltage steps at the output. A new cascaded multilevel inverter topology incorporating a new basic unit is proposed in this paper. The proposed topology utilizes fewer power electronic components to generate a specific number of output voltage levels. Resulting in compact and cost effective design. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, hence the structure of the proposed multilevel inverter is extended.
The effectiveness of the proposed multilevel inverter validated by mat lab Simulink software and a hardware setup was developed for single phase 9level for proposed topology using fundamental PWM technique and results are ensured the feasibility of the proposed configuration.

KEYWORDS: Concept of MLI, Pulse width modulation, Total Harmonic Distortion (THD)

I. INTRODUCTION

MLI concept was first introduced in 1975. It is a power conversion device which produces an AC output voltage by using dc power sources. Multilevel inverters can produce a waveform of desired single or three phase voltage. Multilevel voltage source inverter reduces the THD of the output voltage and does not require transformers. With the increasing number of voltage levels, the power handling capability increases. Also the output waveform of staircase shape approaches to sinusoidal wave with minimum voltage stress. For increase in every level, the number of semiconductor power switches is increased.

The main function of the inverters is to convert DC input voltage to an AC output voltage of the desired magnitude. The output voltage waveforms of the inverters should be sinusoidal, however the waveform of the practical inverters are non sinusoidal and contains different harmonics. By using high speed power semi conductor devices and by using different switching techniques we can reduce the harmonic content in output voltage.

Therefore multilevel inverter (MLI) has been introduced for working with higher voltage levels due to better harmonic spectrum and high power capability. Renewable energy sources such as photovoltaic, wind and fuel cells can be utilized in MLI system for high power application. Square wave or quasi-square-wave voltages are acceptable only for low and medium power applications, but for high power applications low distorted sinusoidal waveforms are required.

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II. LITERATURE SURVEY

A multilevel voltage source inverter topology consisting of DC links and H-bridge inverter is based on minimization of switches, clamping diodes, or capacitors. Level generation cells produce dc voltage of staircase shape and H-bridge inverter produces positive and negative polarity to generate an AC voltage. To reduce switching losses and device stresses, soft switching techniques can be employed. With the increase in voltage levels, this configuration finds application in motor drives, distributed power generation involving fuel cells and photovoltaic cells.

MLI topology with reduction in number of power electronic components reduces the number of switches, gate driver circuits, installation area and cost. Bidirectional switches are employed in multilevel inverters to improve the performance in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels.

Conventional inverter as the quality of the output voltage improves with the number of voltage steps at the output. A new single phase multilevel inverter topology incorporating a new basic unit is proposed. The proposed topology utilizes fewer power electronic components to generate a specific number of output voltage levels in comparison with the other multilevel inverters resulting in compact and cost effective design.

III. SCOPE OF THE RESEARCH

MLI topologies with less number of switches reduce the initial cost and complexity. With increase in number of levels, the number of switches used is very less compared to the other MLI topology. Since switching losses reduces the efficiency of the system, fuel cell based multilevel converter with reduced switches is proposed. The main aim of this topology is to minimize the number of switches, gate driver circuits, capacitors and THD.

Compared to other Multi level inverters, reduces roughly half of the switches and gate drivers. This leads to smaller size and volume. The objective is to use reduced switches in MLI topology is to increase number of levels with less number of switches and sources. This topology reduces the total harmonic distortion, lowers the electromagnetic interference and produces high voltage.

IV. METHODOLOGY OF A NEW PROPOSED MLI

INTRODUCTION

The proposed topology is depicted in Figure 1. The basic unit has three unidirectional switches (S1, S2 and S3) and three dc sources (V1, V2 and V3). Switch S1 is connected in series with the source V2 and switch S2 is connected across the source-switch assembly. Care must be taken that both the series and the parallel switch are not turned on simultaneously. The remaining sources V1 and V 3 are connected in series on either side of the source-switch assembly.

PRINCIPLE OF OPERATION

The basic unit can generate two distinct voltage levels besides zero. It can also be noted that only one of these three switches is turned on at any point in time to avoid short circuiting of the dc sources. As the lowest voltage that is generated by the basic unit is V1+V3 (2Vdc , if V1 =V3 =Vdc), an auxiliary unit is required to generate lowest step (Vdc). The basic unit together with the auxiliary unit can generate all positive the voltage steps. To generate the negative voltage steps, a polarity generator circuit (H-bridge) is connected with this basic-auxiliary unit assembly. The auxiliary unit has a dc voltage source whose magnitude is equal to the lowest voltage step (Vdc) to be generated. In addition, two unidirectional switches (Sa and Sb) are provided to include or exclude the dc source from the rest of the circuit.

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Care must be taken that these two switches (Sa and Sb) are not turned on simultaneously. Further, the switches that belong to the same leg of the polarity generator (H1 and H3 or H2 and H4) should never be turned on simultaneously. Required numbers of basic units can be cascaded further to generate more steps at the output.

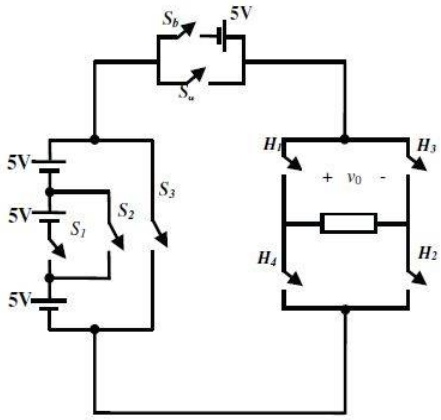

Fig 1 circuit diagram of proposed inverter

OUTPUT VOLTAGE	S_1	S_2	S_3	S_A	S_B	H1	H2	H3	H4
0	0	0	1	1	0	1	0	1	0
$+V_{dc}$	0	0	1	0	1	1	1	0	0
$+2V_{dc}$	0	1	0	1	0	1	1	0	0
$+3V_{dc}$	0	1	0	0	1	1	1	0	0
$+4V_{dc}$	1	0	0	0	1	1	1	0	0
$-V_{dc}$	0	0	1	0	1	0	0	1	1
$-2V_{dc}$	0	1	0	1	0	0	0	1	1
$-3V_{dc}$	0	1	0	0	1	0	0	1	1
$-4V_{dc}$	1	0	0	0	1	0	0	1	1

Table 1 Switching Sequence for Single Phase Nine Level Proposed Inverter

GENERALIZED STRUCTURE FOR N-LEVEL

Required numbers of basic units can be cascaded further to generate more steps at the output. The extended structure of the proposed inverter with 'n' basic units is shown in Fig.2. The output of this structure is equal to the sum of the output of the basic units and auxiliary unit. If the output voltages of the basic units are v01, v02, etc. and that of the auxiliary unit is *va*, then, the output voltage of the extended topology and is given by

$$v0(t)= v01(t)+ v02(t)+ v03(t)+...+ v0n(t)+ va(t)$$

The basic units along with the auxiliary unit generate the voltage levels while the polarity generator determines the polarity of the output. The number of voltage sources and switches required are given by

$$N \text{ sources} = 3n +1$$

$$N \text{ switches} =3+6n$$

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Where, n is the number of cascaded basic units. It is a well established fact that the number of voltage steps Generated at the output depends on the choice of magnitude of the dc voltage sources.

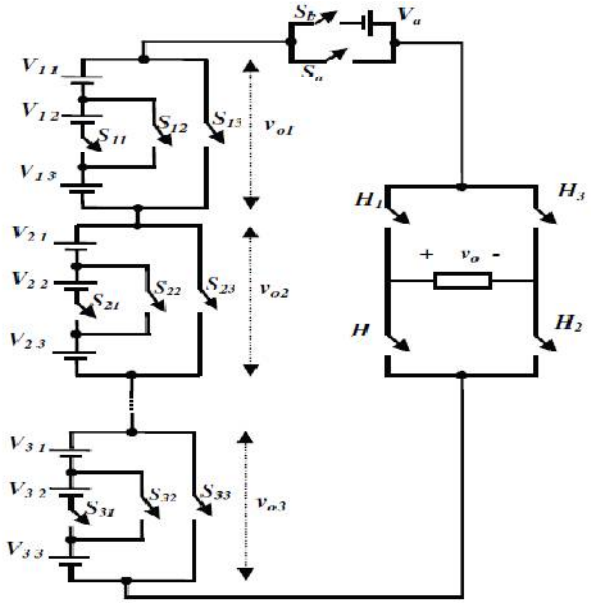

Fig 2 Generalized structure of the proposed topology

V. SIMULATION RESULTS

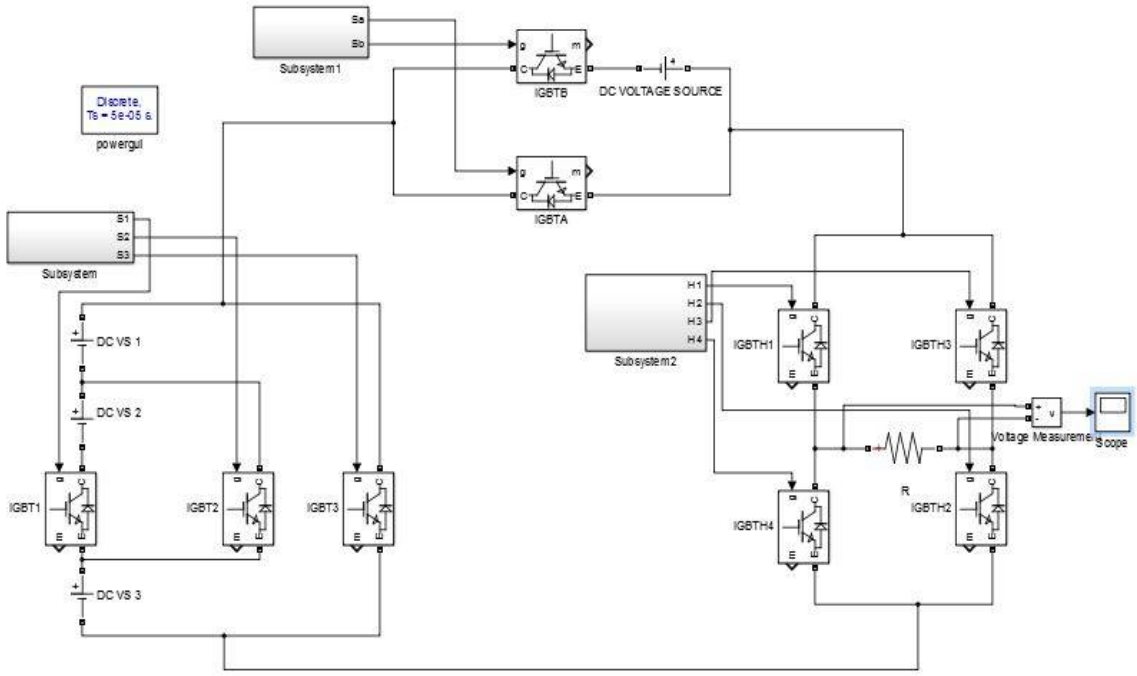

Fig 3 Simulink simulated circuit of a Single Phase 9Level Proposed Topology

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In Fig 4, Fundamental PWM switching pulses for various switches using Mat lab simulink.

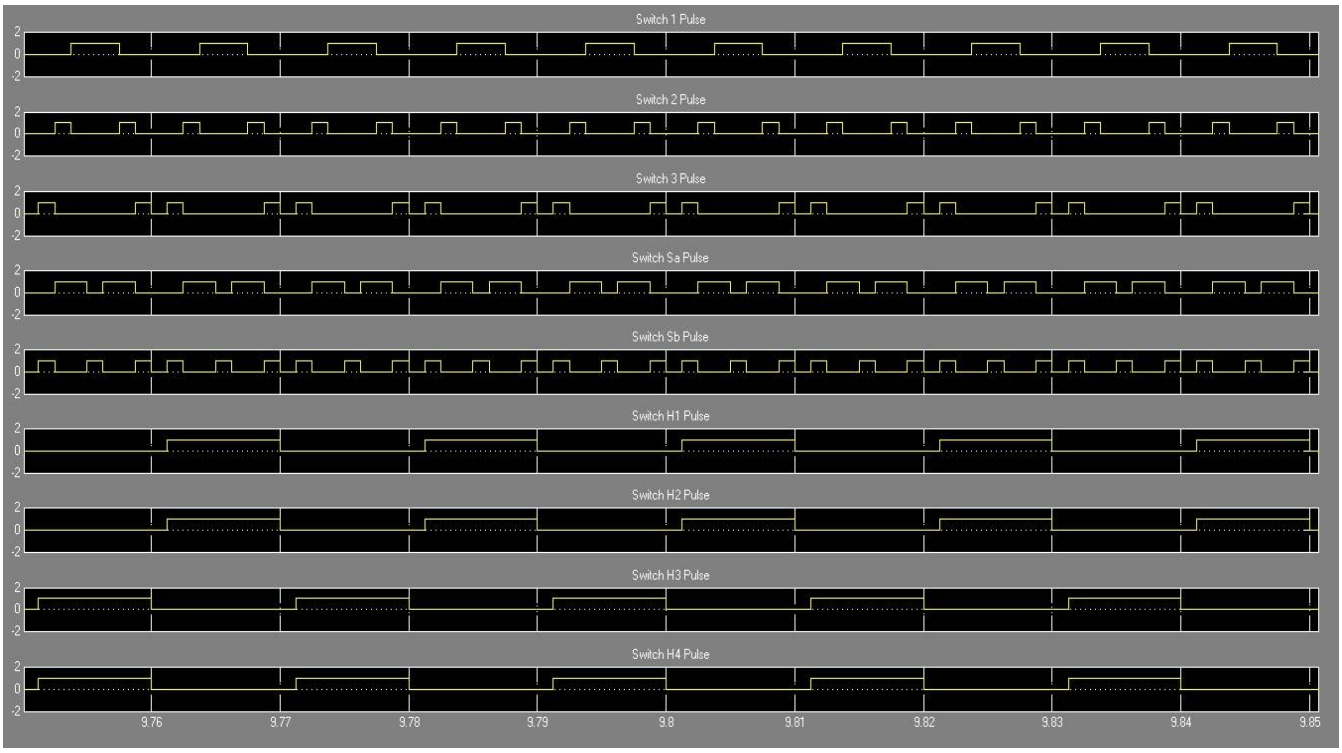

Fig 4 PWM pulses for various switches

In Fig 5, When each source of 9volts feeding the circuit, Output waveform of a 9level Proposed multilevel inverter insteps of 9v with an fundamental PWM switching technique using Mat lab simulink.

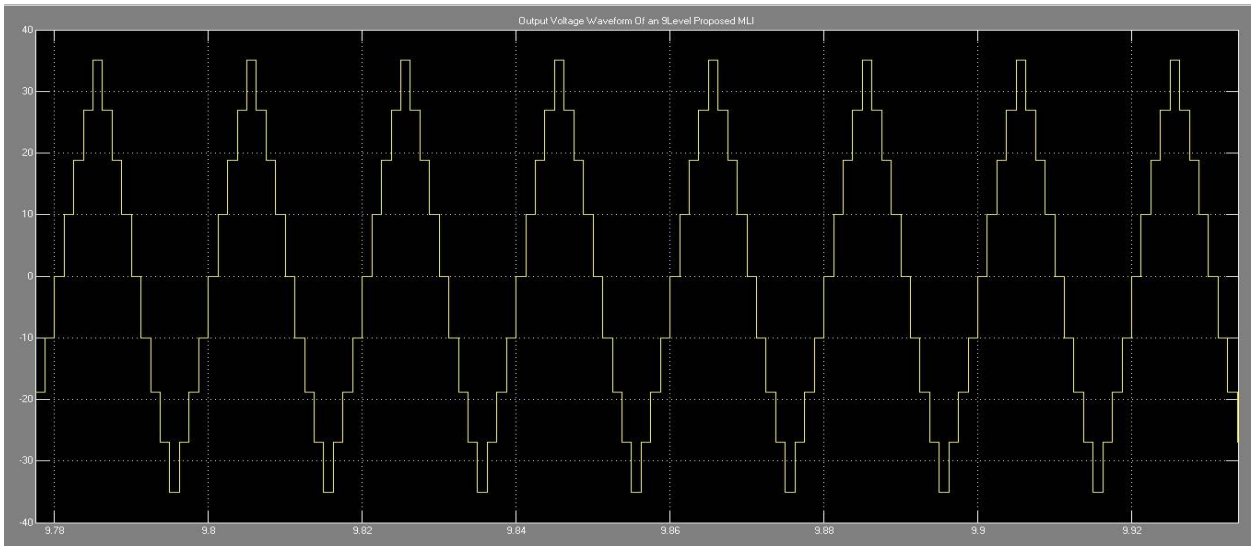

Fig 5 Simulated waveform of a 9level Proposed MLI

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In Fig 6, when an output waveform is analyzed using FFT analysis in Mat lab simulink, Total harmonic distortion can be obtained. Here THD is about 15.51%

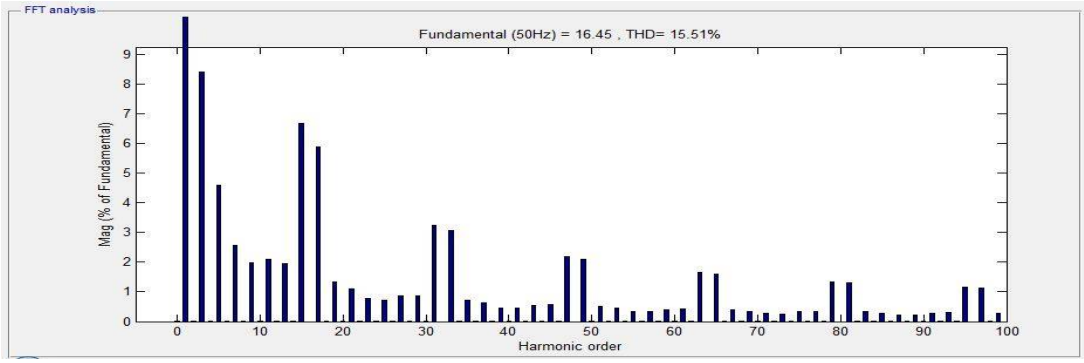

Fig 6 Harmonic Spectrum of 9level Proposed MLI

VI. HARDWARE RESULTS

A prototype of 36V (fig.7), single phase nine level proposed topology is constructed using MOSFETs as the switching device. 9volt four symmetric DC sources feed the inverter and at the load (3kΩ-50watt) output voltage of AC RMS 17volts obtained.
List of Components used are:
MOSFET (IRf840),
Voltage Regulator (7805, 7812),
Buffer (CD4050B),
Opto Isolator (EL817),
MOSFET Driver (IR2101).

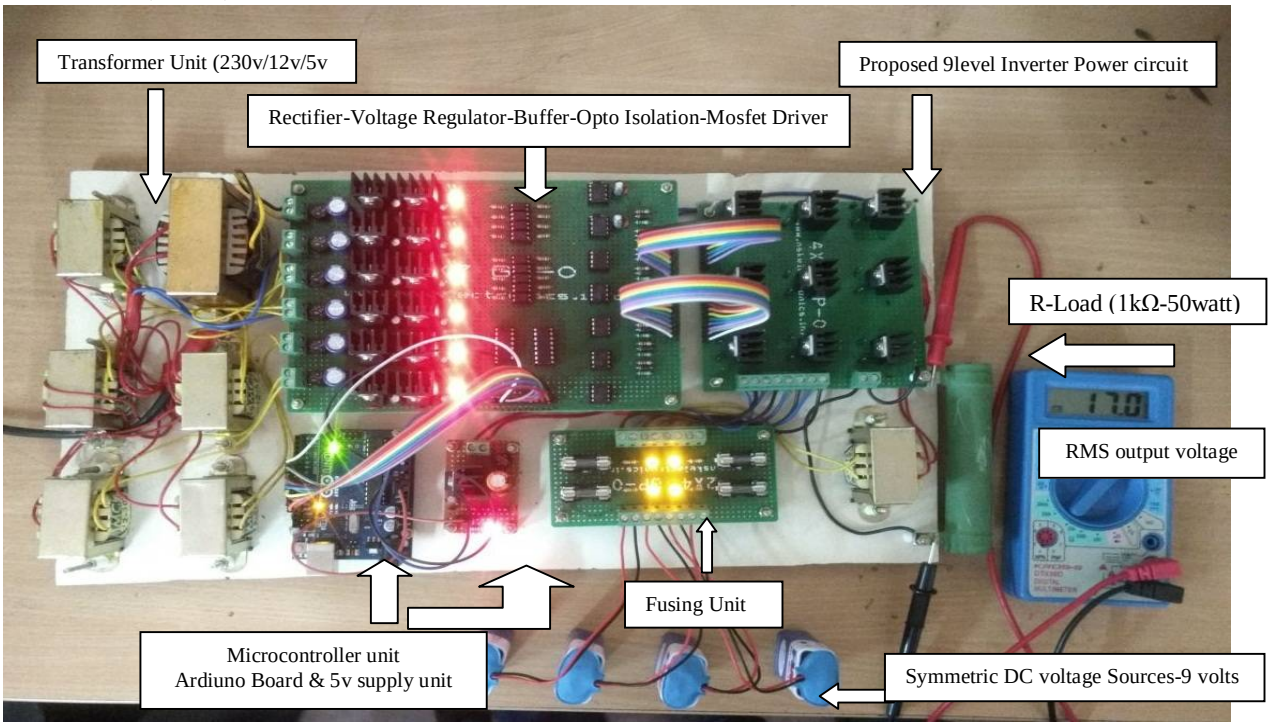

Fig 7 Hardware MLI circuit of a Single Phase 9Level Proposed Topology

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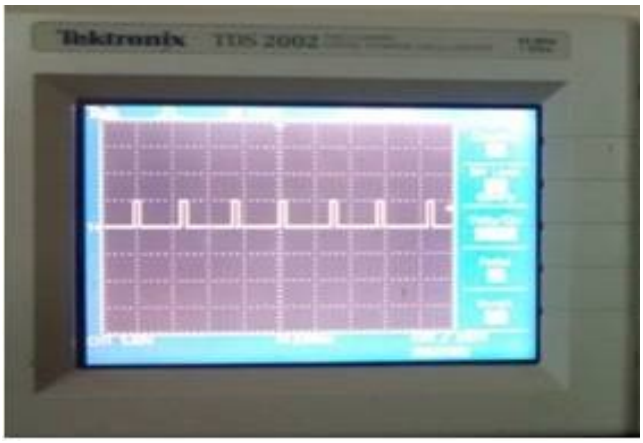

Fig 8 PWM pulse for switch 1

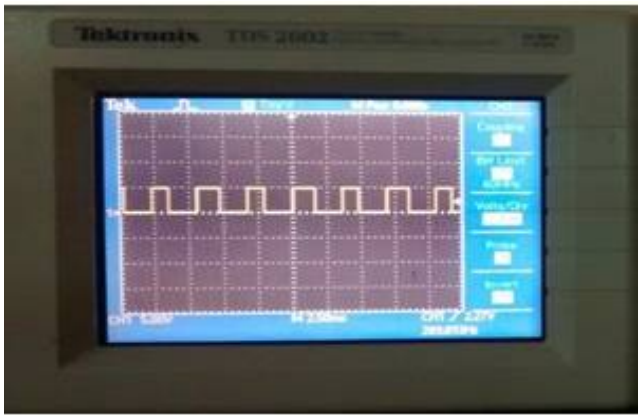

Fig 9 PWM pulse for switch 2

Fig 10 PWM pulse for switch 3

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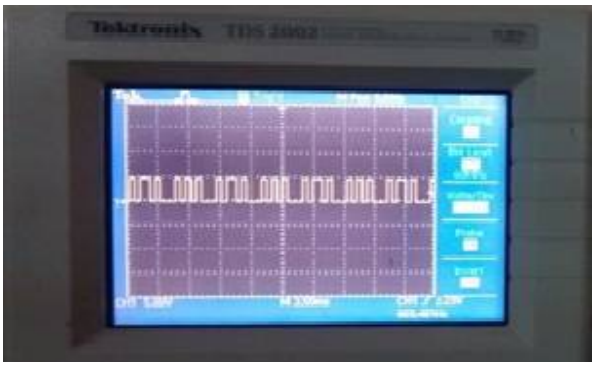

Fig 11 PWM pulse for switch Sa

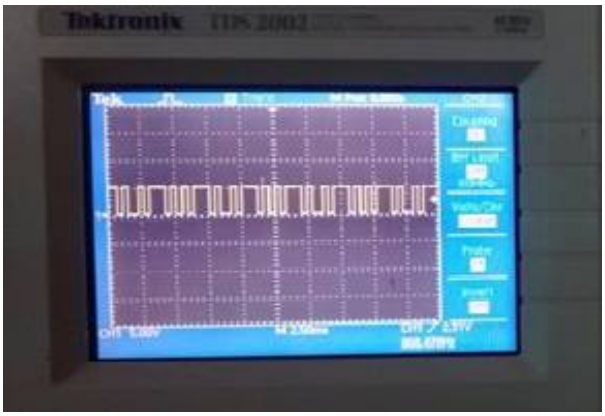

Fig 12 PWM pulse for switch Sb

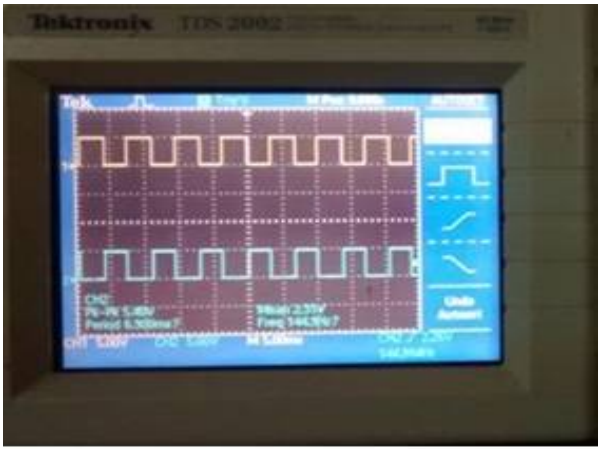

Fig 13 PWM pulse for switches H1 & H3

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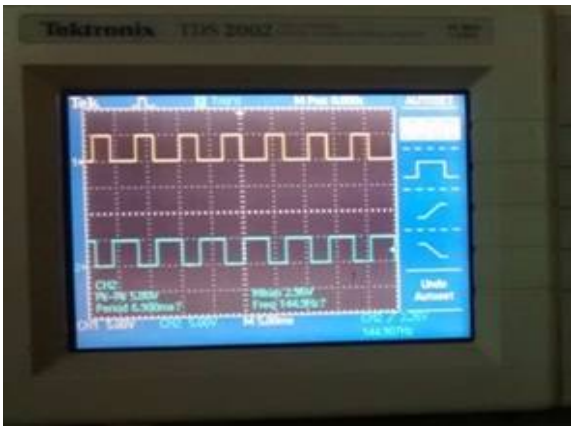

Fig 14 PWM pulse for switches H2 & H4

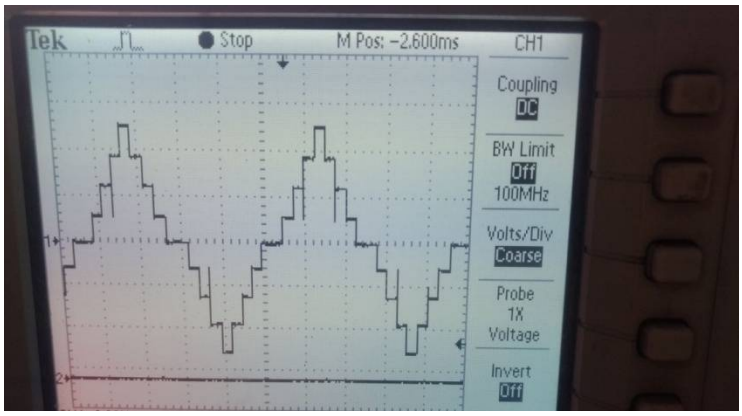

Fig 15 single phase 9 level Output voltage waveform of proposed MLI

VII. CONCLUSIONS

The proposed inverter implemented now can produce nine level voltages but with the modification to the inverter we can achieve more levels with which the THD at the output is further reduced. There is further scope to reduce the switch count and also number of carrier signals in modulation technique used. Advanced modulation techniques can be applied. Results are analyzed using FFT analysis for observing the THD of about 15.51% in fig (6).

A prototype of 36V, single phase nine level proposed topology is constructed using MOSFET's as the switching device. The inverter consists of 9 MOSFET switches. The MOSFET's IRF840 are used in the hardware set up. Ardiuno microcontroller is used to generate the gate signal for inverter switches. In total four symmetric DC source voltage of 9v each is applied across the input side of 9level proposed inverter. The proposed inverter output provides power to a resistive load (3KΩ-50watt). The output voltage waveform of the proposed MLI is a stepped wave with nine levels in fig (15) Shown.

REFERENCES

[1] S.Malathy, R.Ramaprabha *"A New Single Phase Multilevel Inverter Topology with Reduced Number of Switches*" Department of Electrical and Electronics Engineering, SSN College of Engineering, Rajiv Gandhi Salai, Kalavakkam, Chennai, India.2016
[2] Nagaraja Rao, Ashok Kumar and Ch.Sai Babu, *"New Multilevel Inverter Topology with Reduced Number of Switches Using Advanced Modulation Strategies," International Conference on Power, Energy and Control (ICPEC)*, pp.693-699, 2013.
[3] Rashid. M.H, *"Power Electronics circuits devices and applications"*, PHI 3rdedition, 2004 edition, New Delhi
[4] N. Mohan, T. M. Underland, et al., "*Power Electronics Converters, Applications and Design*", 3rd edition, John Wiley & Sons, New York, 2003