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A Low Power Multi-Bit 4TH Order ΔΣ ADC for High Security Application

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ABSTRACT: The main objective of the project is to design a low-power delta sigma ADC by using higher order ADC, which is applicable for high resolution image processing systems for security purpose. The order used here is 4th order ADC (4th order delta sigma ADC) is used to change the sampling clock of delta sigma ADC which will accurately change the power consumption levels of the ADC & the resolution of the image signal is also improved with the proposed design. The objective of the project is to develop the delta sigma ADC which takes an analog input and converts the analog signal into the digital form. The main advantage of this Delta sigma ADC is that it consumes low power, uses less storage memory area, with high resolution. The of the proposed project is to perform synthesis so as to obtain the physical netlist required for the physical design of the system. The synthesis is done by using Synopsys Design vision compiler which is also used for area, power, timing analysis for the proposed design. The physical design of the chip is carried out in CADENCE Encounter. By performing the physical design (PD) in CADENCE the chip layout is obtained for the proposed project. While comparing with the previous work, the proposed design can show the reduction in the power consumption levels of ADC which can be called as cost efficient high resolution Analog-to-digital converter. The power consumption of the proposed circuit is 5848nW and the operating frequency of the circuit is 1.6 MHz. This design is also applicable for the resolution refinement of Audio signals processing and in the various fields in which analog signals resolution should be improved.

KEYWORDS: ADC, Sigma-Delta modulator, image sensor, CMOS technology, power consumption, resolution, op-amp

I .INTRODUCTION

The recent research on Radio Frequency (RF) communication gives both higher integration, to meet low-cost, low-power, small-form factor personal communication device. This power reduction can be achieved be obtained by moving from larger feature size to smaller feature size. The performance of the device will be affected in the process variations and other- idealities. For portable devices like mobile the Analog to Digital Converters (ADC) should achieve low power dissipation, low noise, high speed, less Offset voltage. The Analog to Digital converters has become very popular in wireless application because of its increased performance and flexibility. Oversampling is defined as the type of sampling that uses a sampling rate that is much greater than the bandwidth of the signal. Further filtering and down sampling comes under digital signal processing. The delta sigma ADC comes under Oversampling type. When compared with other ADC's delta sigma ADC is used popularly because it consumes low power, uses low bandwidth, low cost, high resolution and has its applications in communication, signal processing, DSP, ect., This technique has been used in early stages of pulse code modulation (PCM) systems. This technique has been in use for many years, but the advancements in technology made this device popular and made it practical by wide spreading over the world. Now a day it has become a essential component for modern voice band, audio and high resolution application. Therefore, the delta sigma ADC has its applications in parameters like low cost, low power, high resolutions.

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1.1 TYPES OF ANALOG TO DIGITAL CONVERTERS

Depending upon the sampling rate Analog-to-Digital Converter (ADC) can be differentiated in to two. One which samples the signal at Nyquist rate that is fN=2F, Where fN is the sampling rate and F is the bandwidth of the input signal, while in the other samples, the signal which is at a much higher sampling rate in the signal band width, this type of sampling is called oversampling and the converters are called oversampling converters. These converters have an ability to achieve high resolution, high reliability, and better performance.

Types of analog to digital converters are

1. Nyquist rate converters
2. Oversampling converters

1.1.1 NYQUIST RATE CONVERTERS

The nyquist rate converters uses should satisfy the nyquist criteria which states that fs> 2B where fs is the sampling frequency and 'B' is the bandwidth.

Some of the Nyquist rate converters are

1. Flash ADC
2. Digital Ramp ADC
3. Successive Approximation ADC
4. Tracking ADC
5. Pipeline ADC

1.2 BASIC STRUCTURE OF DELTA SIGMA ADC

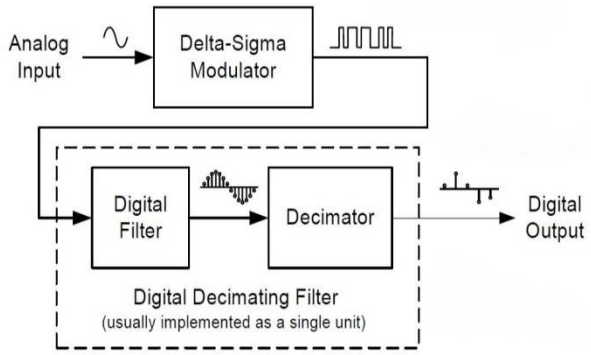

Fig:basic structure of ADC

The project is implemented in virtuoso and simulated in MATLAB. The project consists of integrator, comparator, summing module, quantizer and decimation filter. At the output side we have a block to check power spectral density and the output waveforms. The below block diagram represents the basic structure of the analog to digital converter.

The basic working of the analog to digital converter is given as shown in the figure. At the initial stage aanalog input signal is give which is a sine wave to the delta sigma modulator in which the input is given to the integrator where the analog signal is converted to the pulse form. The output of the delta sigma modulator is given to the digital filter in order to change the pulses to a quantization output. The digital output is further given to the decimation filter where the digital output is further minimized by decreasing the number of samples at the output side.

The delta sigma used here is of 4^{th} order delta sigma ADC. The advantages of using higher order ADC is to eliminate the higher harmonics caused by the ADC modulator. The other advantage of using higher order delta sigma ADC is that it can be implemented for high resolution applications which are the pa rt of the image processing.

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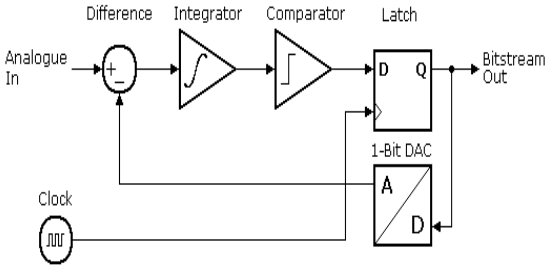
Fig: Basic structure of delta sigma ADC



Initially the analog input is given to the circuit and the signal is passed through the integrator and the comparator And the required output is brought at the output which is in the digital form. The functionality of the basic delta sigma analog to digital converter is to convert the analog input into the digital form i.e discrete.
The expected output waveform is given as shown below.

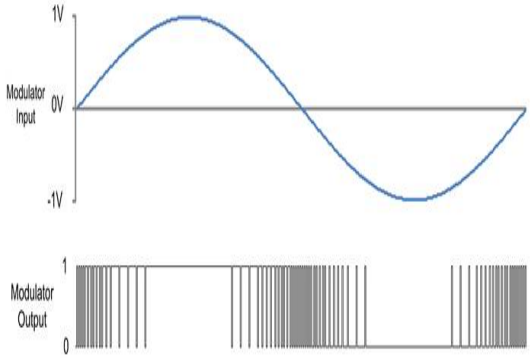


Fig: expected output of delta sigma ADC

III. HARDWARE IMPLEMENTATION

In this project the hardware implementation is done by using verilog code which is written for the delta sigma ADC architecture block. The delta sigma ADC block is designed in matlab 14b . The ADC architecture is implemented in cadence tool. Many software's are included in cadence tool. For this project the tools utilized are (NC- NATIVE CODE for Simulation), (RC- RTL complier for synthesis) and encounter digital implementation tool for soc (Physical layout of standard cells). Finally we obtain a chip layout of IFFT architecture , Area and power of the chip layout. From there GDSII file was generated for fabrication of the chip.

IV. OUTPUTS

The outputs given below are produced from 4th order delta sigma ADC which is designed in the MATLAB. The ADC output and the power spectrum output are shown below for the proposed delta sigma ADC.

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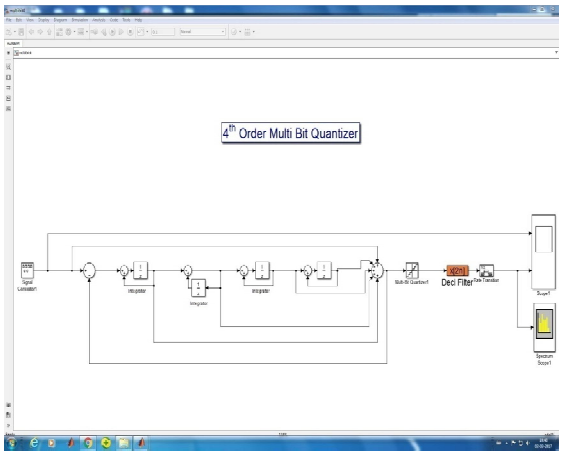

fig. delta sigma ADC

This is the block diagram of delta sigma ADC for high security purpose. The outputs are represented by showing them in terms of power spectrum and digital outputs.

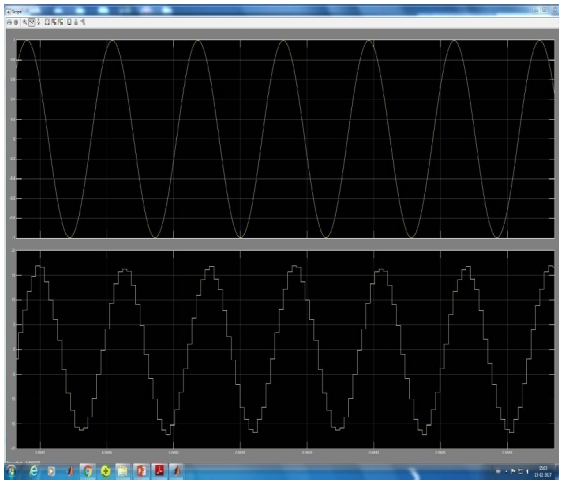

Fig. input and output comparision of delta sigma ADC

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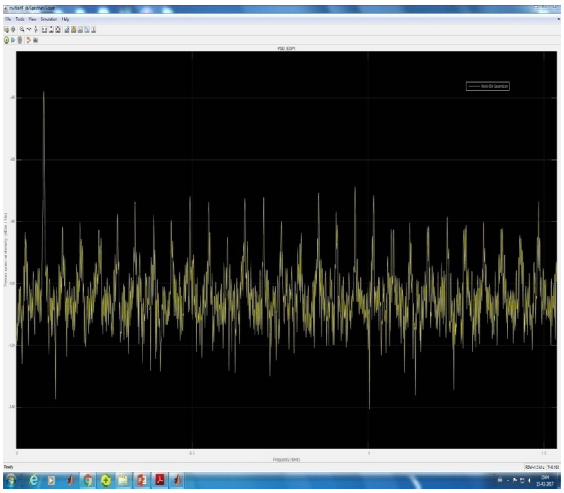

Fig: Power spectrum

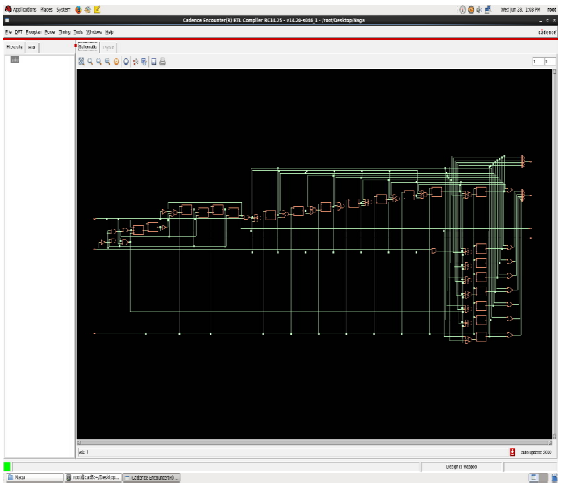

Fig: rtl output

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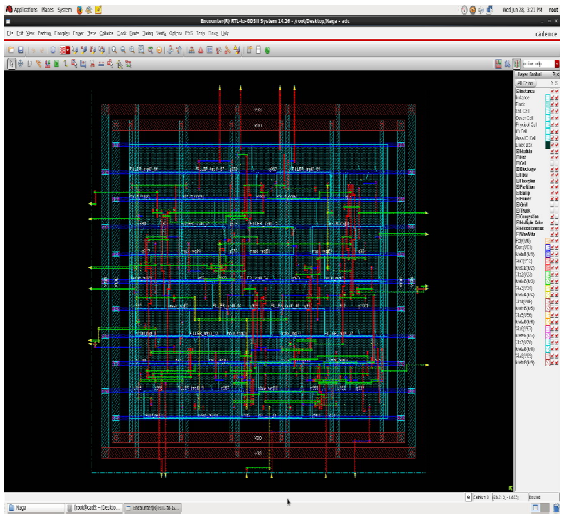

Fig: layout of proposed ADC

The layout and the native compiler outputs are shown above. These outputs are obtained by using the cadence tools.

V. APPLICATION

The proposed application for the project is that this is applicable for image capturing with the help of image sensor for high security purpose. Firstly when an object comes near the sensor it captures the image of the object, which is in the analog form. As we know that the analog is difficult to simulate and it is a bit difficult to calculate the parameters and tough to analyse. Because of this reason we are going for the ADC where the analog input is converted to digital form. Secondly this analog continuous signal is given to the Delta sigma ADC where this converts this analog signal to discrete form. Where the discrete signal is easy to analyse by the electronic device. The parameters are analysed and the discrete output is passed through the decimation filter where the output sample rate is decreased. By this project we are trying to reduce the power consumption and tried to increase the resolution of the picture. The resolution is increased by applying the below MATLAB circuit. Here, the application is done in MATLAB by using some blocks. Initially the input for the block is given in image format which is in .jpeg format. The image is passed through the above block by undergoing integration, quantization and gives the output i.e an image which has high resolution comparatively to the input image.

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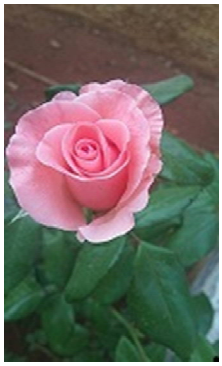
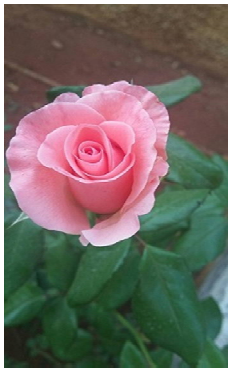
APPLICATION OUTPUT





SPECIALIZATION	CHIP RESULTS
process	UMC 180nm
Core area	121613μm²
Power consumption	15mW
Power Supply voltage	1.8v
Average off set voltage	0v
Input power range	0 to 1.8v
Operating frequency	1.6MHz
SNR	100dB
Band Width range	1.2khz – 100mkhz
Resolution	320 pixel

VI. CONCLUSION

In this project the system level design of the low power ADC which includes the integration of delta sigma ADC, Quantizer, decimation filter circuits are implemented. The input signal to the delta sigma ADC is selected by using a signal generator to which an analog signal is given as the input. The design is modelled by taking the sine signal features as the input parameters. As the delta sigma ADC converts the sine signal into digital form i.e. converting the analog signal into the digital form. The efficiency of quantizing for deciding the sampling clock of ADC can be

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concluded by observing the power consumption levels of ADC at different clock periods. The SoC implementation of the proposed design reduces the area, power consumed by the circuit. The results show that this work not only improves the quality of the signal but also improves the resolution. The obtained chip area is about 121613μm^{2}and the power consumed by the device is mW. Finally the resolution of the image is increased.

VII. FUTURESCOPE

The work presented in the thesis can be extended in several directions. Several research ideas might be followed for further applications. The possible improvements can be given as follows:

In future works, the circuit can be designed by using self-biased super amplifier architecture for ADC systems, more efficient techniques and more flexible hardware architectures can be developed for high resolution applications such as image processing systems. The future work of improving the resolution can be done by analyzing the rules of the image processing.

Another possible future work is expanding the range of input signal parameters and the design of Sigma- delta ADC can be designed by using various low power techniques.

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BIOGRAPHY

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