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FPGA Based Speed Control of Single Phase Induction Motor by Using PWM Technique

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ABSTARCT: Inverters are circuits that convert DC source into AC source. These DC-AC inverters have been widely used for industrial applications such as motor speed control, output voltage control, Emergency power supply, uninterruptible power supply (UPS),etc.Power switches are used in inverter with UNIPOLAR SPWM techniques. The SPWM techniques reduce harmonics and improve fundamental. It also reduces THD of voltage. Another important thing is to design the control circuit to provide switching signal to the power circuit. The control circuit consist of FPGA kit, opto-coupler, and voltage amplification. The Power Circuit consist of MOSFET Switches. A **field-programmable gate array** (**FPGA**) is an integrated circuit designed to be configured by a customer or a designer after manufacturing. The FPGA Real time controller is used to generate PWM pulses at different frequencies by different carrier frequencies. The modulation index is varied by varying the amplitude of the reference or sine wave. These switching pulses are given to four switches of the inverter. The rms output of the inverter is varied by varying modulation index. The harmonic profile of output voltage of the inverter is varied by changing the carrier frequency. Simulation is carried out using MATLAB Simulink, the hardware results and simulation results are compared.

KEYWORDS: FPGA, pulse width modulation, total harmonic distortion, speed control

I. INTRODUCTION

In present years, microcontrollers, Digital Signal Processors (DSPs), DSP IC been widely used implementing control motor algorithms in industry. But it has some disadvantages like, long development period and poor software portability and re-usability. Any changes in the program, imposed in the introduction to the need of good performance or new features require a large change to the project, to fit with the new system. To satisfy these demands a FPGA based hardware implementation technology is used. For three phase induction motor speed control, AC motor drives Pulse Width Modulation (PWM) inverters used in drive applications. Both the magnitude and frequency of the applied voltage to a motor can be controlled by PWM inverters.

The current control loop and PWM are done by analog control, that have fast dynamic advantage, but disadvantage like inflexibility and complexity in the circuit design, difficulty in circuit modification and limited functions. The research on DSP processors for digital current control and digital PWM control, owing its features like flexibility in adaption and software modification to other applications. But high sampling rate is needed to achieve high bandwidth performance. Most of the resources which are computational controllers are used in generation of execution of current control loop algorithms and PWM gating pulses, and time left in control loops and implementing other functions is limited. It can be done by another DSP processor for additional functions, but that increases the size and also complicates design considerably of the system. Hence, we noticed a requirement, shifting more advanced technologies like FPGA.

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II. BLOCK DIAGRAM

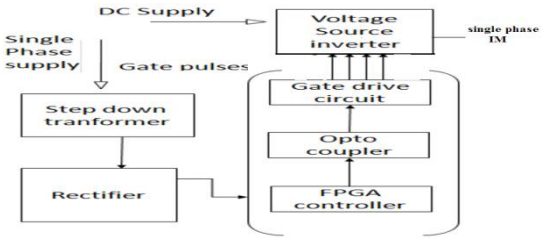

Fig1. Block Diagram

A PWM based VSI is used to convert the DC link voltage to the required AC voltages and frequency. The PWM inverter has four MOSFET switches that are controlled in order to generate an AC output from the DC input. In the present scheme, the SPWM pulses are generated using a software program coded with VHDL and downloaded in FPGA kit to produce gate signals for inverter MOSFET switches. This signal coming from the FPGA controller can't feed directly to the MOSFET gate pin due to the weakness of its voltage (3.3V). The voltage shifting from 3.3V to 12V requires a gate driver circuit. The basic block diagram is shown in Fig. 1The variation in the duty cycle and the number of SPWM pulses determines the amplitude and frequency of the inverter. This can be achieved by varying either the amplitude or frequency of the carrier signal (triangular wave). A model for the controller was designed using VHDL.

III. DESIGN SPECIFICATION

- Output Voltage : Single-phase 24VAC RMS
- Output Frequency : 50Hz
- Output Power Range : <500Watts
- Switching Frequency : Variable frequency, Variable duty cycle
- Controllers : FPGA kit

III. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

Logic circuitry of FPGA consist of arrays of gate and reconfigurable matrix block. The application of software and implementation of hardware is creates when the blocks configured. To process the logic it uses logic of particular hardware processing unlike other OS. Other process need not to be compete as it ids parallel in nature. because of this if there is more loops are logically controlled and performing it doesn't affects the output performance. the FPGA are allows their internal circuit to be reconfigured and hence the control circuit performance increases.

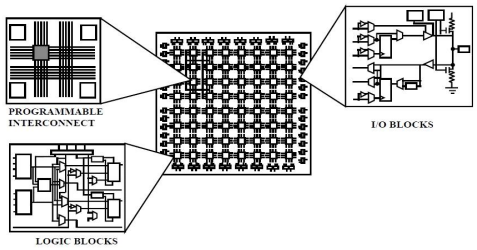

Fig 2. FPGA internal structure

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IV.PULSE WIDTH MODULATION (PWM)

Pulse-width modulation (PWM), or pulse-duration modulation (PDM), is a modulation technique that controls the width of the pulse, formally the pulse duration, based on modulator signal information. Although this modulation technique can be used to encode information for transmission, its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors.

The average value of voltage (and current) fed to the load is controlled by turning the switch between supply and load on and off at a fast pace. The longer the switch is on compared to the off periods, the higher the power supplied to the load.The PWM switching frequency has to be much higher than what would affect the load (the device that uses the power), which is to say that the resultant waveform perceived by the load must be as smooth as possible. Typically switching has to be done several times a minute in an electric stove, 120 Hz in a lamp dimmer, from few kilohertz (kHz) to tens of kHz for a motor drive and well into the tens or hundreds of kHz in audio amplifiers and computer power supplies.

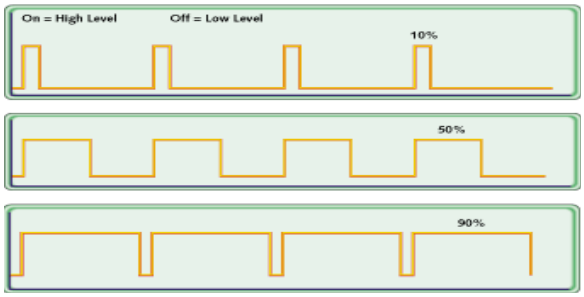

Fig 4PWM signals of varying duty cycles

V. SPWM INVERTER

In SPWM inverter the output voltage is gating by comparing the reference signal and carrier signal at the desired frequency as shown in figure 5. During first half cycle the output voltage is having positive value when reference signal having more amplitude then carrier signal. In the another half cycle the output voltage is having negative value when reference signal having less amplitude then carrier signal. The control frequency depends on pulse per half cycle and the output frequency depends on reference frequency. The basic operation circuit of single phase SPWM inverter is as shown in figure 6.

- S1 is on when Vr>Vc
- S2 is on when -Vr<Vc
- S1 is on when -Vr>Vc
- S2 is on when Vr<Vc

As shown above, if we use switching scheme then we can generate high frequency signal and harmonic free output voltage control. Hence we have the controllable output voltage and smooth speed control of single phase AC Motor.

Single phase inverter with R-load

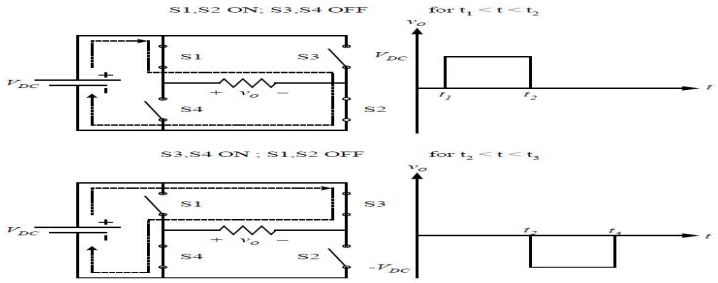

Fig.5Operation of single phase inverter with R-load

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Single phase inverter with RL-load

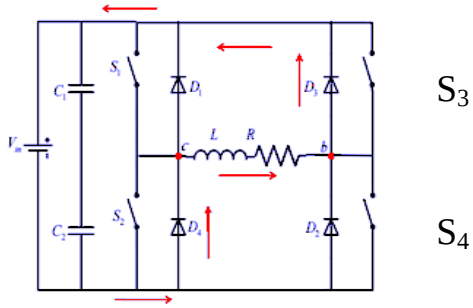

Fig.6: Operation of single phase inverter with RL load

- During positive half cycle, modulating signals are given to switch S1 and S4 is turned ON using ZCD pulses. S2 and S3 is turned off. This is shown in Fig.6.
- During negative half cycle, modulating signals are given to switch S3 and S2 is turned ON using NZCD pulses where as S1and S4 are turned off.

VI. SOFTWARE IMPLEMENTATION

This paper represents three phase induction motor drive of FPGA based controller using PWM speed control method. VHDL language is used to program the Sparten-6 FPGA. Xilinx ISE Design Suite 12.1 is used as software to write coding. Sparten 6 development board has 20MHz clock signal by default i.e. each clock cycle is 50ns. The firmware code is developed based on this frequency.

VII. SIMULATION AND RESULTS

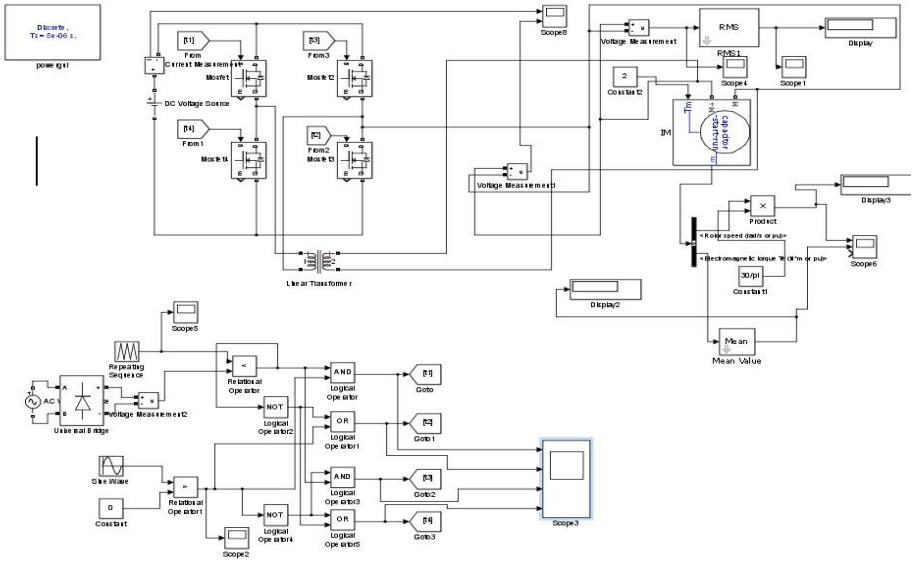

Fig 7 simulink diagrm

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For simulation MATLAB/SIMULINK is used and simulation is verified for this drive at various set speed. This drive system consists of four switches single phase inverter and single phase squirrel cage Induction Motor. Supply voltage: 1-phase, 230 V (rms), 50 Hz. 1450 rpm. The full Simulink block diagram o is shown in Fig.6. The output line voltage and current waveform of inverter is shown in Fig.9, 10 and 11, The stator currents and torque waveforms shown in Fig. 13The speed characteristics of induction motor are shown in Fig.12. It is observed that the speed increases linearly and reaches the set speed at steady state.At starting the the torque increases and reduces to a minimum value when the speed reaches the set value.

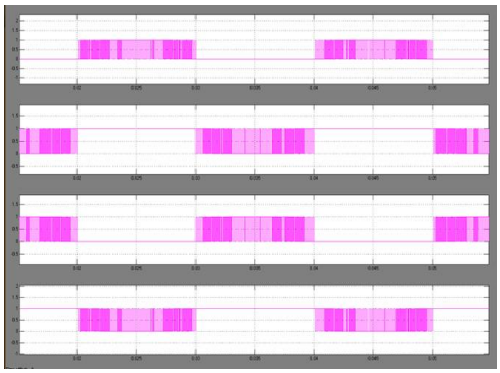

Fig.. 8 Switching pulses

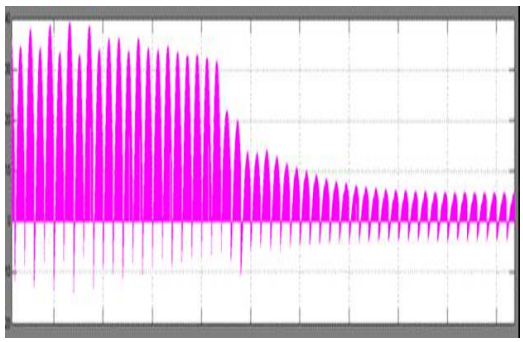

Fig.9.Input current waveform for the inverter

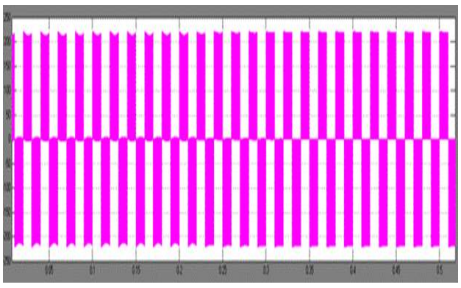

Fig.10.Output voltage waveform of the inverter.

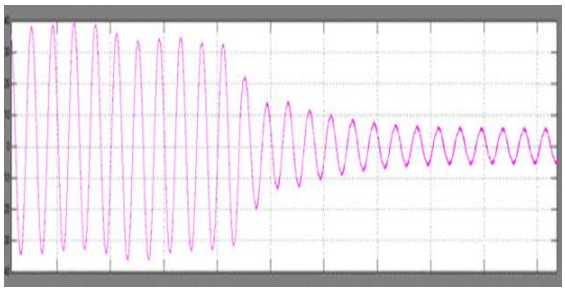

Fig.11.Output current waveform of the inverter.

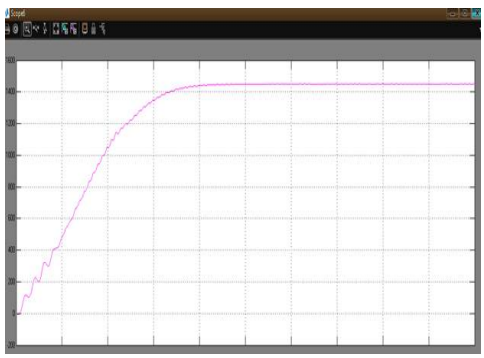

Fig.12.Speed waveform

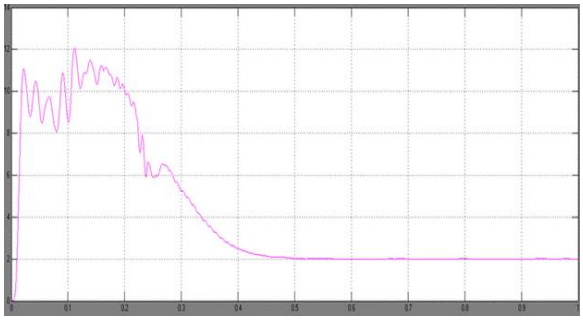

Fig.13.Torque waveform

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TABULAR REPRESENTATION OF RESULTS

Tabular results obtained by performing simulation for frequencies 1.7khz,2.1khz,2.5khz and 2.7khz is as shown in table number.1,2,.3 and 4 respectively.

MI	V	I	THD	N(rpm)
1	174.1	7.34	6.21	1453
0.8	156.3	5.67	7.31	1420
0.6	135	3.927	8.94	1153
0.5	122.4	3.363	9.91	427.6

Table no 1 .For frequency 2.1KHZ

MI	V	I	THD	N(rpm)
1	175.1	7.45	5.89	1453
0.8	156.7	5.54	6.71	1420
0.6	136.1	3.87	7.96	1153
0.5	122.4	3.795	8.68	427.7

Table no.2.For frequency 1.7KHZ

MI	V	I	THD	N(rpm)
1	174.9	7.14	5.79	1453
0.8	156.4	5.664	6.41	1420
0.6	134.7	3.82	7.37	1144
0.5	122.7	3.76	7.91	421.9

Table no.3.For frequency 2.5KHZ

MI	V	I	THD	N(rpm)
1	174.9	7.15	5.75	1453
0.8	156.5	5.301	6.29	1420
0.6	135.1	3.854	7.02	1153
0.5	122.5	3.697	7.74	427.2

Table no.4.For frequency 2.7KHZ

VIII. HARDWARE IMPLIMENTATION

In hardware implimentation the speed control is achieved by controlling the switching pulses for the inverter andharmonics are reduced selectively. IPFPE50 mosfet switches are used for inverter design, MCT2E and ICTC4424used in optocoupler circuit, ADC0804 used for converting analog signal to digital signal, op-amo LM349 used as acomparator in ZCD circuit.the FPGA has inbuilt DAC to produce triangular waveform. The results obtained from the hardware implementation is as shown below,

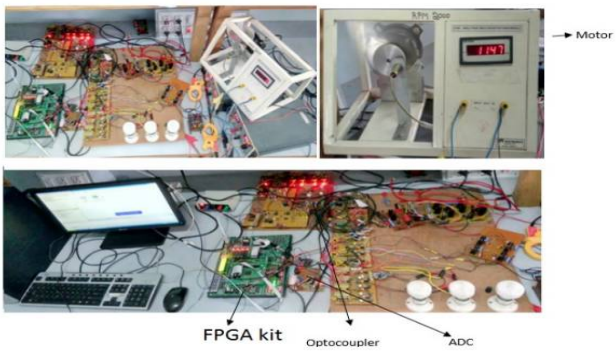

Fig .14.Hardware setup

Fig.15.THD factors up to 50th order display

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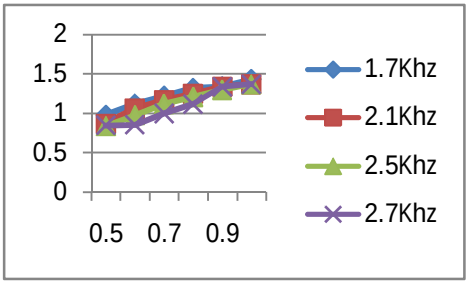

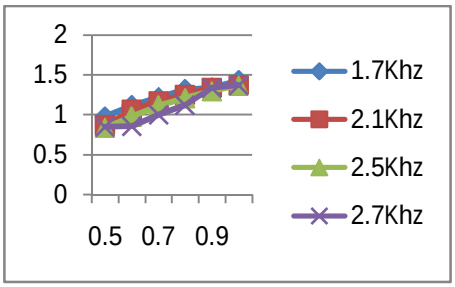

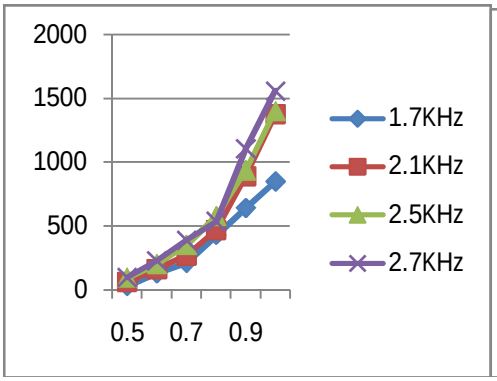

Fig.18.Speed V/S modulation index

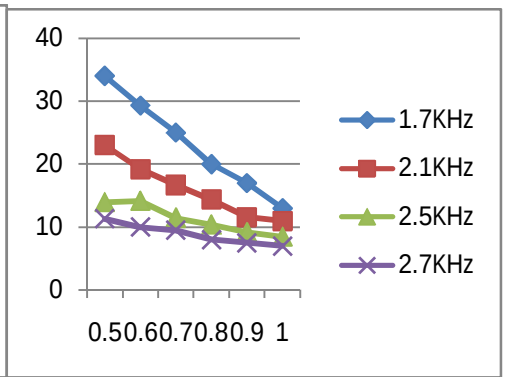

Fig.19.THD V/S modulation index

VIII. CONCLUSION

The FPGA Real time controller is used to generate PWM pulses at different frequencies by different carrier frequencies. The modulation index is varied by varying the amplitude of the reference or sine wave. These switching pulses are given to four switches of the inverter. The rms output of the inverter is varied by varying modulation index. The harmonic profile of output voltage of the inverter is varied by changing the carrier frequency. Simulation is carried out using MATLAB Simulink. The hardware results obtained is conformed with the simulation results obtained.

IX. FUTURE SCOPE

This work can be extended further for implementing SVPWM technique. In SVPWM methods, a revolving reference voltage vector is provided as voltagereference instead of three phase modulating waves. The magnitude and frequency of the fundamental component in the line side are controlled by the magnitude and frequency, respectively, of the reference vector. The highest possible peak phase fundamental is very less in sine triangle PWM when compared with space vector PWM.Total harmonic distortion (THD) can be reduced in fundamental component of voltage using SVPWM technique compared to sinusoidal PWM.

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