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A Photovoltaic Based Dual Output SEPIC-Cuk Converter for Led Driver Applications

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ABSTRACT: The proposed paper has a photovoltaic based a DC-DC converter based on combination of both SEPIC and CUK converter is proposed. In this topology, a single switch is shared by SEPIC and CUK converter and this converter is less complexity. Voltage gain ratio of both converters can be varied by controlling the duty ratio of single switch. Therefore the capacitive switch turn on losses decreases too much extent. Therefore, leakage energy is absorbed, so there is no voltage spikes across the switch. The proposed paper discussed about the principles of driver and design considerations. The prototype for supplying a 21W/30V LED module from 220Vrms/50Hz is implemented and the experimental results are verified by the theoretical analysis.

KEYWORDS: SEPIC-CUK converter , LED driver, photovoltaic(pv) based dual output, single switch

I. INTRODUCTION

Applications of light emitting diodes (LEDs) are rapidly increasing, due to their advantages such as high light efficiency, good life time , high reliability, low maintenance requirements, small sizes, being mercury-free, etc. [1]-[3]. LEDs are being used as the light sources in lighting applications, including street lighting, traffic lighting, automotive lighting, decorative lighting, and many other applications [4]-[6]. In recent times, some regulations for limiting the input current harmonics of power supplies (such as IEC 61000-3-2) have been approved, which impose the power factor requirements on AC-DC power converters [7]. To meet these requirements, designers have to be improve the low frequency harmonic contents of power supplies. In advance methods for improving the power factor, suggested applying a basic DC-DC converter (such as boost or cuk converters) for AC-DC stage [8]-[10]. This method suffer from significant twice-line-frequency voltage ripple across the output capacitor. This situation, to achieve a regulated DC output voltage, a second stage is required which results in lower efficiency because of processing the power twice. In order to increase the efficiency of two-stage PFC converters, some journalism proposed the parallel structure In this way, the majority of power is processed once and the remainder twice. Even though using the parallel structure improves the efficiency, but its complexity and cost are high. Therefore, another approach is to integrate two stages into single stage by sharing the components, especially switch(es), between two stages . This leads to single-stage structure which has less components and lower complexity. Usually, the switch current stress in a single-stage structure is high and restrictions the power level. However, due to lower complexity and cost, it is a correct choice for low power applications. A family of single-stage isolated power supplies are introduced in based on buck and boost. Also, an integrated boost-cuk converter is proposed in (11). In this converter, there are voltage spikes across the switch when it turns off. normally multiple cold cathode fluorescent lamps (CCFLs) ar necessary to offer enough backlighting for large-scale liquid show (LCD) panels This converter is enhanced by employing an extra winding on the Cuk converter to reduce the bulk capacitor voltage Reference [12] presents a single-stage converter which integrate a buck-boost converter with a buck converter. However, it uses two active switches and, therefore, its difficulty is high. An integrated buck-Cuk converter is proposed as a LED driver, in which the switch has voltage spike . Another single-stage converter is introduced in [13] which is an integrated double-buck converter. This converter suffer from zero-crossing distortion in line current and its switch also requirements a floating driverIn this paper, a new isolated single-stage single-switch (S4) converter for LED driver applications is proposed, which is composed of a single-ended primary inductor converter (SEPIC) with a Cuk converter and uses no electrolytic capacitors. Rest of the paper is managed as follows Section 2 introduces the future LED driver and presents its operating principles. Its analysis and design strategy are discussed in section 3 and experimental results of the implemented prototype are shown in section

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4. Finally, section 5 presents the conclusions. Analysis of the Integrated SEPIC-Cuk Converter as a Single-Stage Single-Switch LED Driver

`II. PROPOSED LED DRIVER

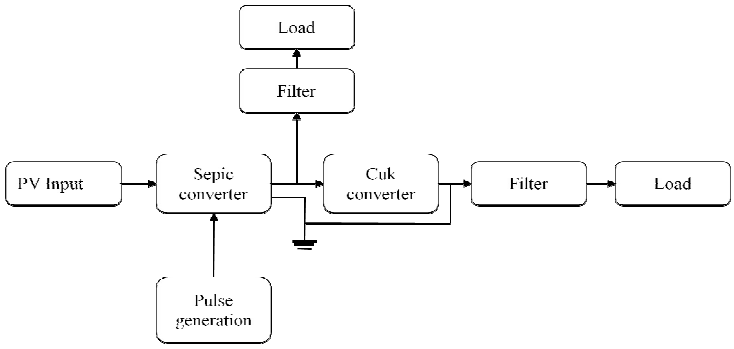

Fig.1BLOCK DIAGRAM OF PROPOSED LED DRIVER

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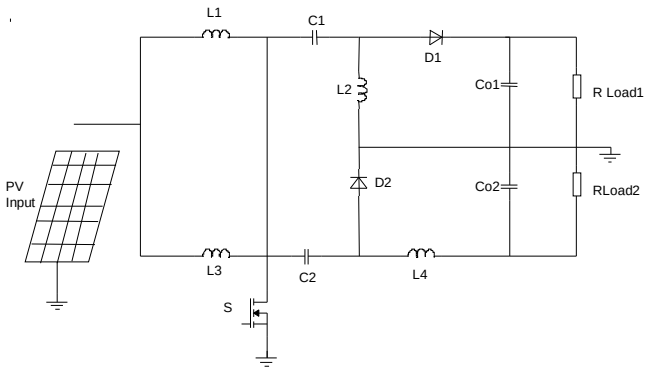

Fig.1 POWER CIRCUIT DIAGRAM OF PROPOSED LED DRIVER

Fig. 2 shows the circuit diagram of the proposed LED driver. The proposed driver is a SEPIC converter integrated with a Cuk converter (DC-DC cell), both operating in discontinuous conduction mode (DCM). The elements of the SEPIC converter include Lin, L, D1, C, and CB; and the Cuk converter consists of a transformer T, two diodes D2 and Do, and an output capacitor Co. Also, these two converters share the same switch S. CB is the output capacitor, so it acts as the bulk capacitor of the single-stage structure. In the proposed driver, The operation of input stage in DCM. As a result, the input current is discontinuous and an extra LC filter is needed to filter out the high frequency harmonics. For convenient explanation of the proposed driver operation, According to this figure, the input LC filter is omitted, and the AC input source and the bridge diodes are substituted by a rectified sinusoidal voltage source and a series diode Dr. Also, the transformer T is modeled by a magnetizing inductance Lm, a leakage inductance Llk, and. The proposed LED driver has six operating modes during one switching cycle in steady state condition. It is assumed that all semiconductor devices are ideal. Also, the capacitors C, CB, and Co are large sufficient that their voltages are constant, approximately. The switching frequency fs is much larger than line frequency fl, so the input voltage is constant through each switching period Ts. The equivalent circuit diagrams and main waveforms of the proposed driver through a switching period are illustrate in Fig. 3 , respectively. Before mode 1, it is assumed that all semiconductor devices are off and the output capacitor provides the load DC–DC converters are generally known that can increase or decrease the magnitude of the dc voltage and/or invert its polarity. This is able by the pulse width modulation (PWM) technique, typically to a constant frequency. Switching dc–dc converters are main power electronics systems commonly used in a

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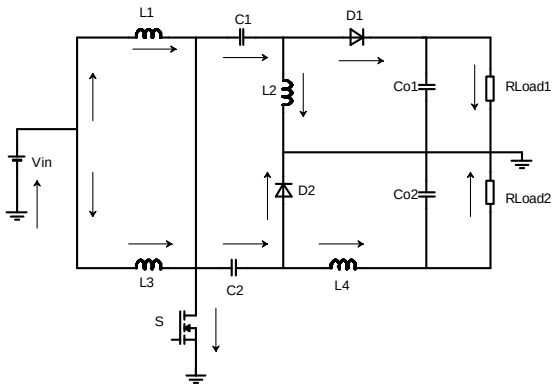
huge applications variety. Several conventional single inductor dc–dc converters, such as buck, boost, canonical switching cell, and buck–boost single inductor converters, and well-known two-inductor topologies, Cuk, SEPIC, and Zeta converters have been studied from different viewpoints (voltage gain, operating principle, voltage and current stress, and efficiency) for years The combination of these fundamental converters, such as boost–buck–cascaded converter and buck–boost–cascaded converter (two-switch topologies), and buck–boost–zeta converter, SEPIC–boost converter, zeta– flyback converter], and SEPIC-Cuk converter have also describe in the literature. The single-ended primary inductance converter (SEPIC) can also moreover increase or decrease the Voltage magnitude. However, it does not invert the polarity. The change ratio is M(D) = D/(1 – D). If SEPIC and Cuk configurations are compared, it is observed that have identical front end. Both converters have the same voltage conversion ratio with opposite polarities. Hence, it is likely to join the two structures to build a bipolar-type converter, as it is shown in Fig.2. As can be seen, the two combined structures divide a common ground indication switch and an equivalent inductor at the input. The Cuk converter contain inductors in series with the converter input and output ports. The switch network alternately connect a capacitor to the input and output inductors. The change ratio M(D) is identical to that of the buck-boost converter. Hence, this converter also inverts the voltage polarity, whilst either increasing or decreasing the voltage magnitude.The main benefit of the future configuration is that it allows completion bipolar dc link with only one controllable switch, which simplifies the implementation of control strategies since it is not necessary synchronization of various switches. Moreover, control terminal is connected to ground which simplifies the implementation of the gate drive.

Mode 1:



This mode begins when the switch S turns on. The voltages Vin rect, applied to the inductors L1, L3, . Therefore, L1, L2, increase linearly from zero. Even increment of the currents through the inductors ensures zero current switching (ZCS) turn-on condition of the switch S and diode D2. During this mode, the diodes D1 and D2 are reverse biased. Time duration of this mode is equal to DTs where D is the duty cycle of the switch. This mode ends when the switch S turns off.

Mode 2:

The beginning of this mode, the switch S turns off and the diodes D1 and D2 start conducting. By conduction of D1, voltage across the switch is clamped to C01. The voltage Vo is applied to the inductor Llk inversely and its current decreases until reaches zero. In this way, the leakage energy is absorbed and voltage spikes across the switch are eliminated. The time duration of this mode is too short when switch is turn off

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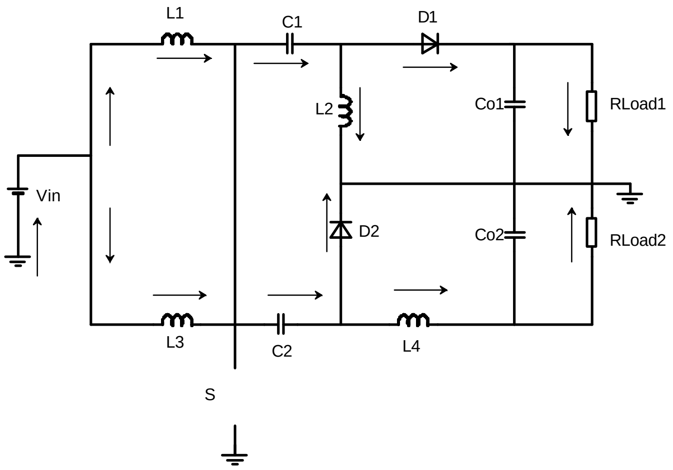

III. ANALYSIS AND DESIGN CONSIDERATIONS OF THE PROPOSED LED DRIVER

In this section, the detailed analysis of the proposed LED driver along with design guidelines is presented. It is assumed that the line voltage is a sinusoidal waveform given as

$$V_{in}(t) = V_m \sin \omega_l t \ where \ w_l = 2\pi f_l$$

According to DCM operation of the input inductor Lin, the current I Lin consists of triangular current pulse which are filtered by the input LC filter. Therefore, the line current can be obtained by averaging ILin on each switching period Ts

$$I_{inave}(t) = \frac{1}{T_s}\frac{1}{2}\left(DT_s + t_{flin}\right)I_{lin\,peak} \cdots (1)$$

The peak value of ILin occur at the ending of mode 1 which is equal to

$$I_{lin\ peak} = \frac{V_m DT_s}{L_{in}}\left|\sin \omega_l t\right| \ldots (2)$$

The fall-time of ILin, i.e., the time required for IL in to reach zero from its peak value can be calculated as

$$t_{f\,l_{in}} = \frac{V_m\left|\sin\omega_l t\right|}{V_B + V_C - V_m\left|\sin\omega_l t\right|} DT_S \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3)$$

By substituting (2) and (3) into (1), the line current is obtained as

$$I_{in\ ave}(t) = \frac{V_m D^2 T_s}{2l_{in}} \frac{V_B + V_C}{V_B + V_C - V_m}\left|\sin \omega_l t\right| \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

According to (4), input current waveform is depended on the value of VB+VC such that if VB+VC is much larger than Vm, the input current will be approximately sinusoidal. It is important to investigate the effect of VB+VC on the input current waveform and consequently on the power factor. Sincethe first term in (4) is a constant, it can be ignored in power factor calculation. Thus, the current i is defined as

$$i(t) = \frac{V_B + V_C}{V_B + V - V_m\left|\sin\omega_l t\right|}\sin\omega_l t \ldots\ldots\ldots\ldots\ldots(5)$$

The power factor can be calculated using

$$PF = \frac{I_{1rms}}{I_{rms}}\cos\Phi \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(6)$$

According to the Fourier series of i, its first harmonic can be expressed as

$$i(t) = a_1 \cos\omega_l t + b_1 \sin\omega_l t \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(7)$$

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an odd function of t, so the coefficient a1 is zero. Consequently, i1 is in-phase with Vin, and $\varphi\varphi$ is also zero. However, the coefficient b1 is obtained as

$$b_1 = \frac{2}{T_1}\int_0^{T_1} i(t)\sin\omega_l t\,dt \quad \ldots\ldots\ldots\ldots (8)$$

By substituting i from (5) into (7), b1 can be written as

$$b_1 = \frac{1}{\pi}\int_0^{2\pi} \frac{(V_B + V_C)\sin^2\theta}{V_B + V_C - V_m|\sin\theta|}d\theta \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

Equation (8) can be simplified by defining the integral expression as a parameter such as k.

$$b_1 = \frac{2k}{\pi} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

on the way to (9), the limit k is a function of Vm and VB+VC. Therefore, this limit can be numerically planned in terms of different values of VB+VC for a constant value of Vm. Then obtain numerically using (5) to (7) and (11). The limit k and power factor are inside Fig. 5 in terms of different values of VB+VC for Vm equal to 310V. As it can be observed, the power factor approaches to unity for large values of VB+VC. So, in order to achieve high power factor, VB+VC must be selected as large as possible. On the other hand, this results in high voltage stress of the switch. Thus, there is a trade-off between the power factor and switch voltage stress,

$$t_{fL} = \frac{V_C}{V_B}DT_s \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (10)$$

The following expression is obtained using (3) and (10), and setting tf Lin smaller than tf L

$$\frac{V_m|\sin\omega_l t|}{V_B + V_C - V_m|\sin\omega_l t|} \left\langle \frac{V_C}{V_B} \right.$$

The definition of input average power is

$$P_{in} = \frac{2}{T_1}\int_0^{\frac{T_1}{2}} V_{in}(t) I_{in\,ave}(t)dt \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (11)$$

Then

$$L_{in} = \frac{KD^2V_m^2}{2\pi f_s p_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

Therefore, the input inductor can be designed using (12) and choosing proper values for fs and D.
At output stage of the proposed driver, power is delivered to load through a CUK converter. So, the output power can be expressed as

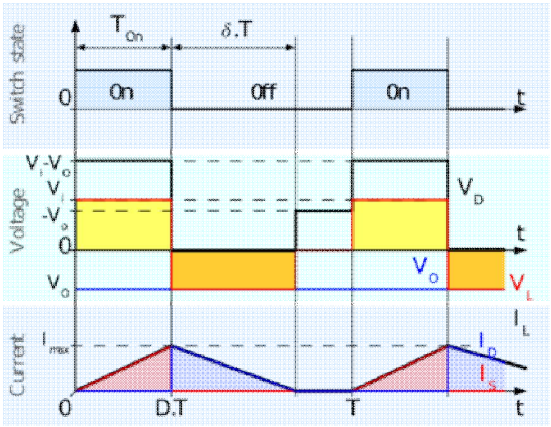

Fig. 3. Main waveforms of the proposed LED driver during a switching period
peak value of is

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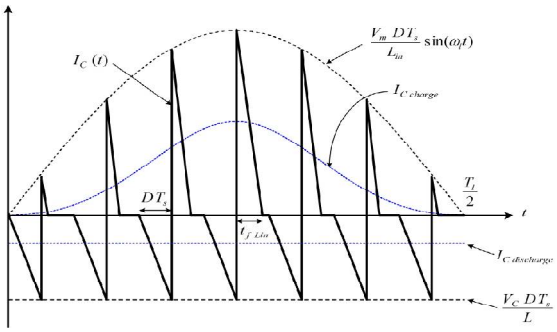

Fig. 4. Current waveform through the capacitor C during the half-period of line voltage.

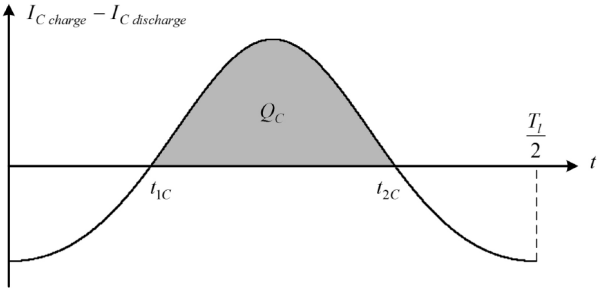

Fig. 5. Average current through the capacitor C during the half-period of line voltage.

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a laboratory prototype to supply a 21W/30V LED module from 220Vrms/50Hz AC mains is designed and implemented. The LED module has been composed of series connection of nine 3.3V white LEDs. The switching frequency of 50kHz is selected. According to (12), (16), (27) inductances and capacitances of the proposed driver are proportional to the square value of D. Thus, it is essential to choose D as small as possible in order to reduce the size of passive elements. Consequently, the operating duty cycle is selected equal to 0.1.

TABLE I
KEY PARAMETERS OF THE IMPLEMENTED PROTOTYPE

Parameter	value
output power (po)	21w
Output voltage (vo)	30v
Output current (Io)	700mA
Input voltage (vin)	220Vrms
Switching frequency (fs)	50KHZ
Operating duty cycle (D)	0.1
Switch S	2SK2611
Bridge diodes Dr	US1M
Diodes D1 and D2	UF5408
Diode	MUR460
Inductor Lf	2 mH
Inductor lin	430 µH
Inductor L	870 µH
Capacitor Cf	220 nF
Capacitor Co	2×4.7µF/100v

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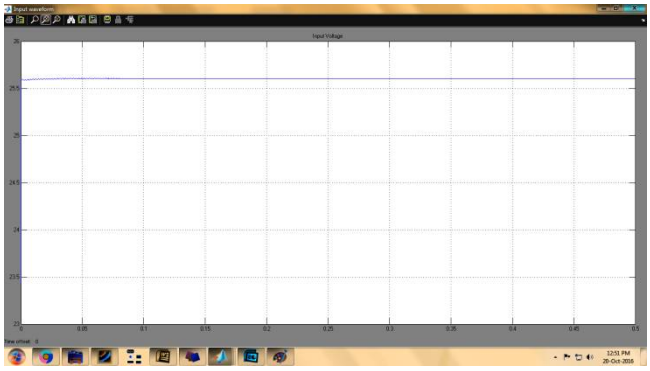
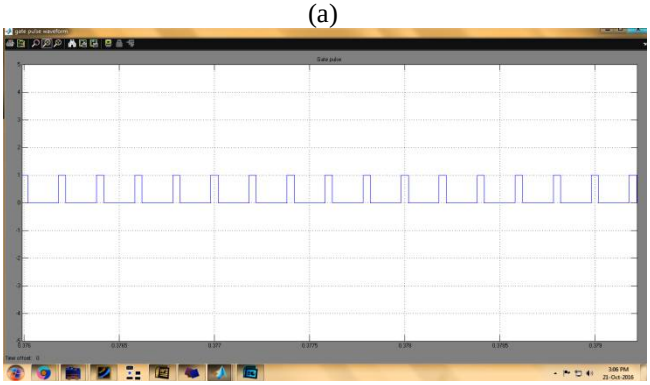
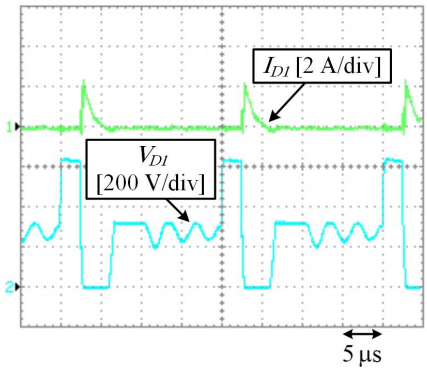
implemented prototype has an efficiency of 91.6% under full-load and 220 Vrms line voltage condition. Loss breakdown for the implemented prototype under this condition is presented in table 2. As it can be observed, major parts of the driver losses are associated with the power switch and output diode. Thus, improvement of these two components can improve the driver efficiency.



(a)



(b)



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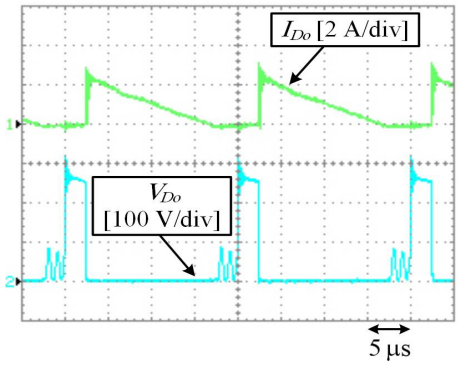

(d)

Fig. 6. Experimental waveforms of the implemented prototype (a) Input current and voltage waveforms.
(b) Current and voltage waveforms of the switch S.
(c) Current and voltage waveforms of the diode D1.
(d) Current and voltage waveforms of the diode Do.

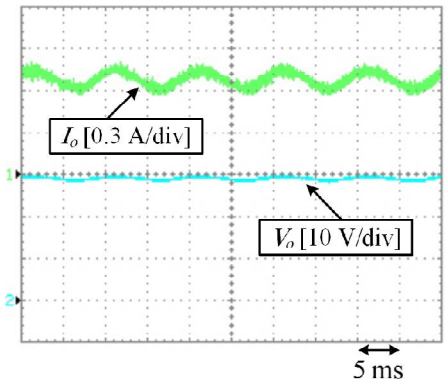

Fig7.Output current and voltage waveforms.

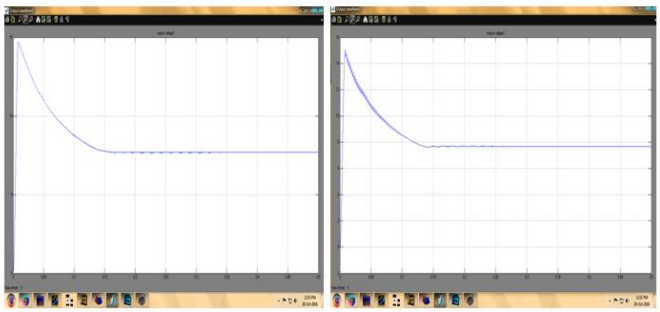

Fig8.Multiple output waveforms

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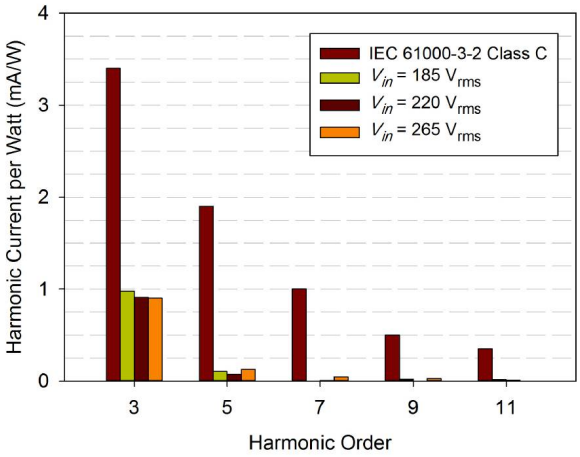

Fig9.Measured input current harmonics under three different line voltages

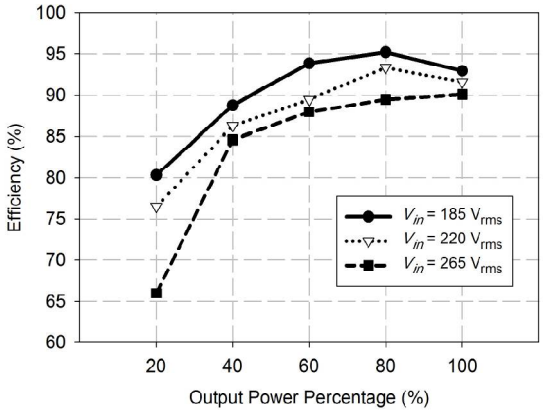

Fig.10. Efficiency of the implemented prototype under different load conditions for three line voltage

TABLE II
MEASURED COMPONENT LOSSES IN THE IMPLEMENTED PROTOTYPE

Component	P loss(mw)
Switch	760
Bridge diodes Dr	4×50
Diode D1	100
Diode D2	100
Inductor Lf	25
Inductor Lin	15
Inductor L	**20**

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V. CONCLUSION

A converter for dc applications has been presented. This converter consist the combination of SEPIC and Cuk topologies (SEPIC-Cuk). Both converters have the same voltage conversion ratio. Therefore, it is possible to combine the two topologies to build a converter. The two combined structures share a common ground reference switch, and an equivalent inductor at the input. The main advantage of the proposed configuration is that it allows implementation dc link with only one controllable switch, which simplifies the implementation of control strategies. Highlighting three aspects of the converter: simple structure since it uses an only switch and fewer passive elements, a driver circuit more simple due to there is only one switch to be controlled and it does not require isolation, and control circuit is simpler since they can be regulated dc voltages with an only controller. This means that switches with lower voltage ratings and lower on-resistances can be used. These features make the proposed driver efficiency improve.

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