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Highly Reliable Frequency Multiplier with DLL-Based Clock Generator for System-On-Chip

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ABSTRACT: High-speed, low-power, fully operational and reliable frequency multiplier is proposed for a delay locked loop based clock generator to generate a multiplied clock with a high frequency and maximum frequency range. The proposed edge combiner efficient achieves-speed and highly reliable operation using a hierarchical structure and an overlap deselected. By applying the logical effort to the pulse generator and multiplication-ratio control logic design, the proposed frequency multiplier minimizes the delay difference between positive- and negative-edge generation paths, which causes a measurable jitter. Finally, a jitter analysis is performed to analyze and compare the performance of the proposed frequency multiplier with that of previous frequency multipliers. The proposed frequency multiplier is fabricated using a 2.5-μm technology, and has the multiplication ratios of 2^0, 2^1, 2^2, 2^3, and 2^4, and an output range of 50 MHz–3.3 GHz.

KEYWORDS: Clock generator, delay-locked loop (DLL), edge combiner, frequency multiplier..

I.INTRODUCTION

Dynamic Voltage Frequency Scaling is currently being used in nearly every System-On-Chip (SoC), because this design can be efficiently lower the dynamic power consumption of the SoCs. It detects the SOC workload and dynamically changes the supply voltage and frequency, requires a low power dc converter and a clock generator. The clock generator is generally implemented using a phase-locked loop to easily change the output clock frequency. While, PLLs have several weaknesses such as the difficulty of design, high-cost loop filters, and jitter accumulation is high. Delay-locked loops (DLLs) are a good alternator for PLLs, because they overcome the PLL drawback however, because a DLL uses a delay line instead of an oscillator, its output clock frequency is always the same as its input clock frequency. Therefore, a DLL alone cannot be used as a clock generator. Several DLL-based clock generators have been proposed to solve this problem. The DLL-based clock generator is composed of a DLL core and a frequency multiplier, and the frequency multiplier is generally divided into two blocks:

A Pulse Generator and An Edge Combiner. In case that variable frequency multiplication is required, a multiplication-ratio control circuit is added. The DLL core generates multiphase clocks using a input clock in the DLL core. The pulse generator generates the required number of pulses from the multiphase clocks according to the multiplication-ratio control signal generator, and the edge combiner generates a multiplied clock using the selected pulses. In general, the maximum multiplication ratio of the frequency multiplier is N/2 of the number of multiphase clocks. Because the frequency multiplier generates the multiplied clock by simply collecting the multiphase clocks, jitter accumulation does not occur. In addition, the frequency multiplier can easily change multiplication ratios. However, to increase the Multiplication ratio, the logic depth or output loading of the frequency multiplier must be increased. However, it severely degrades the maximum multiplied clock frequency.

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II.PROPOSED FREQUENCY

Our proposed Delay Lock Loop based clock generator is consists of a DELAY LOCK LOOP core and the proposed frequency multiplier. To enhance the lock time, which is an vital design parameter in the clock generator, a dual-edge-triggered phase-detector-based DELAY LOCK LOOP core is adjustable. Same as previous frequency multipliers, the proposed frequency multiplier is also consists of a pulse generator, multiplication ratio logic circuit controller, and an Edge Combiner. The Dual Edge Triggered, Phase-detector characterises both the raising and the falling edges of Reference CLK, Delayed CLK and output CLK, Delayed CLK, which are the duty cycle recovered clocks of Reference CLK and Output CLK using the duty-cycle maintainer.

The ***DELAY LOCK LOOP*** is locked within (300) three Hundred clock cycles in all process–voltage–temperature corners owing to the dual-edge detection characteristic, and generates 32-phase differential clocks phase 2^0 to 2^5 and phase $2^{0\text{ to}}$ 2^5. Using the 32-phase differential clocks, the pulse generator makes pulses Phase G 2^0:2^5 and Phase G $2^{0\text{ to}}$ 2^5 for positive- and negative-edge generation. The multiplication-ratio control logic selects appropriate pulses from Phase-G 0:31 and Phase-G 0:31 and generates MC-*P*,0:15 and MC-*N*,0:15 according to the multiplication ratio control signal. Finally, the high-speed and highly reliable edge combiner generates one multiplied clock *using* all the outputs of the multiplication ratio control logic. Hence the number of multiphase is $2^{0\text{ to}}$ 2^5, the maximum multiplication ratio is 16.

III. HSHR-EC

To solve the speed and the reliability issues of previous edge combiners, an HSHR-EC, which consists of a pre-combining stage, overlap canceller, and push–pull stage, as shown in Fig. 4, is proposed. The two-step edge combiner, pre-combining, and push–pull stage are used to enhance the maximum multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier. Fig. 5 shows the operation of the HSHR-EC. As the number of signals merged in the pre-combining stage (*N*PRE*)* increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of *N*PRE. It might appear that, by increasing *N*PRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; however, because the logic depth and the number of NAND and NOR gates in the pre-combing stage are equal to log2*N*PRE and 32(1–1/*N*PRE*)*, respectively, a large *N*PRE causes the pre-combining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter. Thus, *N*PRE is limited to two, which corresponds to a logic depth of one in the HSHR-EC, and thus, the pre-combining stage can be simply realized using NAND and NOR gates. As is true for the frequency multipliers the proposed frequency multiplier may suffer from pulse overlapping owing to the multiplication-ratio control logic. To prevent this, an overlap canceller is inserted between the pre-combing and the push–pull stages.

An HSHR-EC, it has a pre-combining stage, overlap canceller, and push–pull stage is proposed. The two-step edge combiner, Pre-combining, and push–pull stage are used to enhance the maximum multiplied clock frequency. The overlap canceller is used to guarantee the stable operation of the frequency multiplier. Fig. 5 shows the operation of the HSHR-EC. As the number of signals merged in the pre-combining stage (*N*PRE*)* increases, the number of PU-Ps and PD-Ns required in the push–pull stage are reduced by a factor of *N*PRE. It might appear that, by increasing *N*PRE, the maximum multiplied clock frequency of the HSHR-EC can be enhanced; Because the logic depth and the number of NAND and NOR gates in the pre-combing stage are equal to log2-*N*-PRE and 32, respectively, a large *N*PRE causes the pre-combining stage to be vulnerable to process variation, which in turn could cause a large deterministic jitter.

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IV.PROPOSED DIAGRAM

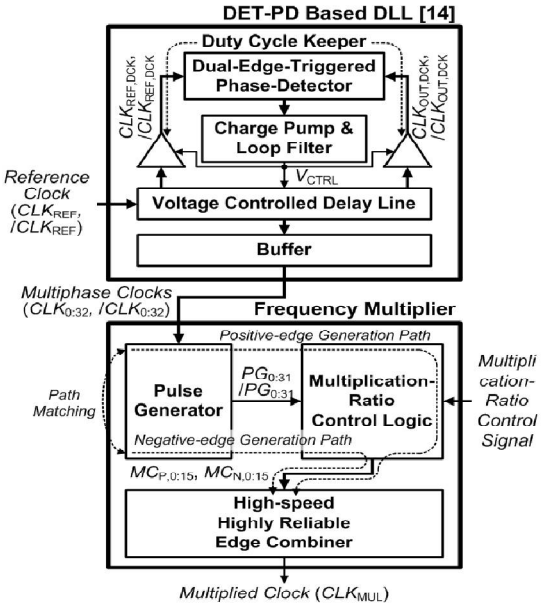

FIG:1. STRUCTURE OF THE PROPOSED CLOCK GENERATOR.

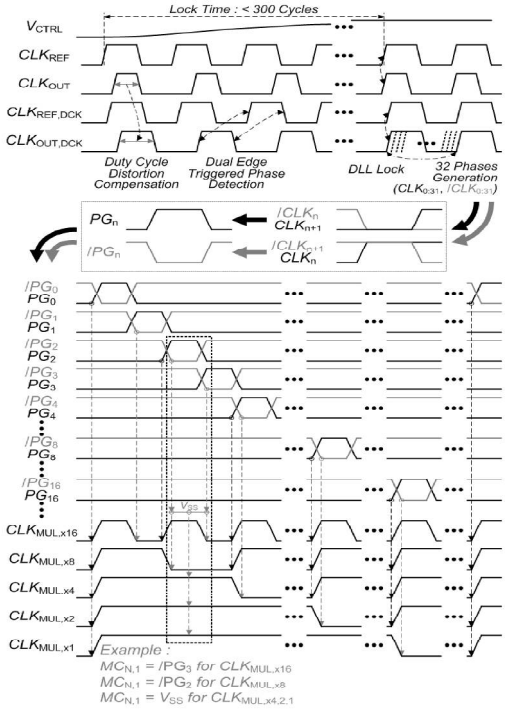

Fig:2 Operation of the proposed clock generator

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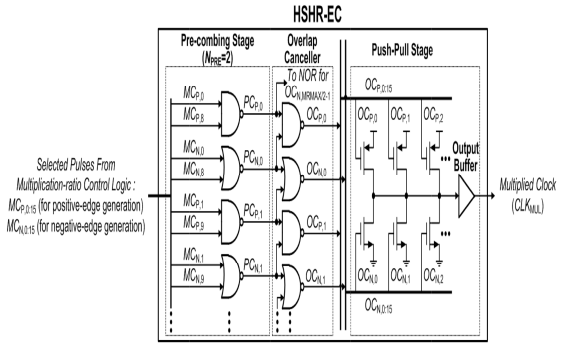

Fig:3. Structure of the proposed HSHR-EC.

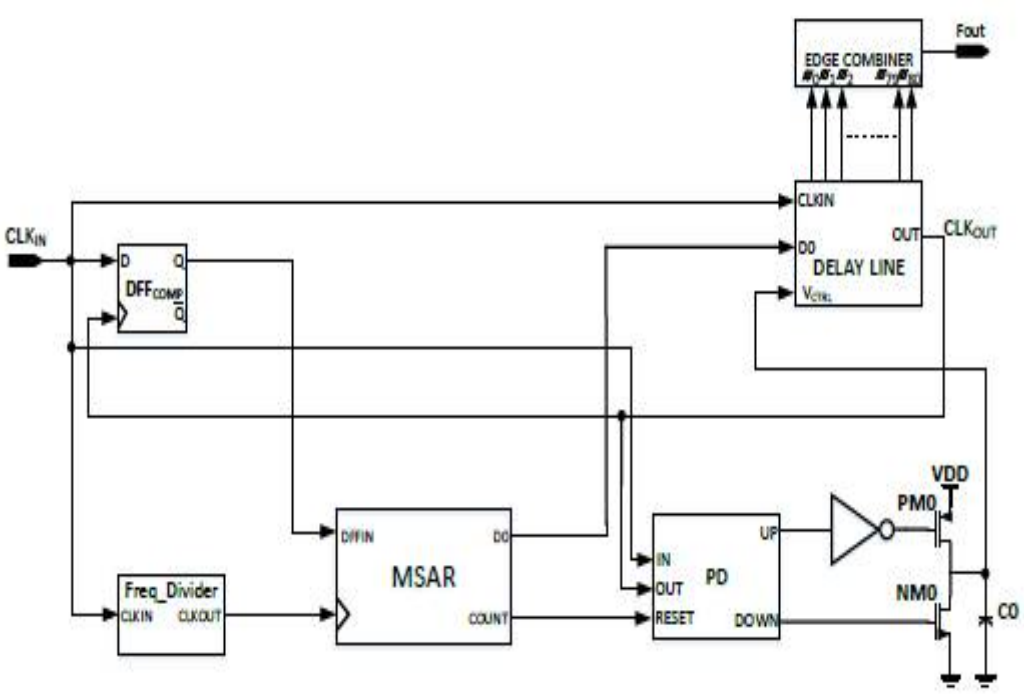

Fig:4 MODIFICATION

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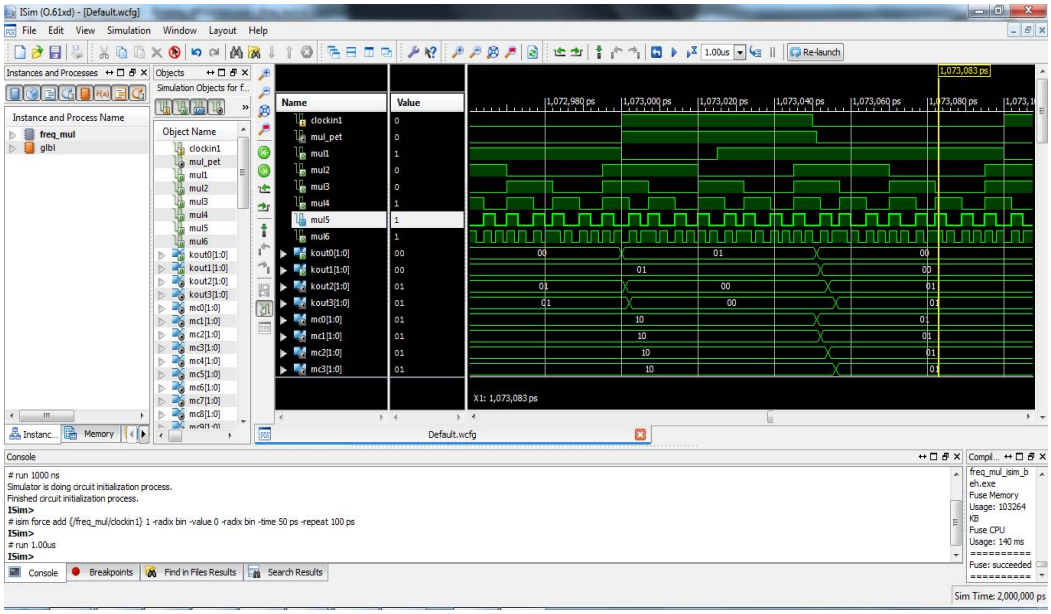
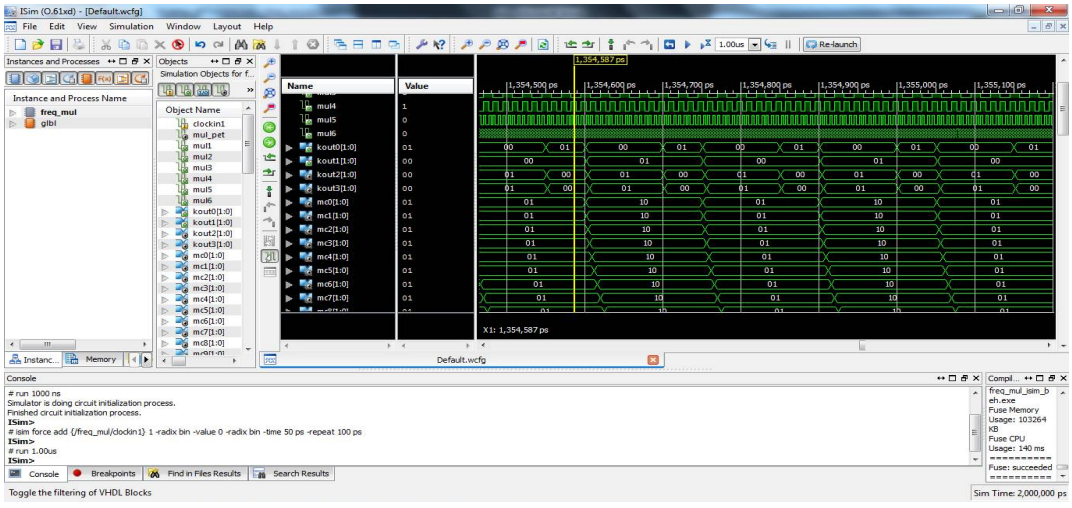
V. RESULT AND DISCUSSION

SNAPSHOT:DIGITAL DESIGN(VERILOG HDL)

SIMULATION WAVE FOR DLL FREQUENCY MULTIPIER:



DUAL EDGE TRIGGER:



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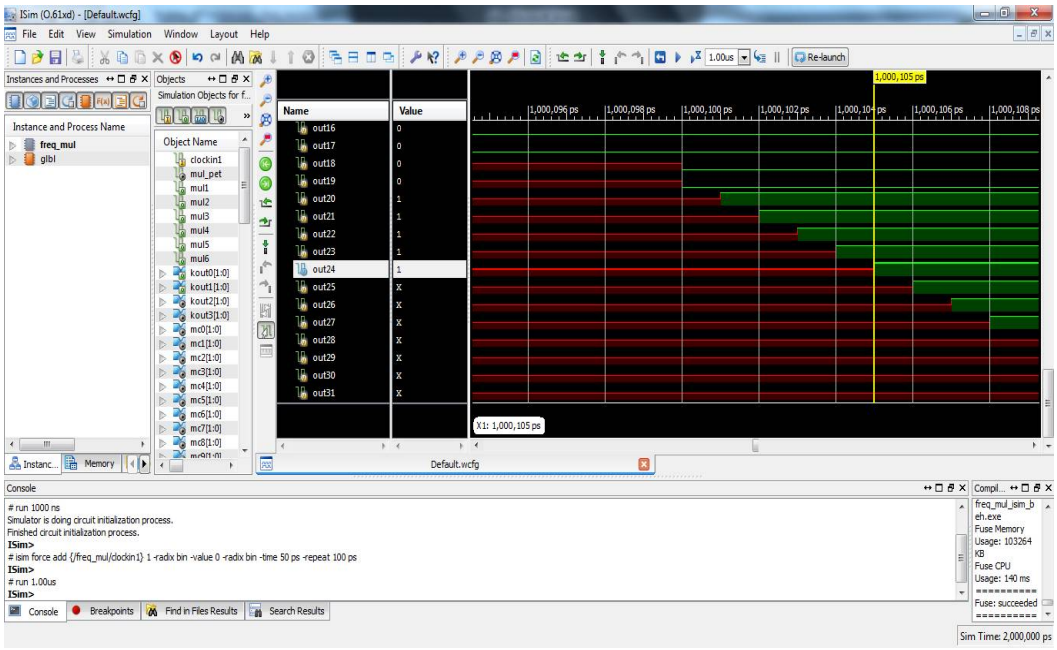
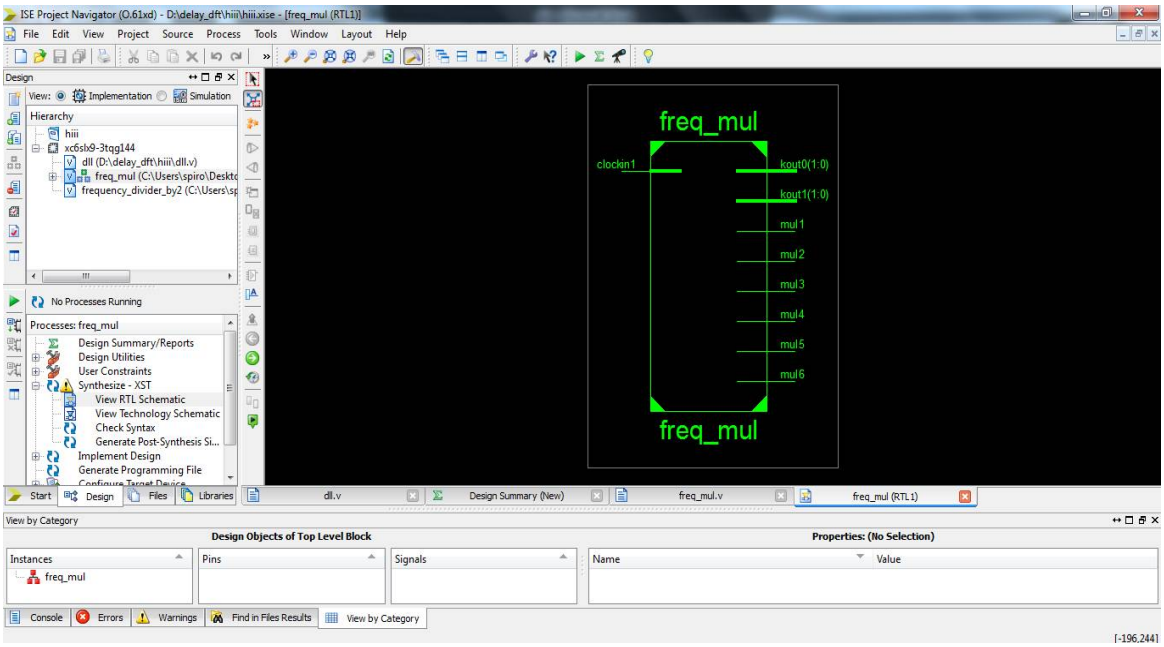
32-DIFFERENT PHASE GENERATOR:



RTL SCHEMATIC



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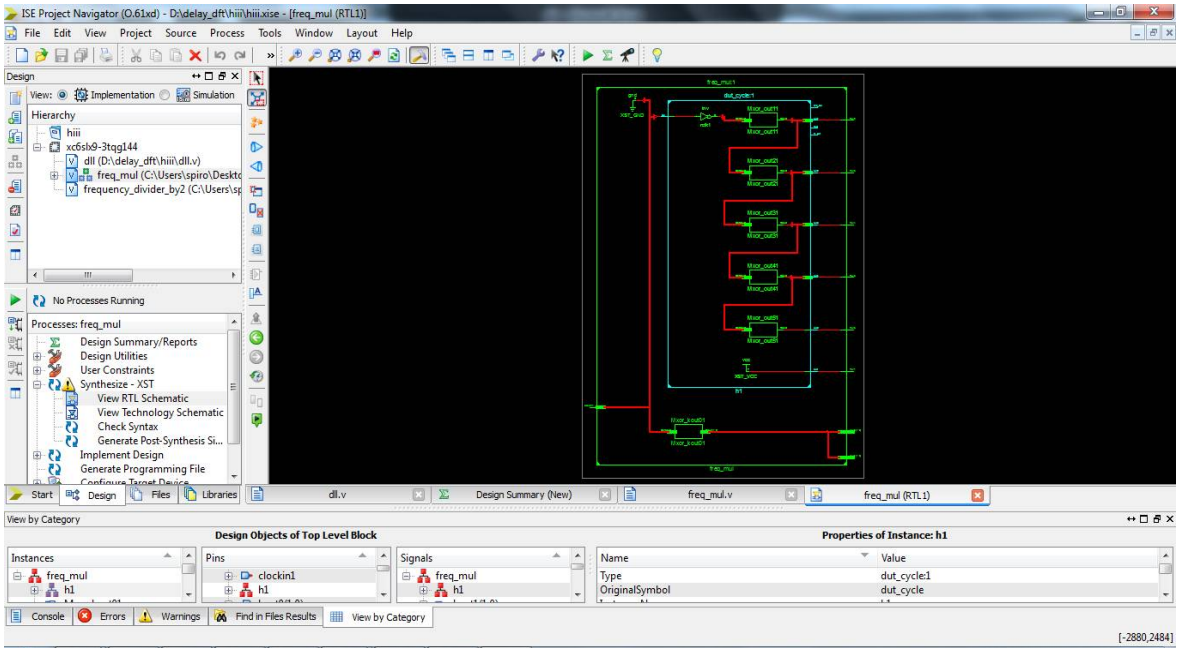
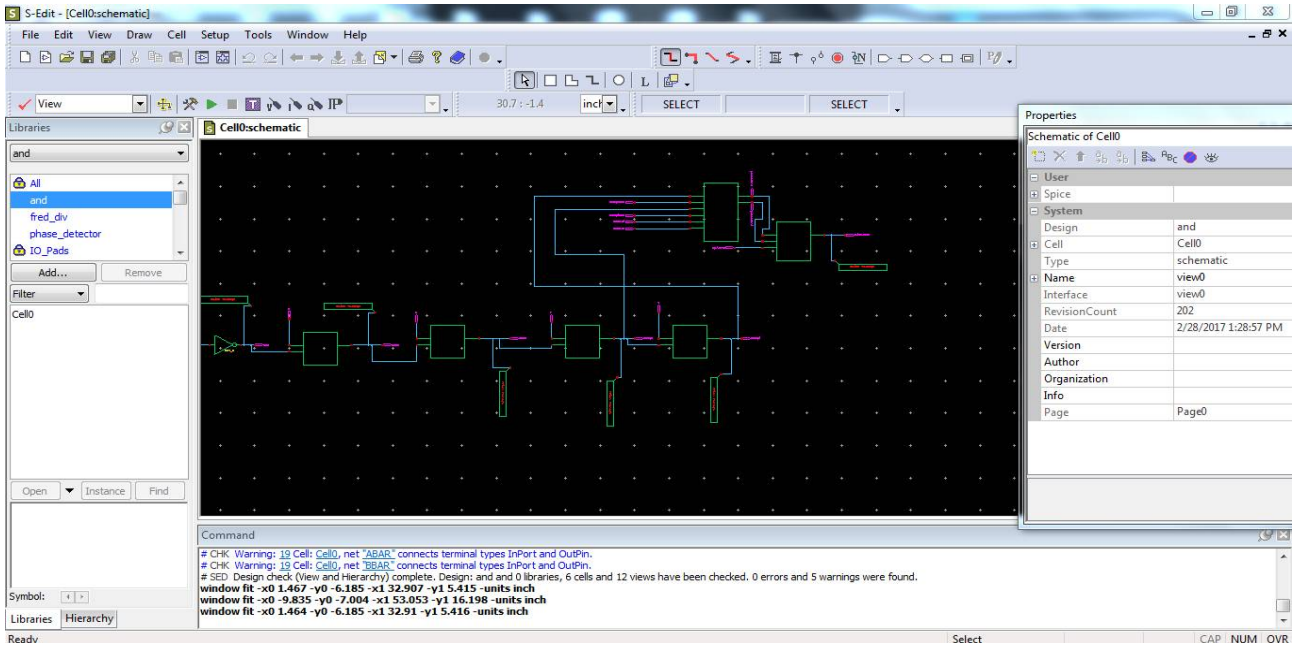
TECHNOLOGICAL VIEW



ANALOGY DESIGN :CMOS BASED DESIGN IN TANNER EDA TOOL



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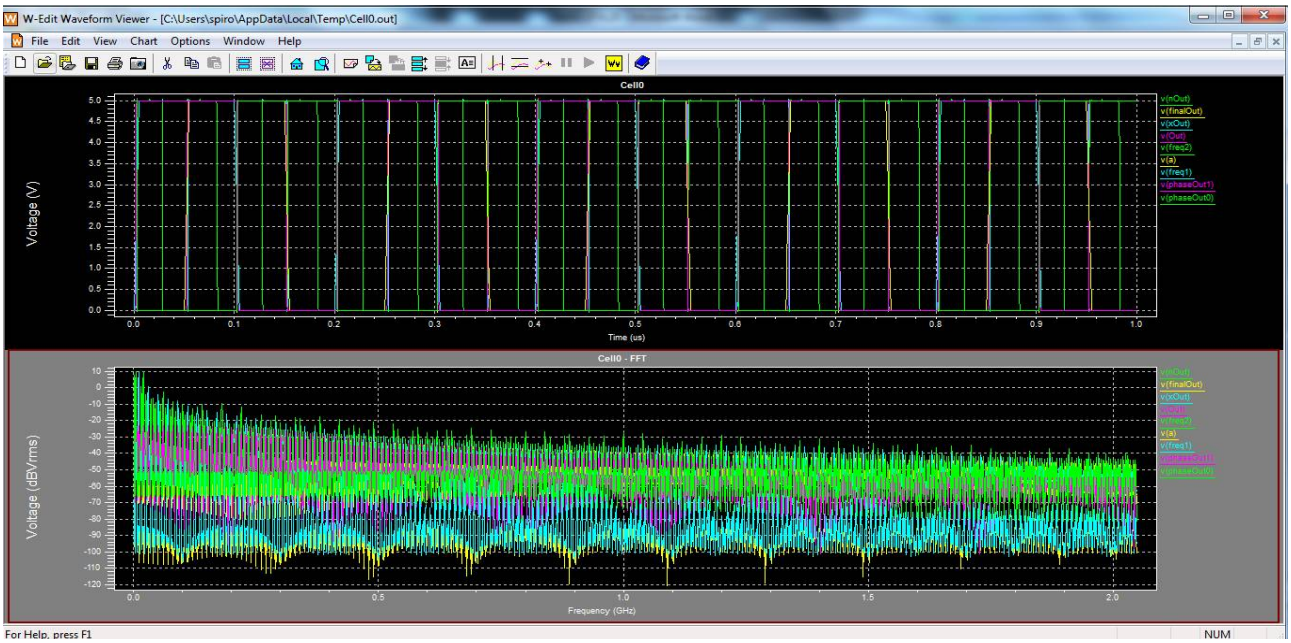
FFT ANALYSIS



POWER RESULTS

Total Power from time 0 to 1e-006

Average power consumed -> 1.349300e-002 watts

Max power 6.825094e-002 at time 4.02767e-007

Min power 1.322325e-007 at time 4.9e-007

* END NON-GRAPHICAL DATA
*

* Parsing 0.01 seconds
* Setup 0.03 seconds
* DC operating point 0.98 seconds
* Transient Analysis 2.79 seconds
* Overhead 0.80 seconds
* ----------

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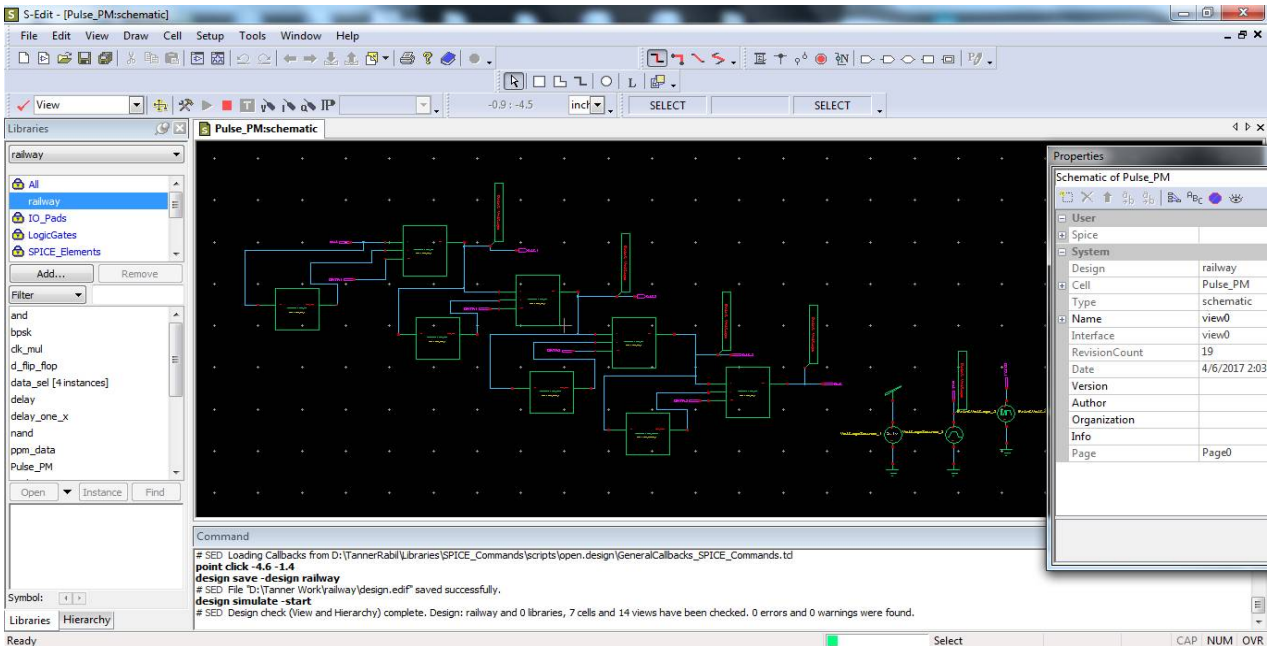
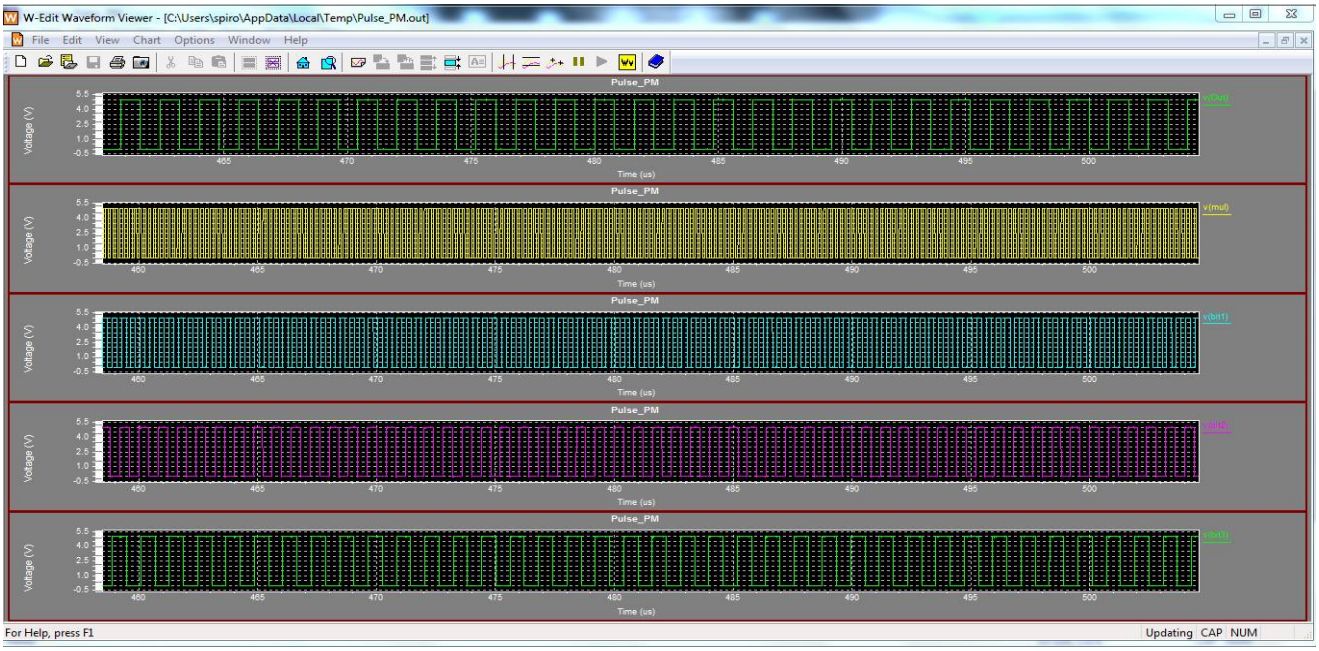
MODIFICATION



SIMULATION WAVEFORM



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POWER RESULTS
Total Power from time 0 to 0.001
Average power consumed -> 5.314303e-004 watts
Max power 9.686614e-002 at time 2.30045e-009
Min power 6.128086e-010 at time 0.00081622

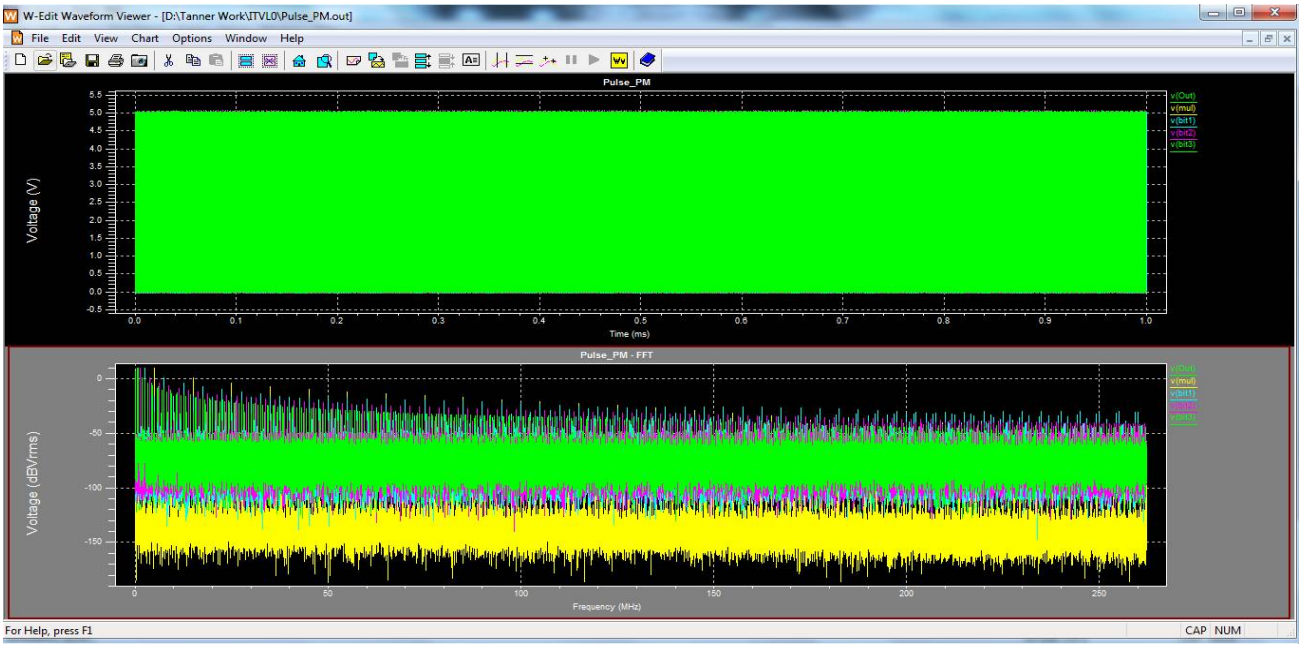
* END NON-GRAPHICAL DATA

* Parsing 0.01 seconds
* Setup 0.04 seconds
* DC operating point 0.13 seconds
* Transient Analysis 387.74 seconds
* Overhead 0.78 seconds
* ----------
* Total 388.71 seconds

* Simulation completed

* End of T-Spice output file

FFT ANALYSIS:



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PHASE NOISE:

0.0000050,-5
0.0000100,-5
0.0000150,-5
0.0000200,-5
0.0000250-5
0.0000300,-5
0.0000350,-5
0.0000400,-5
0.0000450,-5
0.0000500,-5
0.0000550,-5
0.0000600,-5
0.0000650,-5
0.0000700,-5
0.00050,-5
0.00100,-5
0.00150,-5
0.00200,-5
0.00250-5
0.00300,-5
0.00350,-5
0.00400,-5
0.00450,-5
0.00500,-5
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0.00700,-5

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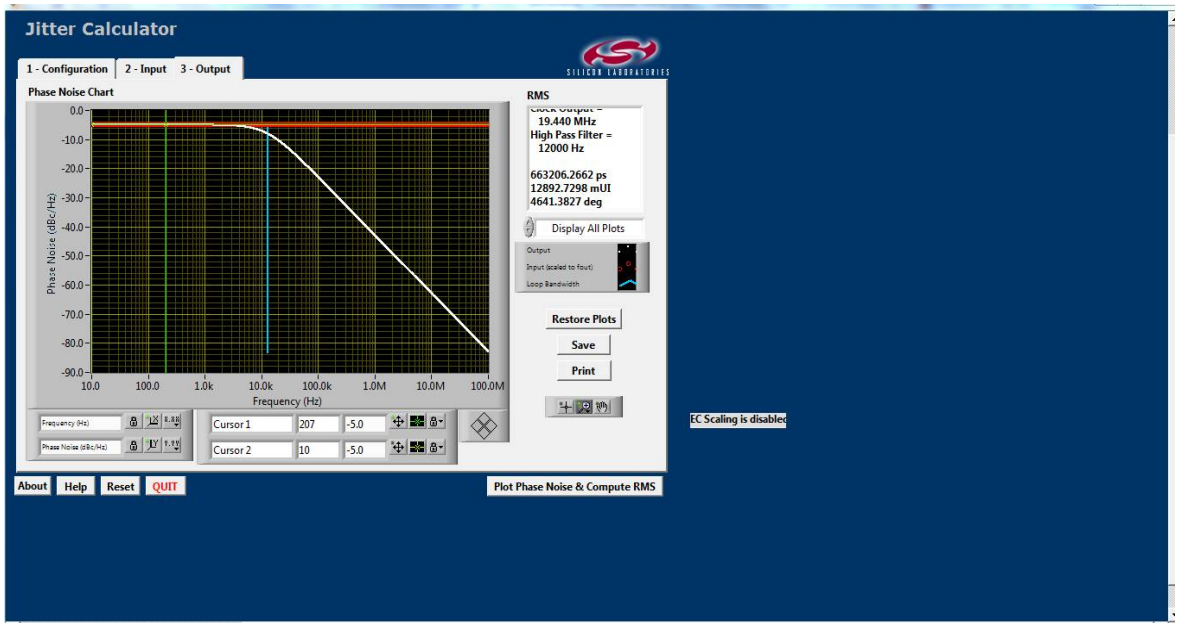

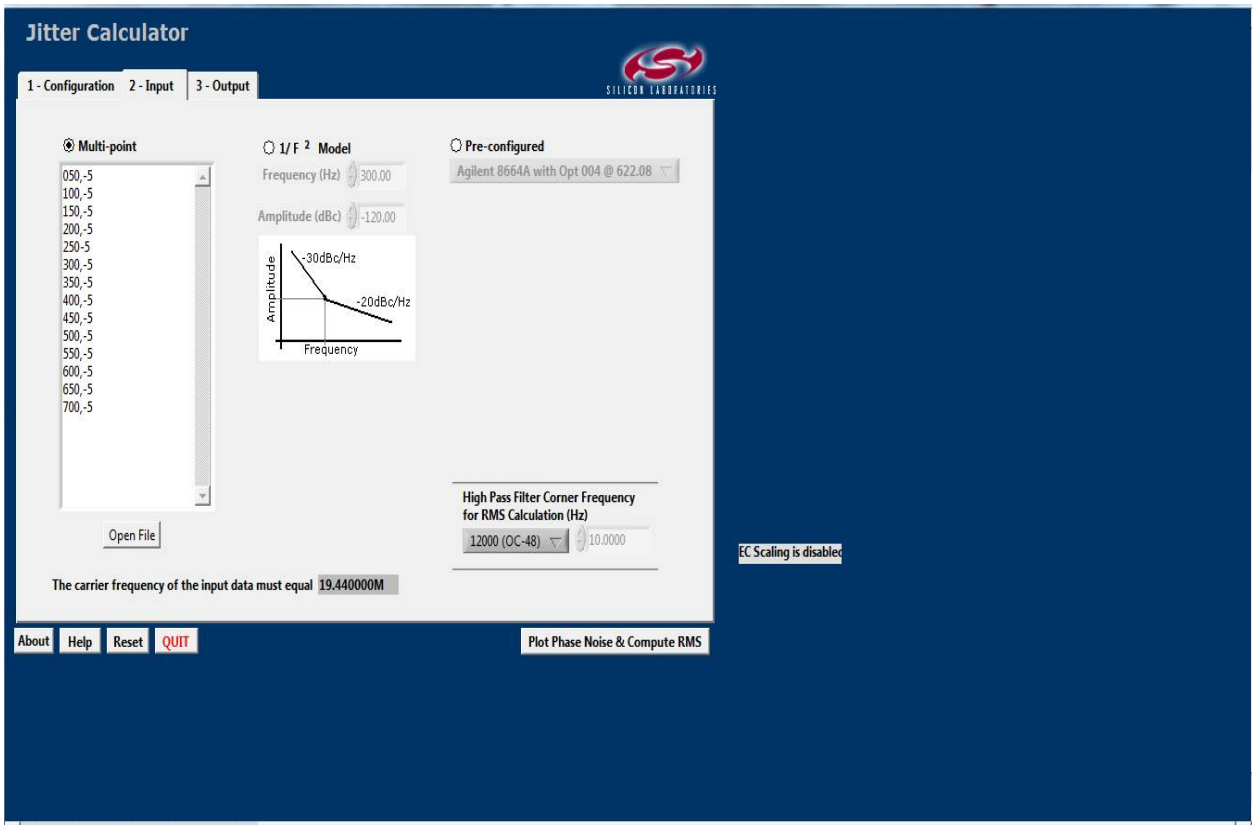

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Jitter calculation:
Clock Output =
19.440 MHz
High Pass Filter =
12000 Hz

663206.2662 ps
12892.7298 mUI
4641.3827 deg

Table I PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

PARAMETERS	EXISTING SYSTEM				PROPOSED SYSTEM
	[1]	[2]	[3]	[4]	
V_{DD}	3.3 V	1.2 V	1.8 V	1.8 V	1.2 V
Multiplication ratio	4	4	4	8	16
Power Consumption of FM	Not shown	4.8mW @2GHz	17mW @1.7GHz	6.8mW @2GHz	9.6mW @3.3GHz
Normalized Area	$0.143*10^6$	$0.281*10^5$	$0.337*10^5$	N/A	$0.037*10^6$
Jitter (rms/peak-to-peak)	1.8/13.2ps @1.3GHz	3.2/19ps @1GHz	2.6/16.8ps @1.7GHz	N/A	1.9/13.6ps @3.3GHz

VI.CONCLUSION

In this paper, a frequency multiplier for a DLL-based clock generator is proposed. The proposed HSHC-EC guarantees high-speed operation owing to its hierarchical edge-combiner structure and highly reliable operation owing to its use of an overlap canceller. The optimized pulse generator and the multiplication-ratio control logic are proposed to reduce the delay difference between positive- and negative-edge generation paths. Finally, a numerical analysis is performed to validate its performance. The frequency multiplier, which is fabricated using the 0.13-μm CMOS process technology, has the multiplication ratios of 1, 2, 4, 8, and 16, an output range of 100 MHz–3.3 GHz, and a power consumption to frequency ratio of 2.9 μW/MHz.

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BIOGRAPHY

Miss. B. Janani, B.E. pursuing final year in Bachelor of Engineering (B.E) in the Electronics and Communication Department, Panimalar Engineering College, Chennai, Anna University. Her fascination towards the Electronics field burgeoned; she mainly focused on Low Power VLSI design for reducing power and jitter in this work. Her interest includes in Digital image Processing and Communication Networks.

Mrs. N. ARUN PRIYA, M.E. completed the B.E. (ECE) Degree from the Anna University, Chennai in 2009 and M.E. (Applied Electronics) degrees from the Anna University, Coimbatore in 2012 respectively. She worked as Assistant Professor for a year in Apollo Engineering College. She is currently working as Assistant Professor in Panimalar Engineering College, Chennai till now. She Published 4 international journal and 2 paper presented in national conference. Her interest includes Low Power VLSI and High Speed system Design and Digital Image Processing.