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Performance Analysis of Multilevel Inverter Using LFPWM Technique

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ABSTRACT: Cascaded multilevel inverters (CMLI) have gained an edge over the other conventional topologies due to their modularity and ease of extendibility. The size, cost and control complexity of the CMLI can be greatly reduced by bringing count multilevel inverter topology is proposed and it is analysed with four different low frequency pulse width modulation LFPWM techniques. The performance of the proposedsystem, is compared with other cascaded CMLI topologies in terms of the total harmonic distortion, number of switches, levels and dc sources. The simulated results and the comparative analysis are presenteddown the number of switches employed in inverter topology. In this paper, one such reduced device is proposed.

KEYWORDS: Multilevel inverters, reduced device count, total harmonic distortion, LFPWM, half height

I.INTRODUCTION

Multilevel inverters (CMLI) have recently gained increasing attention because of the significant advantages like low voltage stress across the switches, reduced harmonic distortion, modularity and ease of expandability [1]-[6]. The stepped voltage waveform generated by the CMLI can get closer to sinusoidal waveform if the number of voltage steps is increased. This results in lesser harmonic distortion and filtering requirements. However the major drawback is that more number of switches is to be included in the topology to increase the number of voltage steps. Increasing the device count will result in lesser efficiency and reliability.

The basic unit of the conventional cascaded CMLI is the H bridge unit which has one dc source and four unidirectional switches. It can generate three unique voltage levels (0, +Vdc and -Vdc) at the output. The H bridges (basic units) can be connected in series to increase the number of voltage levels. The cascaded CMLI structure is further classified in two types as symmetric and asymmetric based on the magnitude of the dc voltage sources incorporated. In symmetric topology all the dc sources will have the same magnitude (V_{dc}).

The magnitudes are chosen to be in a geometric progression of two (binary) or three (trinary) in asymmetric arrangement. The symmetric structure with ‘m’ cascaded basic units can generate 2n+1 voltage levels. The asymmetric structure on the other hand can generate 2(m+1)-1 and 3n levels for binary and trinary progression respectively [1]. The number of voltage levels is more in case of trinary than that of the binary for the same number of switches. The higher the number of voltage steps the lower will be the harmonic distortion. More number of basic units is to be cascaded to increase the number of voltage steps which in turn increases the step to switch ratio. Increased devicecount reduces efficiency and reliability. This significant drawback of the conventional cascaded CMLI has opened up the research on the development of topologies utilizing reduced device count. Many such RDCCMLI topologies have been reported in literature [7]-[12]. In this paper, one such recently proposed topology is considered and this topology is modified so as to increase the number of voltage steps. The modified topology is analyzed with various low frequency LFPWM techniques. The metrics of the proposed topology are compared with that of the reference topology in terms of the device count, dc sources .

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II.THE RDCMLI

The topology proposed by Mahrous&Essam is a reduced device count topology that makes use of a basic unit and has two unidirectional switches and one dc voltage source as highlighted in Fig 1. When switch S_1 is turned on the voltage across basic unit is V1 and when the switch S_2 is turned on voltage across basic unit is zero. More number of voltage levels can be generated in the output by cascading basic units. The cascaded structure is connected to H-bridge to generate voltage levels of bothpolarity. The output voltage is positive when the switches H_1 and H_2 are turned on. The polarity is negative if switches H_3 and H_4 are turned on. The generalized structure with the 'm'cascaded basic units is presented in Figure 1.

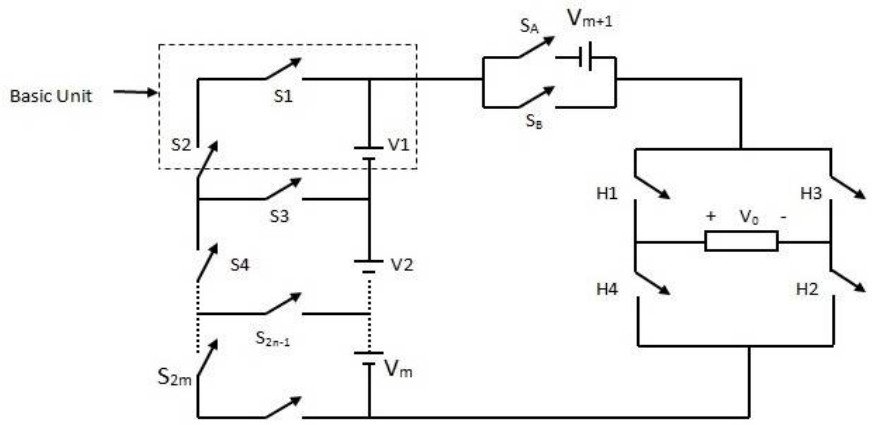

Figure 1: Topology in [13] with n=3

This topology can generate 2m+1 levels in symmetric configuration where the magnitudes of all the dc sources are chosen to be same. In asymmetric configuration V_1 is chosen to be the V_{dc}, V_m is chosen to be the 2 V_{dc} and all the remaining dc sources are chosen to be $3V_{dc}$ ($V_3=V_4=...=V_{n-1}=3V_{dc}$). This arrangement can generate 6(m-1)+1 voltage levels for m>1. The metrics of this topology are summarized in the Table 1.

Table 1
Metrics of the topology in [13]

	Symmetric	*Asymmetric*
Number of cascaded units	M	M
Number of switches	2m+5	2m+5
Number of levels	2m+1	6(m-1)+1
Number of dc sources	M	M
Level /switch ratio	[2m+1]/[2m+5]	[6(m-1)+1]/[2m+5]
Variety of dc sources	1	3

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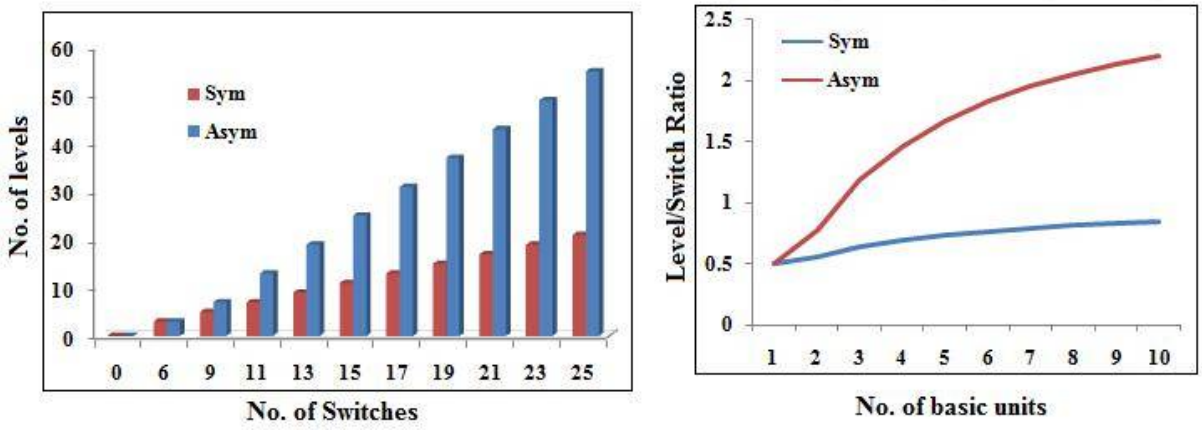

Figure 2: Comparison between the symmetric and asymmetric configuration

It can be inferred that asymmetric configuration results in more number of levels than that of the symmetric counterpart. The level to switch ratio is also plotted and it is found that ratio increases with the number of cascaded units m. Further, the ratio is higher fora asymmetric configuration.

III.THE PROPOSED MODIFICATION

The topology presented in the previous section is modified to increase the level to switch ratio. The proposed topology has three functional units namely, the sub unit, the Supplementary unit and the sign generator as shown in Figure 3.

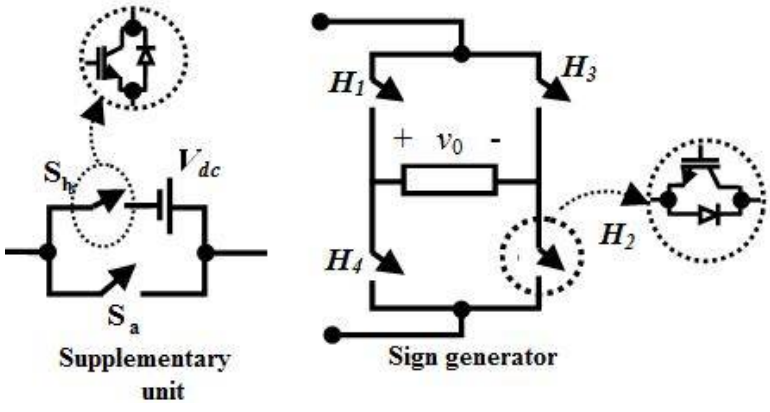

Figure 3: The Standby unit and sign generator

The sub unit comprises of cascaded basic units m and the structure of the basic unit of the proposed topology is similar to the one presented in section 2. Standby unit is included in structure to increase switch ratio. The Standby circuit consists of two unidirectional switches and one dc voltage source. One of the switches is connected in series with dc source while second switch is connected across the source-switch assembly. The sub unit together with the Standby unit generates the voltage levels and it is called level maker unit. Further, the level maker generates only the positive voltage levels. The negative voltage levels are generated by the full inverter (H-bridge) circuit and hence it is called the sign generator unit. The status of the switches in these units and the corresponding output they generate are

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presented in Table 2. The voltage of the level maker unit (V_{lm}) is equal to the sum of the voltage across the sub unit (V_{sub}) and Standby unit (V_{sup}).

Table 2

Status of switches and the output

	Switches in 'on' state	*V_{out}*
Standby unit	S_a	V_{sub}
	S_b	$V_{sub} + V_{sup}$
Sign generator	H_1& H_3	0
	H_1& H_2	+ V_{lm}
	H_3& H_4	- V_{lm}
	H_2& H_3	0

The three functional units are combined to generate stepped voltage waveform at the output and the generalized structure of the proposed topology.

The output voltage (Vout) of the proposed topology is equal to the sum of voltages across the sub unit (Vsub) and the Standby unit (Vsup) and it is given by

$$Vout = Vsup + Vsub \quad (1)$$

The sign of the generated voltage is dictated by the switches in the sign generator. The number of sources employed and the switches involved in the proposed structure with 'm' cascaded basic units are given by

$$\text{Number of sources } (M_{sor}) = \text{Number of basic units} = m \quad (2)$$

$$\text{Number of switches } (M_S) = 2m+7 \quad (3)$$

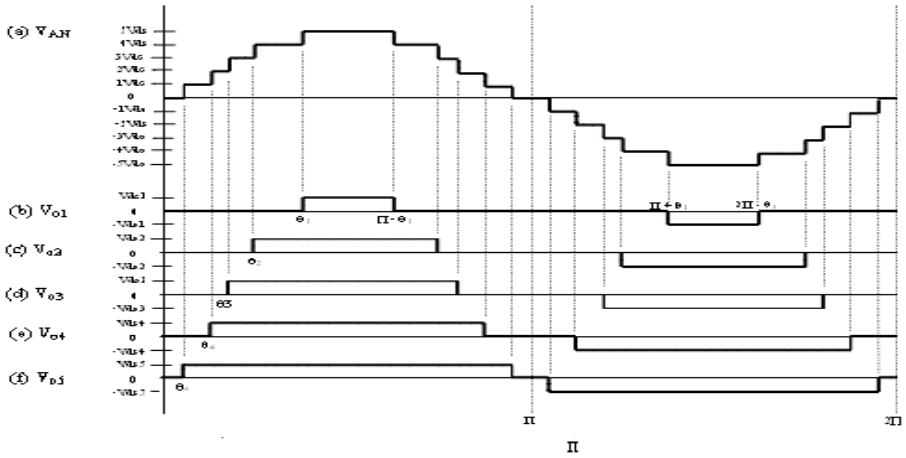

Figure.7.PWM with nearer pulse to sine wave

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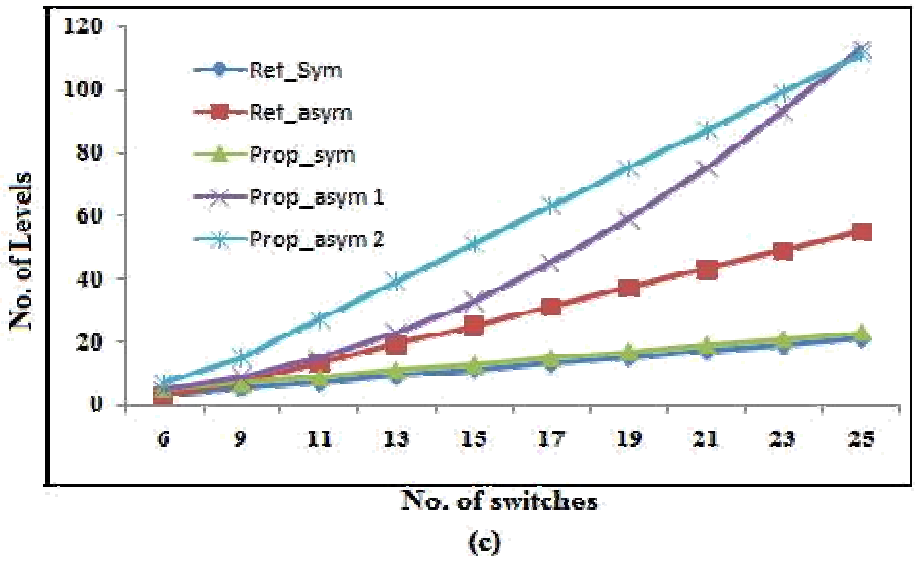

The voltage waveform has 9 distinct levels as ± 20V, ± 40V, + 60V, and 0 V. The total harmonic distortion is found to be 9.48%. The harmonic distortion can further be reduced by cascading more basic units and employing suitable filter circuit. The required dc supply may be obtained from batteries, fuel cells or solar PV panels.

4.2. Comparison of proposed topology with the reference topology

The proposed topology is compared with the reference topology in terms of sources, switches and voltage levels. The proposed topology makes use of a Standby unit which has a dc source. Hence, the source requirement is more in case of the proposed topology.

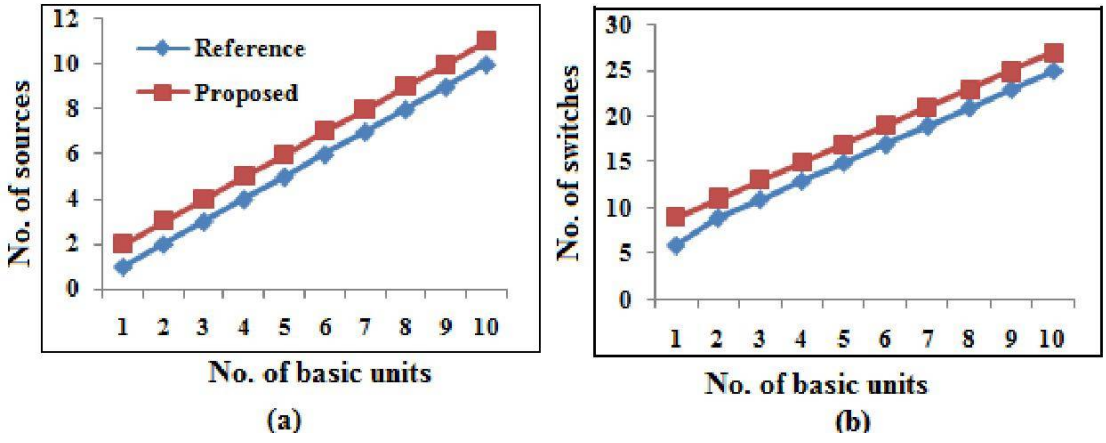

Figure 8: Comparion of proposed topology with the reference topology

For a structure with ‘m’ basic units, the proposed topology employs 'mm+1' sources whereas, the reference topology uses only ‘m’ sources. The proposed inverter structure employs two additional switches and hence the ratio of switches to basic unit is slightly higher. The additional switches are due to inclusion of Standby unit which consists of two unidirectional switches. The proposed structure is capable of generating more number of levels than that of the reference topology in both the symmetrical and asymmetrical arrangement. As a result, the level to switch ratio is

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higher for proposed topology. Though the inclusion of Standby unit increases the number of sources and switches by one and two, the level to switch ratio of the proposed topology is significantly higher than the reference topology. It is preferred to employ scheme 3 to determine the dc source magnitudes if the cascaded units are lesser than ten and scheme 2 if the cascaded units are greater than ten.

In this scheme, each node with message searches for possible path nodes to copy its message. Hence, possible path nodes of a node are considered. Using NSS, each node having message selects its path nodes to provide a sufficient level of end-to-end latency while examining its transmission effort. Here, it derives the CSS measure to permit CR-Networks nodes to decide which licensed channels should be used. The aim of CSS is to maximize spectrum utilization with minimum interference to primary system. Assume that there are M licensed channels with different bandwidth values and ydenotes the bandwidth of channel c. Each CR-Networks node is also assumed to periodically sense a set of M licensed channels. Midenotes the set including Ids of licensed channels that are periodically sensed by node i. suppose that channel c is periodically sensed by node iin each slot and channel c is idle during the time interval xcalled channel idle duration. Here, it use the product of channel bandwidth yand the channel idle duration x, tc= xy, as a metric to examine the channel idleness. Furthermore, failures in the sensing of primary users are assumed to cause the collisions among the transmissions of primary users and CR-Networks nodes.

IV.CONCLUSION

This paper has proposed a new reduced device count cascaded CMLI topology by including a Standby unit to reference topology. The structure of three fundamental units and their working are explained. The generalized structure of this proposed topology and three different schemes by which the magnitudes of dc sources can be determined are also presented. A 11 level inverter is developed and simulated to validate the proposed structure and schemes. The performance of the 11 level inverter is also compared for different low frequency LFPWM schemes and the results showed that HH LFPWM results in lesser distortion. Further, the proposed structure is compared with the reference structure in terms of sources, switches and number of voltage levels and it is found that level to switch ratio is higher for the proposed topology than that of reference topology.

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