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Design and Applications of Schottky Barrier Carbon Nanotube Field Effect Transistor

M.S.Raviteja[1], M V Rajarao[2], CVSR Phanikiran[3], C.Madhu Shalini[4], KLN Rao Omsrivathsa[5]

Sr. Engineer, Veramasa, Hyderabad, India

Sr. Engineer, Veramasa, Hyderabad, India

Engineer, Veramasa, Hyderabad, India

Engineer, Veramasa, Hyderabad, India

ABSTRACT:The difficulty in shrinking silicon transistor past a certain feature size has been acknowledged. Carbon nanotube offer a technology with an existing solution to the scaling issues of transistor and interconnection with the possibility of coexistence in the present silicon technology.The goal of the present work is to propose circuit model for carbon nanotube filed transistor and apply them to aspects of digital circuit design. This research models the current voltage characteristics are similar to MOSFET's but with a few caveats under standard conduction, the device do not enter saturation. Also, it is shown that CNTFETs are ambipolar devices with maximum current $v_{ds}/2$.Despite of this distinction from MOSFETs, CNTFETs show impressive voltage transfer characteristics, even at low voltage.The large noise margin and notable output voltage swing can be trade-off for higher on current depending on the nanotube diameter is shown in this network .Thus digital designer have an ability to control performance and power by changing the nanotube diameters. Carbon nanotube FETs can become prominent in the arenaof array device , which are a technical front runner for the integration of wire and transistor .This work show that carbon nanotube field effect transistor have strong potential in read only memory array.

I.INTRODUCTION

The electronics industry continues to push the limits of Moore's Law. However, the physical restrictions of scaling metal oxide semiconductor field effect transistors (MOSFET) are becoming more prevalent; as these limitations arise, alternative technologies must replace the standard silicon technology. Completely disruptive technologies are being researched and among them carbon nanotubes offer a technology with a unique solution to scaling transistors and interconnects and with the possibility of integration into the well-established current Silicon technology, in the near future. Since the discovery of carbon nanotubes in 1991, their many extraordinary properties and applications have been researched closely. Carbon nanotubes (CNT) can grow up to millimeters in length however, their diameters are around 1nm to 40nm. These long thin nanotubes can withstand incredibly high current rates and can be used as both metal wires and channels of field effect transistors (FET). With these impressive properties, CNTs can aid the problem of shrinking electronics.

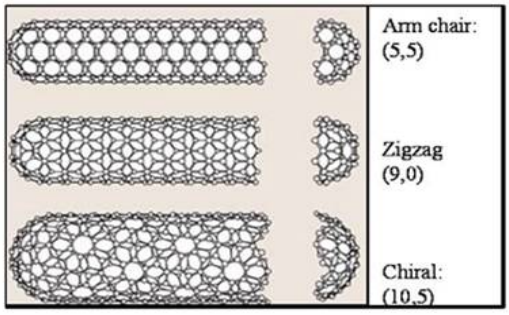

Fig:1 Carbon nanotube cylinders varying chirality

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I.II .CARBON NANOTUBES AS TRANSISTORS

The transport of electrons and holes in carbon nanotubes (CNT) has been described below: Carbon Nanotubes Structure, Properties, and Growth. Semiconducting single walled CNT current can be modulated with a voltage and can have similar IV characteristics to a metal oxide semiconducting field effect transistor (MOSFET). Therefore, these s-CNTs can be used in FET devices, but with higher current rates and a possibility for better scaling characteristics compared to Silicon devices. There are two main types of carbon nanotube FETs differing by their current injection methods: Schottky barrier FETs [5] [6] [8], and doped CNTFETs, [10] [19]. This research only models Schottky Barrier (SB) carbon nanotube FETs.

II.MODEL AND CURRENT WORK

It has been shown that semiconducting carbon nanotubes can be used as the conducting channel in Schottky barrier carbon nanotube FETs (CNTFET). [4] [5] [6] [7] [8]. To create such devices, nanotubes are grown on top of a thick silicon dioxide, which is itself on a silicon wafer. Metal contacts, commonly made of Titanium or Cobalt, are placed over the nanotube to create source and drain contacts. To form a strong interaction between the metal and the nanotube, the metal is annealed at 850°C for approximately 100 seconds to form metal carbides.[29] These high annealing temperatures are acceptable because the carbon nanotube structure can withstand temperatures up to its melting point of around 3,000°C. To understand the operation of a Schottky barrier CNTFET, the energy band diagram for the structure should be studied. At the intersection between the metal carbide contacts and the semiconducting carbon nanotube, Schottky barriers are created. The energy band diagrams in Figure 2 illustrate this situation. The current in CNTFETs is from the tunneling of carriersthrough the Schottky barriers. The type of metal for the contacts is chosen so that its work function forces the metal Fermi Level to lie between the valance and conduction band of the CNT, hopefully lining up approximately in the center of the s-CNT's energy band. The work function for Al is 4.2eV and Ti is 3.9eV; these are similar to the work function of a CNT with a diameter of 1.4nm (≈4.5 eV). [11] Titanium is used most frequently because of its stable carbide. [11] For the strongest nanotube to contact interactions, the contact is best placed a the end of a nanotube, because of possible loose carbon-carbon bonds within the tube structure However, if many transistors are placed along the length of a nanotube, tube-end contacts are not always possible. At sufficiently short channel lights, the CNT channel can become ballistic and hence, the metal contact resistance and the Schottky barriers at the source and drain ends limit the current drive through the nanotube. Thus, a low contact resistance, such as that of Titanium, is desirable. Presently, the control of the metal contacts to carbon nanotubes is not consistent and the tunneling current levels between transistors can vary greatly, even on the order of magnitude. This problem must be addressed before mass numbers of CNT circuits can be realized. The thickness of the source Schottky barrier at the metal Fermi level decreases exponentially with an increasing gate to source voltage. Thus, the tunneling current through the Schottky barrier increases exponentially, inversely to the barrier thickness. The I_d versus V_{gs} graphs do not differ greatly with a changing Vds because the drain voltage does not significantly control the source Schottky barrier. If the gate voltage increases in the opposite direction, with a positive V_{gs}, thesame effect will occur due to the Schottky Barrier on the opposite side of the s-CNT energy band however, since the metal Fermi level is further away from the conduction band, a larger gate voltage is needed to achieve similar current levels.

II.II OPERATION

Typically CNTFETs are PFETs. When a negative voltage is applied between the drain and source, the band structure, of the CNT, is modulated to account for the drain to source voltage (V_{ds}) as shown in Figure 2. When a small negative gate to source voltage is applied, a CNTFET is in the subthreshold regime. With a negative gate voltage applied, the Schottky barrier width at the source is modulated, allowing for holes to tunnel through the valence band and pass unimpeded to the drain. The transistor threshold voltage, where the device acts similarly to an 'on' MOSFET, is reached when the metal source Fermi level is approximately even with the valence or conduction band of the s-CNT, in a p-channel or n-channel respectively. If the gate voltage continues to increase above this threshold, the Schottky barrier thickness at the source will remain constant and thecurrent will not continue to increase exponentially. Above the threshold voltage, the current will only increase linearly with V_{ds}. . Above the CNTFET threshold voltage, the current voltage characteristics look very similar to a MOSFET's IV characteristics the current increases linearly with V_{ds}; and, when the barrier at the drain is completely eliminated, the FET current saturates.

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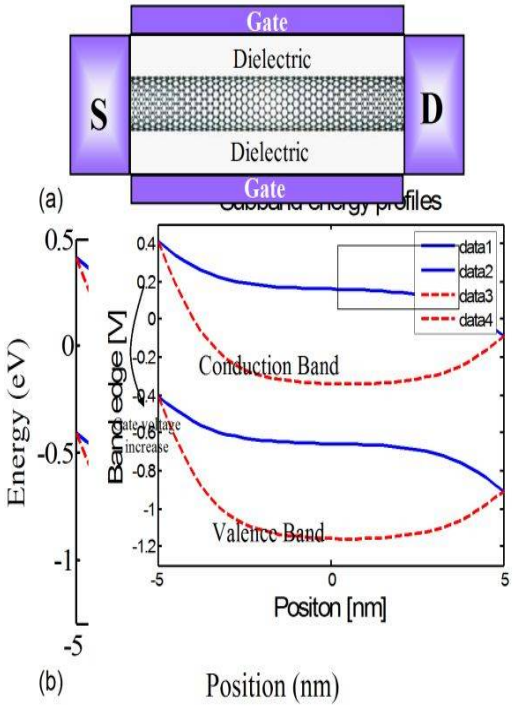

Fig 2

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III.CAPACITANCE, ENERGY, AND DELAY OF SUB THRESHOLD CNTFETS

In order to find the delay and energy characteristics of a carbon nanotube FET device, the capacitance of the transistors must be ascertained. The main types of capacitances are the gate capacitance (C_{gate}), the drain to bulk capacitance (C_{db}), the overlap capacitance ($C_{overlap}$), and the Miller capacitance (C_{Miller}). Looking first at the gate capacitance, a nanotube is grown on a thick silicon dioxide and then surrounded by a thin gate oxide (assumed to be SiO_2 in this research, with $\epsilon ox=3.9$). A metallic gate rests on the thin oxide, creating a coaxial capacitance structure with the nanotube at the center, shown in A of Figure 3; however, because the nanotube lays directly on the bulk oxide, the actual capacitance is described by B in Figure 3.1. Also, the metal gate extends not just over the nanotube, but over the width of the transistor, which is dictated by the lithographic specifications for minimum metal width and minimum via size. Because of the large metal gate width, the gate to bulk or back-gate capacitance must also be considered .In the gate capacitance measurements here, the nanotube will be treated as an equipotential metal. The gate capacitance of a MOSFET depends on the existence and size of the conducting channel; therefore, the capacitance depends on the region of operation for the transistor. This is not the case in a CNTFET. The conducting channel of a CNTFET, is the carbon nanotube itself and thus, the channel exists independently of the FET operation. If no current is flowing, which only happens when there is no potential different across the transistor, the channel will be considered an insulator and the gate capacitance will only consist of the parallel plate capacitance from the gate metal to the back gate. However, in any active regime, there will be either off- or on-currents flowing through the carbon nanotube and it can be modeled as a equipotential metal cylinder; in this case, the gate capacitance is composed of both a gate to nanotube and gate to bulk capacitances. Treating the CNT classically will give an overestimate for the capacitance in a classical coaxial formation such as A of Figure 3, the capacitance per channel length is $\{Cgate/ L\} = \{2\pi\epsilon_{ox} /\log (t_{ox} /R +1\}$, if the nanotube is treated as an equipotential. In the case given by B, the gate capacitance is less, however, it is not just described by the percentage of the CNT covered by the gate. As shown in B, of Figure 3, the gate has influence on the

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lower section of the nanotube, not covered by the gate, due to fringe capacitance. However, the fringe capacitance will not be considered in this model. Therefore, the model has an overestimate from treating the nanotube classically and an underestimate from neglecting fringe capacitance. The CNT to bottom silicon plate must also be considered for the gate capacitance measurements, however, is neglected here due to the thick bulk oxide, $T_{ox-bulk}$, and narrow carbon nanotube. Reference [9] describes the gate to nanotube capacitance in terms of arrays of CNT devices. If nanotubes are placed below a certain pitch, where pitch is defined as the distance between the centers of two nanotubes, screening between nanotubes will become important for capacitance measurements.

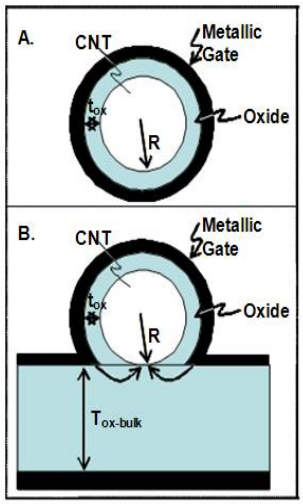

Fig 3

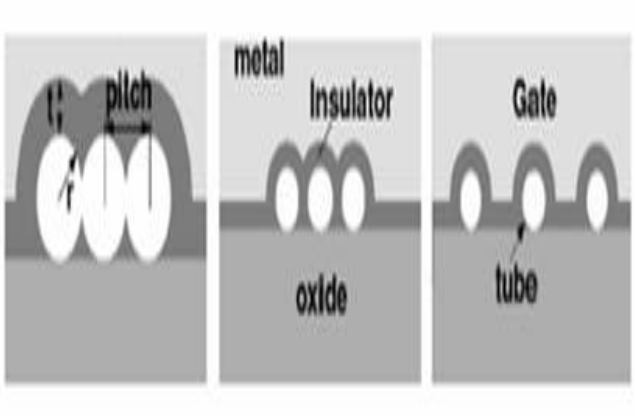

Fig 3.1

The point where screening becomes an issue is at a pitch of $2(t_{ox} + R)$, where R is the CNT radius and t_{ox} is the thickness of the SiO_2 gate oxide. The gate to CNT coupling capacitance is stronger for the edge nanotubes, so the general capacitance in [9] is given for the middle nanotubes within an array. In this research, the pitch between nanotubes will be greater than $2(t_{ox} + R)$. Gives data for the gate to nanotube capacitance per channel length for one nanotube in the middle of an array, versus the pitch between the arrays of nanotubes. To simplify the capacitive calculations in this research, the capacitance of B in Figure 3is used, which is less than actual capacitance due to the extra fringe capacitance.$(C_{gate} – C_{partial})/L=(2\theta+\pi)/2\pi *(C_{gate} – \text{channel})/L$ where $2\theta+\pi$ represents the angle of the CNT cylinder covered by the metallic gate(θ = arc sin (1/1+(tox/R))). The partially covered cylindrical capacitance will be used in this research, however, this is an underestimate of the capacitance. The model assumes that screening between nanotubes is not a true consideration because the pitch $\geq 2(R+Tox)$. The gate capacitance per channel length for one

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nanotube has been described above. The actual value of the capacitance differs depending on the channel length. The channel length and metal gate width are considered to be controlled by the metal pitch needed for the gate, source, and drain contacts in future generations, according to the 2003 ITRS Roadmap. [10] .All future gate capacitance calculations will include the gate to nanotube capacitance for one nanotube, unless otherwise specified,the gate to bulk capacitance. The gate capacitance consists of both the metal gate to back gate and the metal gate to nanotube capacitances. The gate to nanotube capacitance depends on the nanotube diameter. Here the two types of gate capacitances are graphed versus the future lithographic generations for multiple nanotube diameters (D_t). The back gate oxide thickness is 100nm, compared to the gate oxide thickness of [1.1,08,0.65,0.55,0.5] for years[2007,2008,2013,2016,2018] respectively. The channel lengths are dependent on the ITRS Roadmap's lithographic specifications.

III.I .CAPACITANCE IN RELATION TO LITHOGRAPHY

The capacitance is greatly affected by the lithograph dimensions. The dimensions of metal contacts are much larger than the radii of a carbon nanotubes and the t_{ox} of a gate. The minimum metal dimensions will control the contact sizes, the necessary gate overlap, and the width between the metallic gate, and the metal source/drain contacts. Contrary to CMOS poly gates, a metallic gate has much less resistance; however, the scaling relies on metal dimensions. Thus, many parallel nanotubes can be placed under a metallic gate, source, and drain contact without increasing the minimum metal contact or gate sizes. Also, the channel length of a CNTFET will not be limited by the carbon nanotube, but instead by the metal minimum lithographic pitch between the sources, drain, and gate vin as contacts. The lithographic dimensions effect the capacitance by the following: the gate capacitance depends on the number and the diameter of the CNTs and to a lesser extent, the width and length of the channel in comparison to the back gate. The overlap capacitance depends on both the width and the length of the overlap and thus, scales quadraticaly as the generation scales. With the capacitance of inverter structures known, the time delay (T_{delay}) of an inverter can be found from $T_{delay} = C_L * \Delta V / I_{average,\ where}\ \Delta V = V_{dd}/2$.[31]. It was shown above that the capacitance in the near term relies on the parasitic drain and miller capacitances,which are independent of the number of CNTsper gate or the nanotube diameter. Thus, a transistors time delay is dependent on the transistors average current ($I_{average}$). When considering an inverter, if the V_{in}=0V, then the PFET will pull the output node high. $I_{average}$ for this case is the average between I ($V_{ds}=V_{dd}$) and I ($V_{ds}=V_{dd}/2$). As previously described, the average on-current increases with diameter and drain control. The diameter of a CNT transistor can be used as a trade-off for performance, energy, and voltage swing. These trade-offs can be used to a circuit designer's advantage. If high performance is required for a circuit structure, larger nanotubes can be implemented with the knowledge and understanding that the noise margin and high/low output voltage swing. The contacts dictate the current levels and the metal contacts to carbon nanotubes differ dramatically, even among transistors along the same CNT. During the contact annealing process, a different number of carbon-carbon bonds are broken within the nanotube structure and thus, there is a different level of connection between the contact and nanotube. This difference leads to a limited ability of modern CNTs to be use in circuits. However, in general, once the process variations are controlled, carbon nanotubes can excel in digital circuit designs because of the large $I_{on:}$ I_{off} ratio and high current drives.

IV.RESULT

Carbon nanotubes can have very impressive current characteristics, however as it was mentioned above and in as Subthreshold Carbon Nanotube FETs, the process variations have to be controlled more closely before the use of CNTFETs will become prolific. It is very difficult to assume a certain current level for a particular CNT device due to large process variations. This thesis research has carefully considered carbon nanotube field effect transistors in the subthreshold regime and their applications to an inverter structure. This chapter will model and characterize CNTFET devices above threshold, in both the triode and saturation regimes. IBM has generously given data for a carbon nanotube transistor in these two regimes, focusing on the triode regime. The IBM data of a CNTFET above threshold. The IBM data here and in the sub threshold chapter are not for the same transistor devices; the device characteristics do not match perfectly. CNTFET's I_d versus V_{ds} curve; it resembles the IV characteristics for a MOSFET in the triode regime. Just as with MOSFETs, the triode and saturation regions of CNTFETs are dependent on the source voltage in respect to both the drain and gate voltages. At the threshold voltage of a transistor, the subthreshold regime ends and the CNTFET enters the linear or triode regime. Here, the Schottky Barrier (SB), at the source end of the transistor does not change in thickness with a varying gate voltage. Instead the tunnelling current is controlled by the drain SB barrier.

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The carbon Nano tubes are cylinders that grow up to millimetres in length with diameters in the nanometres ranges; these long cylinder can aid in scaling because of their unique properties the work presented in this paper displays their potential within digital circuits design by creating a mode and applying that modal to low voltage circuit and ROM array.

1999 ITRS Table	2006 100nm	2009 70nm	2012 50nm	2015 35nm
MOSFET:Max I_{off} (for LOP) @25C(nA/ µm)	3	10	10	2
MOSFET: Nominal I_{on} [NMOS/PMOS] (High perf) @25C(µA\ µm)	600/280	600/280	600/280	600/280
CNTFET: Max I_{off} for 2.5nm/1.3nm tube @one tube per contact(nA\ µm)	3.0e5/30	4.3e5/43	6.2e5/61	8.4e5/85
CNTFET: Nominal I_{on} for 2.5 nm/1.3nm @one tube per contact (µA\ µm)	377.4/37.4	440/44	580/58	740/74
CNTFET:I_{on} for 2.5/1.3nm @ 12 tubes per contact (µA\ µm))	4000/769	4000/769	4000/769	4000/769

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